

DESCRIPTION

The 3818 group is designed mainly for VCR timer/function control, and include six 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and an 8-channel A-D converter.

The various microcomputers in the 3818 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

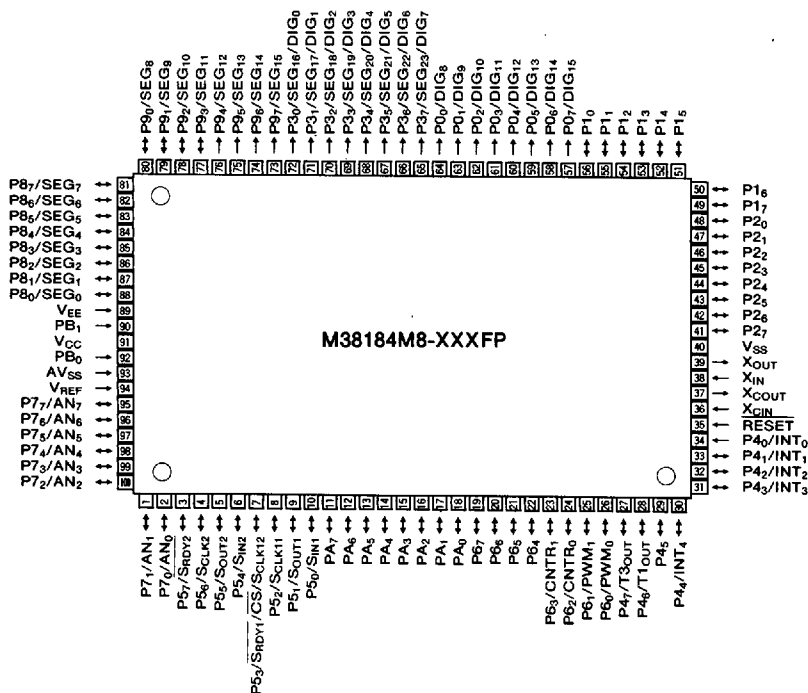
- Basic machine-language instructions 71
- The minimum instruction execution time 0.48 μ s
(at 8.4MHz oscillation frequency)
- Memory size
 - ROM 4K to 60K bytes
 - RAM 192 to 1024 bytes
- Programmable input/output ports 67
- High-breakdown-voltage I/O ports 12
- High-breakdown-voltage output ports 20
- Interrupts 18 sources, 15 vectors

- Timers 8-bit×6
- Serial I/O Clock-synchronized 8-bit×2
(Serial I/O1 has an automatic data transfer function)
- PWM output circuit 14-bit×1
8-bit×1 (also functions as timer 6)
- A-D converter 8-bit×8 channels
- Fluorescent display function
 - Segments 8 to 24
 - Digits 4 to 16
- 2 Clock generating circuit
 - Clock (X_{IN} - X_{OUT}) Internal feedback resistor
 - Sub-clock (X_{CIN} - X_{COUT}) Without internal feedback resistor
- Power source voltage 4.0 to 5.5V
- Low power dissipation
 - In high-speed mode 50mW
(at 8.4MHz oscillation frequency)
 - In low-speed mode 300 μ W
(at 32kHz oscillation frequency)
- Operating temperature range -10 to 85°C

APPLICATIONS

VCRs, microwave ovens, domestic appliances, ECRs, etc.

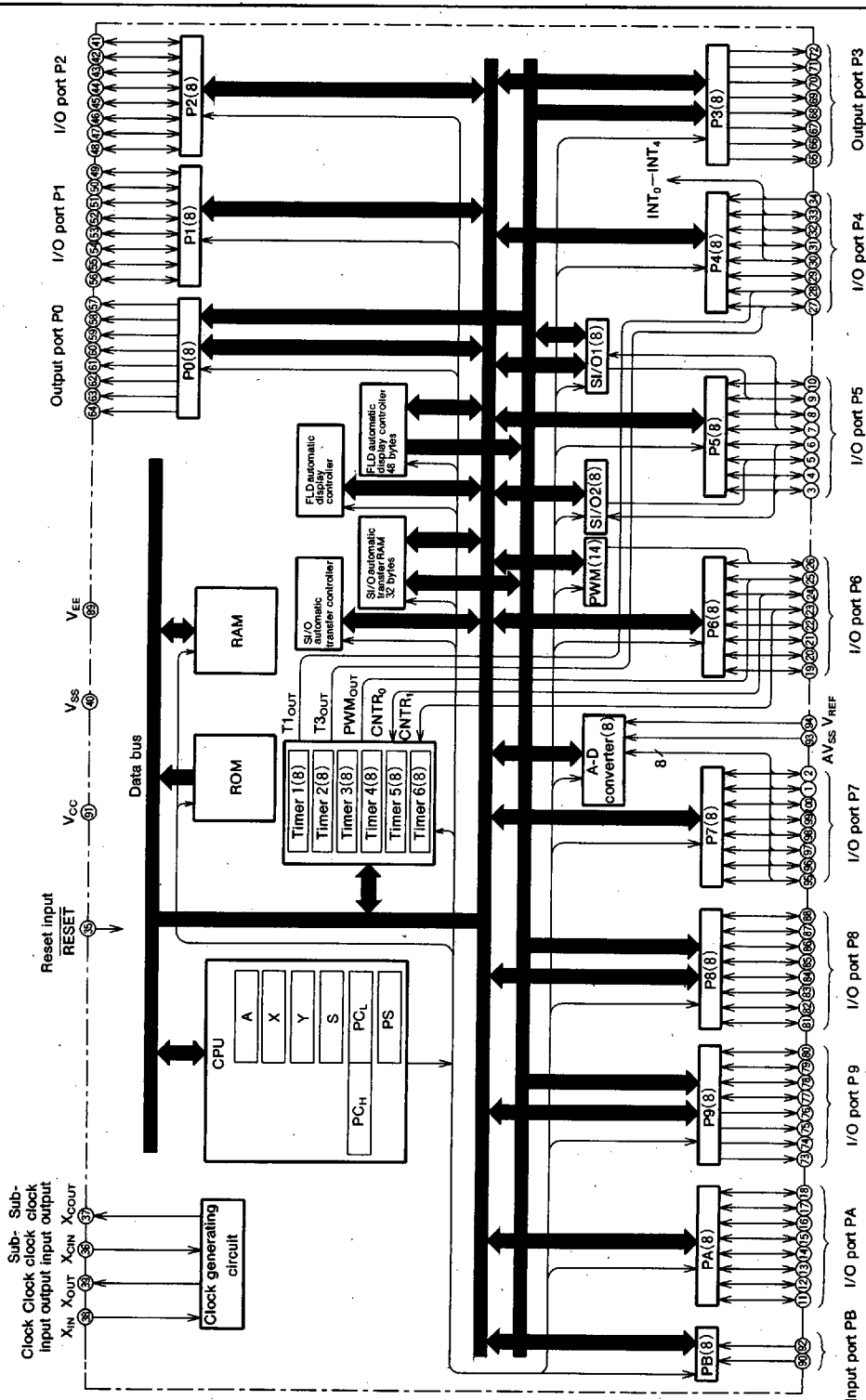
PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A
100-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL BLOCK DIAGRAM (100P6S-A)



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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Function	
			Function except a port function
V_{CC}, V_{SS}	Power source	Apply voltage of 4.0 to 5.5V to V_{CC}, and 0V to V_{SS}.	
V_{EE}	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P3 and P9.	
V_{REF}	Analog reference voltage input	Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	- GND input pin for A-D converters - Connect to V_{SS}.	
$\overline{RESET}$	Reset input	Reset input pin for active "L"	
X_{IN}	Clock input	- Input and output signals for the clock generating circuit. - It consist of internal feedback resistor. - Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. - If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. - This clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
X_{CIN}	Sub-clock input		
X_{COUT}	Sub-clock output	- Input and output signals for the internal sub-clock generating circuit. - It consist of without internal feedback resistor. Connect a ceramic resonator or quartz-crystal oscillator and external feedback resistor between the X_{CIN} and X_{COUT} pins. - If an external clock is used, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open. - This clock can also be used as the oscillating source of system clock.	
$P0_6/DIG_8 - P0_7/DIG_{15}$	Output port P0	8-bit output port - The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V_{EE} pin. V_{EE} pin level is output at reset.	FLD automatic display pins
$P1_0 - P1_7$	I/O port P1	8-bit CMOS I/O port - I/O direction register allows each pin to be individually programmed as either input or output. - At reset this port is set to input mode. - CMOS compatible input level - CMOS 3-state output structure	
$P2_0 - P2_7$	I/O port P2	8-bit CMOS I/O port with the same function as port P1 - CMOS 3-state output structure - TTL compatible input level	
$P3_6/SEG_{18}/DIG_0 - P3_7/SEG_{23}/DIG_7$	Output port P3	8-bit output port with the same function as port P0	FLD automatic display pins
$P4_0/INT_0$	Input port $P4_0$	1-bit CMOS input port	External interrupt input pin
$P4_1/INT_1 - P4_4/INT_4$	I/O port P4	7-bit CMOS I/O port with the same function as port P1 - CMOS compatible input level	External interrupt input pins
$P4_5$			
$P4_6/T1_{OUT}, P4_7/T3_{OUT}$			Timer 1, Timer 3 output pin

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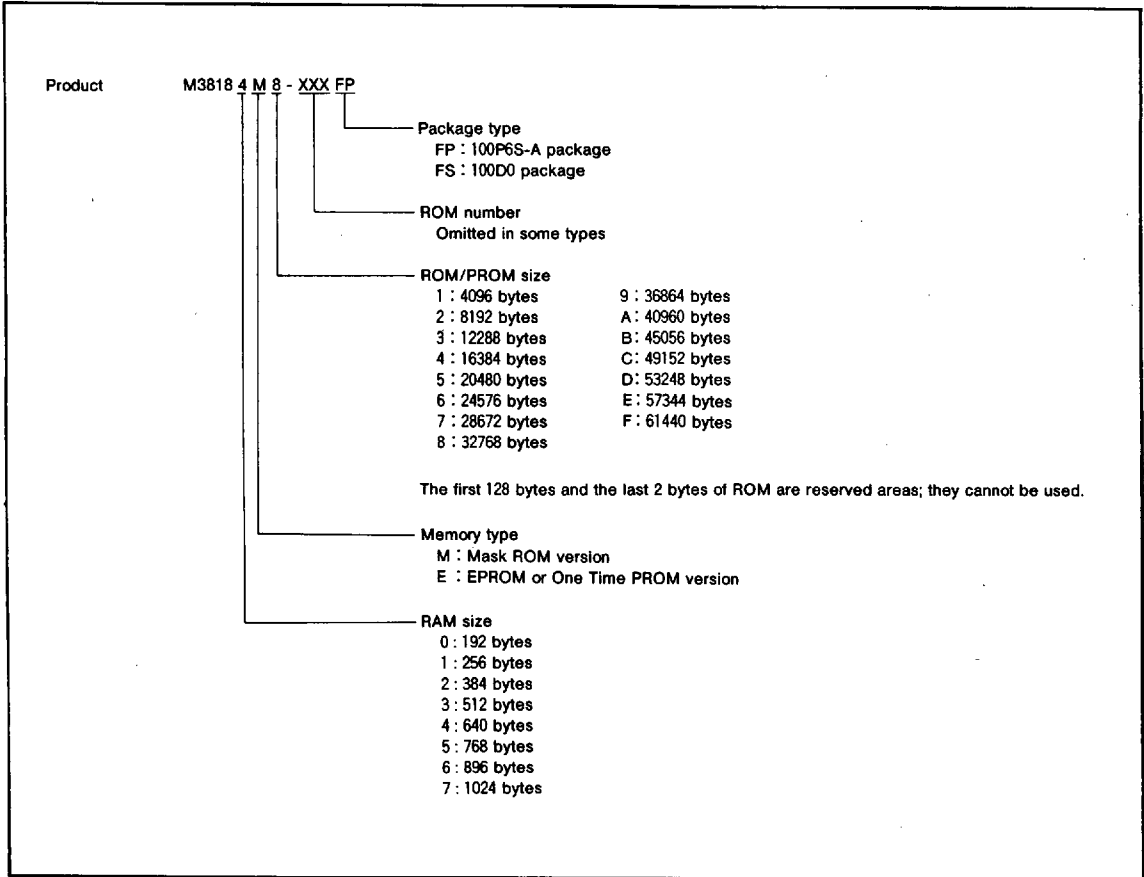
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Function	Function except a port function
P5 ₀ /S _{IN1} , P5 ₁ /S _{OUT1} , P5 ₂ /S _{CLK11} , P5 ₃ /S _{RDY1} / CS/S _{CLK12}	I/O port P5	• 8-bit I/O port with the same function as port P1 • N-channel open drain output structure • CMOS compatible input level • Keep the input voltage of this port between 0V and V_{CC}.	• Serial I/O1 I/O pins
P5 ₄ /S _{IN2} , P5 ₅ /S _{OUT2} , P5 ₆ /S _{CLK2} , P5 ₇ /S _{RDY2}			• Serial I/O2 I/O pins
P6 ₀ /PWM ₀	I/O port P6	• 8-bit CMOS I/O port with the same function as port P1 • CMOS compatible input level • CMOS 3-state output structure	• 14-bit PWM output pin
P6 ₁ /PWM ₁			• 8-bit PWM output pin
P6 ₂ /CNTR ₀ , P6 ₃ /CNTR ₁			• Timer 2, Timer 4 input pins
P6 ₄ —P6 ₇			
P7 ₀ /AN ₀ — P7 ₇ /AN ₇	I/O port P7	• 8-bit CMOS I/O port with the same function as port P1 • CMOS compatible input level • CMOS 3-state output structure	• A-D converter input pins
P8 ₀ /SEG ₀ — P8 ₇ /SEG ₇	I/O port P8	• 8-bit I/O port with the same function as port P1 • P-channel open drain output structure • CMOS compatible input level • Please note that this port does not have internal pull-down resistors.	• FLD automatic display pins
P9 ₀ /SEG ₈ — P9 ₃ /SEG ₁₁	I/O port P9	• 4-bit I/O port with the same function as port P1 • P-channel open drain output structure • CMOS compatible input level • This port has internal pull-down resistors.	• FLD automatic display pins
P9 ₄ /SEG ₁₂ — P9 ₇ /SEG ₁₅	Output port P9	• 4-bit output port with the same function as port P0	• FLD automatic display pins
PA ₀ —PA ₇	I/O port PA	• 8-bit CMOS I/O port with the same function as port P1 • CMOS compatible input level • CMOS 3-state output structure	
PB ₀ , PB ₁	Input port PB	• 2-bit CMOS input port	

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PART NUMBERING



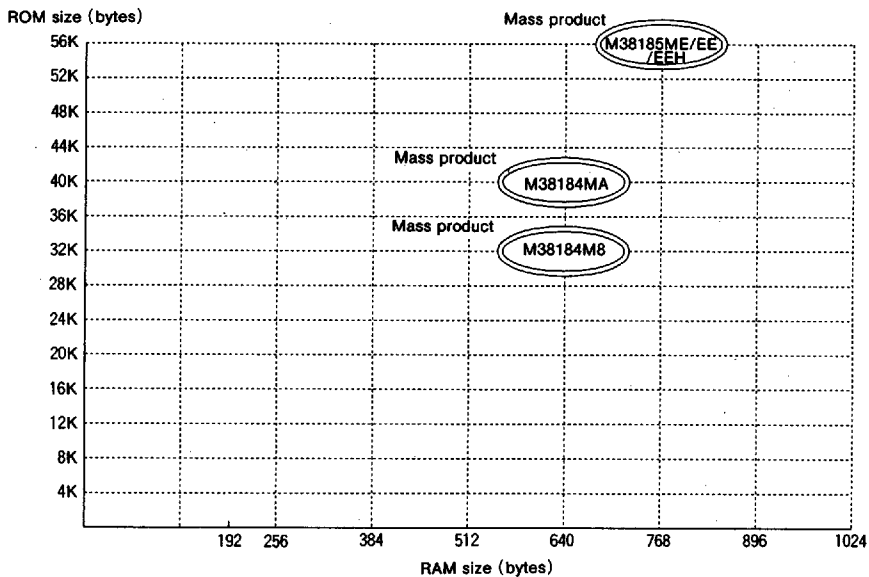
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GROUP EXPANSION

Mitsubishi plans to expand the 3818 group as follows:

- (1) Support for mask ROM, One Time PROM, and EPROM versions
- (2) ROM/PROM size 32K to 56K bytes
RAM size 640 to 768 bytes
- (3) Packages
100P6S-A Plastic molded QFP
100D0 Window type ceramic LCC

Memory Expansion Plan



Currently supported products are listed below.

As of May 1996

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38184M8-XXXFP	32768 (32638)	640	100P6S-A	Mask ROM version
M38184MA-XXXFP	40960 (40830)			Mask ROM version
M38185ME-XXXFP	57344 (57214)	768	100P6S-A	Mask ROM version
M38185EE-XXXFP				One time PROM version
M38185EEFP			100D0	One time PROM version (blank)
M38185EEFS				EPROM version
M38185EEHXXXFP			100P6S-A	One time PROM version
M38185EEHFP				One time PROM version (blank)
M38185EEHFS			100D0	EPROM version

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 3818 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL and DIV instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 003B₁₆.

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

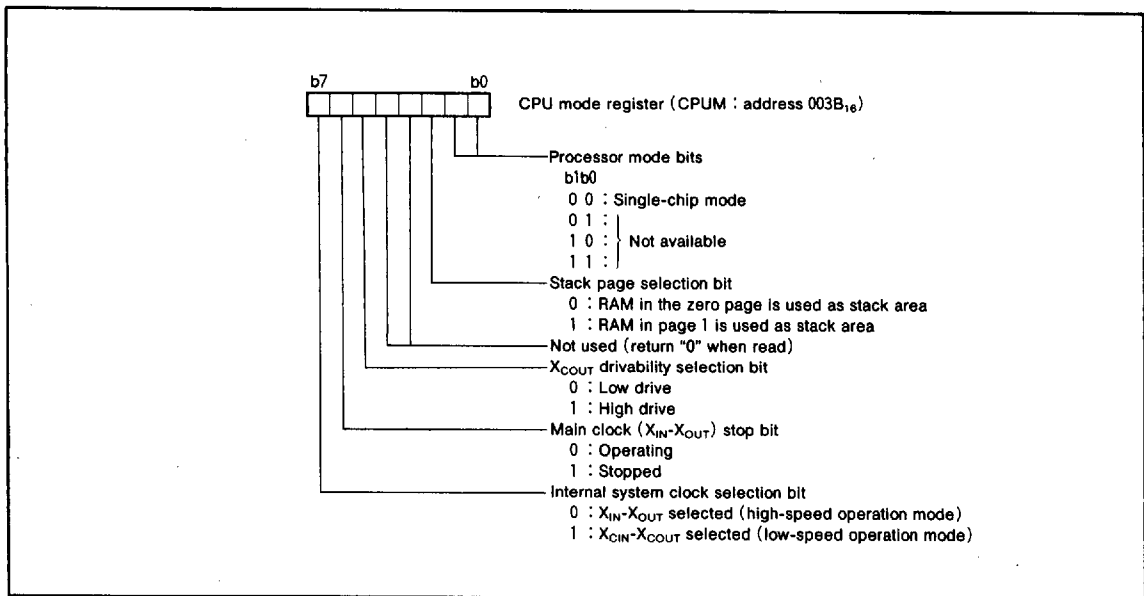


Fig. 1 Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of sub-routine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

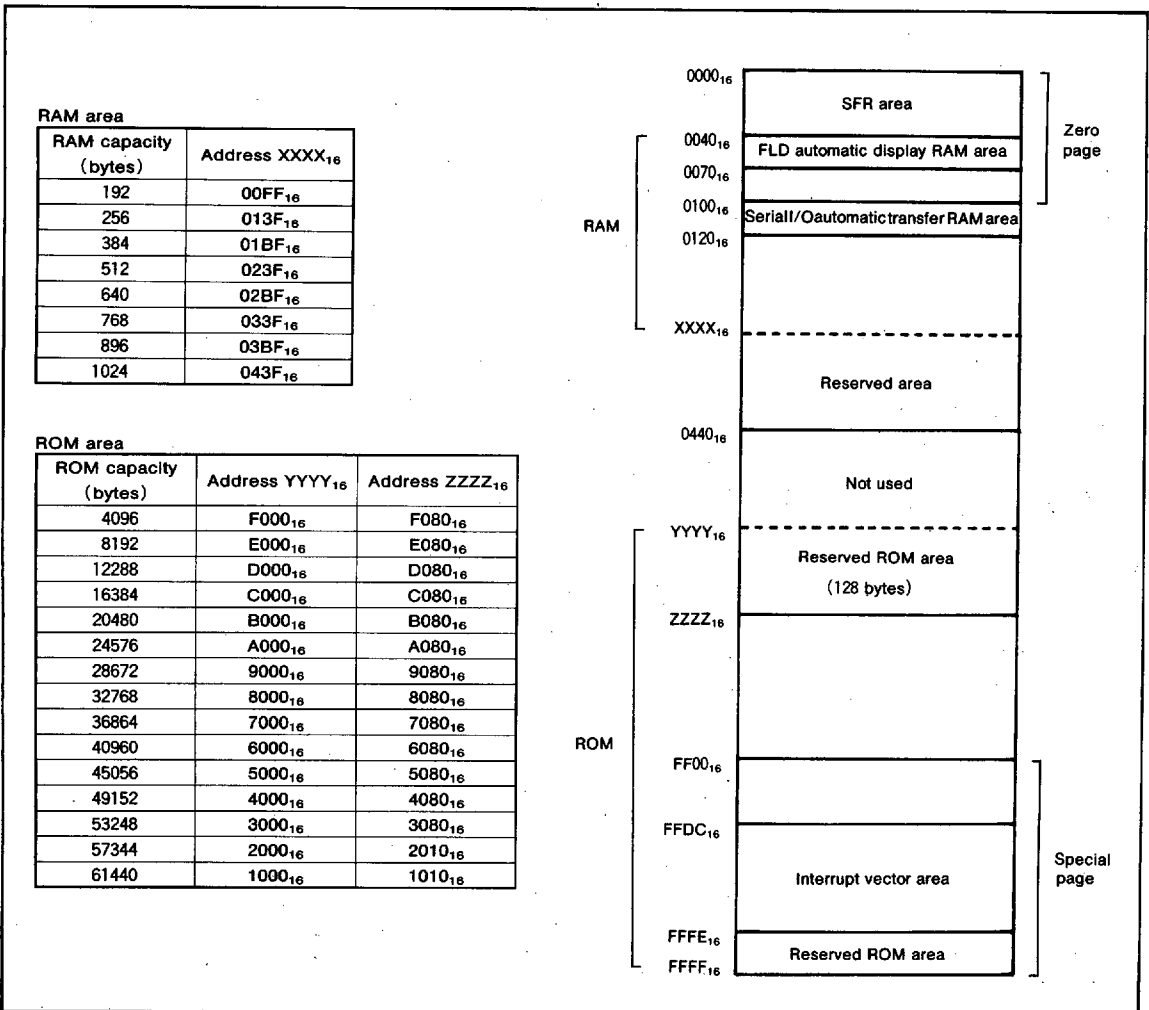


Fig. 2 Memory map diagram

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0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆		0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	PWM control register (PWMCON)
000C ₁₆	Port P6 (P6)	002C ₁₆	PWM register (upper) (PWMH)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	PWM register (lower) (PWML)
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	A-D control register (ADCON)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	A-D conversion register (AD)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	Port P3 segment/digit switching register (P3SDR)
0013 ₁₆	Port P9 direction register (P9D)	0033 ₁₆	Port P0 digit/port switching register (P0DPR)
0014 ₁₆	Port PA (PA)	0034 ₁₆	Port P8 segment/port switching register (P8SPR)
0015 ₁₆	Port PA direction register (PAD)	0035 ₁₆	Key-scan blanking register (KSCN)
0016 ₁₆	Port PB (PB)	0036 ₁₆	FLDC mode register (FLDM)
0017 ₁₆		0037 ₁₆	FLD data pointer (FLDDP)
0018 ₁₆	Serial I/O automatic transfer data pointer (SIODP)	0038 ₁₆	High-breakdown-voltage port control register (HVPC)
0019 ₁₆	Serial I/O1 control register (SIO1CON)	0039 ₁₆	
001A ₁₆	Serial I/O automatic transfer control register (SIOAC)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register (SIO1)	003B ₁₆	CPU mode register (CUPM)
001C ₁₆	Serial I/O automatic transfer interval register (SIOAI)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 register (SIO2)	003F ₁₆	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The 3818 group has 67 programmable I/O pins arranged in nine I/O ports (ports P1, P2, P4₁-P4₇, P5-P8, P9₀-P9₃ and PA). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

The 3818 group has four ports with high-breakdown-voltage pins (ports P0, P3, P8, P9). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC} - 40V$. Each pin in Ports P0, P3, and P9 has an internal pull-down resistor connected to V_{EE} . Port P8 has no internal pull-down resistors, so that connect an external resistor to each port. At reset, the P-channel output transistor of each port latch is turned off, so it becomes V_{EE} level ("L") by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register (address 0038₁₆) slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

MITSUBISHI MICROCOMPUTERS

3818 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0 ₀ /SEG ₈ — P0 ₃ /DIG ₁₁	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(1)
P0 ₄ /SEG ₁₂ — P0 ₇ /SEG ₁₅					FLDC mode register Port P0 digit/port switching register High-breakdown-voltage port control register	(2)
P1 ₀ —P1 ₇	Port P1	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(3)
P2 ₀ —P2 ₇	Port P2	Input/output, individual bits	TTL level input CMOS 3-state output			(3)
P3 ₀ /SEG ₁₆ / DIG ₁₆ —P3 ₇ / SEG ₂₃ /DIG ₇	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Port P3 segment/digit switching register High-breakdown-voltage port control register	(4)
P4 ₀ /INT ₀	Port P4	Input	CMOS compatible input level	External interrupt input	Interrupt edge selection register	(5)
P4 ₁ /INT ₁ — P4 ₄ /INT ₄		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	Interrupt edge selection register	(6)
P4 ₅						(3)
P4 ₆ /T1 _{OUT} , P4 ₇ /T3 _{OUT}				Timer output	Timer 12 mode register Timer 34 mode register	(7)
P5 ₀ /S _{IN1} , P5 ₁ /S _{OUT1} , P5 ₂ /S _{CLK1} , P5 ₃ /S _{RDY1} / CS/S _{CLK12}	Port P5	Input/output, individual bits	CMOS compatible input level N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(8)
P5 ₄ /S _{IN2} , P5 ₅ /S _{OUT2} , P5 ₆ /S _{CLK2} , P5 ₇ /S _{RDY2}						(9)
				Serial I/O2 function I/O	Serial I/O2 control register	(10)
						(10)
P6 ₀ /PWM ₀	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	14-bit PWM output	PWM control register	(11)
P6 ₁ /PWM ₁				8-bit PWM output	Timer 56 mode register Timer 6 PWM register	(7)
P6 ₂ /CNTR ₀ , P6 ₃ /CNTR ₁				Timer 2, Timer 4 input	Interrupt edge selection register	(6)
P6 ₄ —P6 ₇						(3)
P7 ₀ /AN ₀ — P7 ₇ /AN ₇	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	A-D control register	(12)
P8 ₀ /SEG ₀ — P8 ₇ /SEG ₇	Port P8	Input/output, individual bits	CMOS compatible input level High-breakdown-voltage P-channel open-drain output without pull-down resistor	FLD automatic display function	FLDC mode register Port P8 segment/port switching register High-breakdown-voltage port control register	(13)

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P9 ₀ /SEG ₈ — P9 ₃ /SEG ₁₁	Port P9	Input/output, individual bits	CMOS compatible input level High-breakdown- voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown- voltage port control register	(14)
P9 ₄ /SEG ₁₂ — P9 ₇ /SEG ₁₅		Output	High-breakdown- voltage P-channel open-drain output, with pull-down resistor			(15)
PA ₀ —PA ₇	Port PA	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(3)
PB ₀ , PB ₁	Port PB	Input	CMOS compatible input level			(16)

- Note 1. For details of how to use double-function ports as function I/O ports, refer to the applicable sections.
 2. Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction.
 When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

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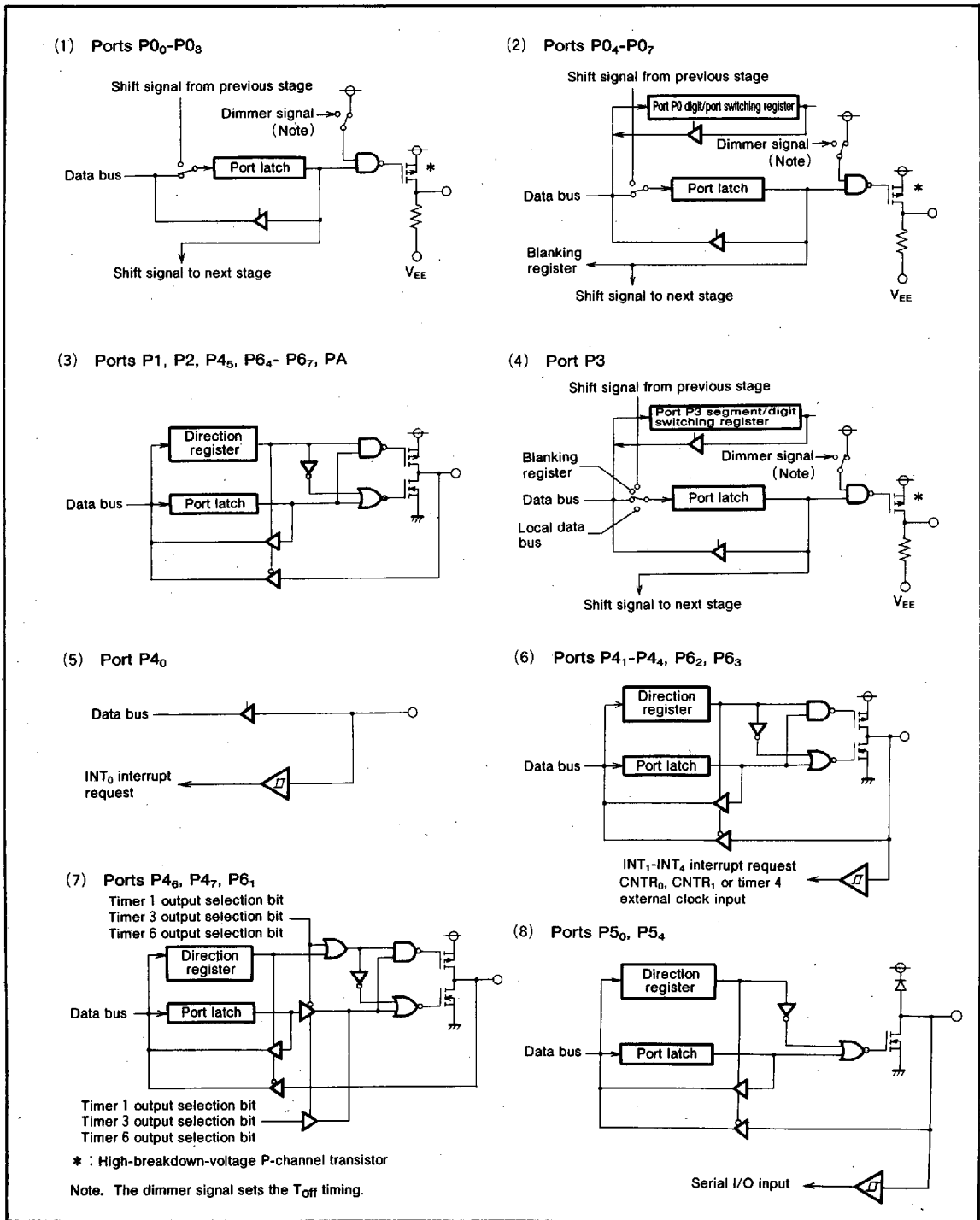


Fig. 4 Port block diagram (1)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

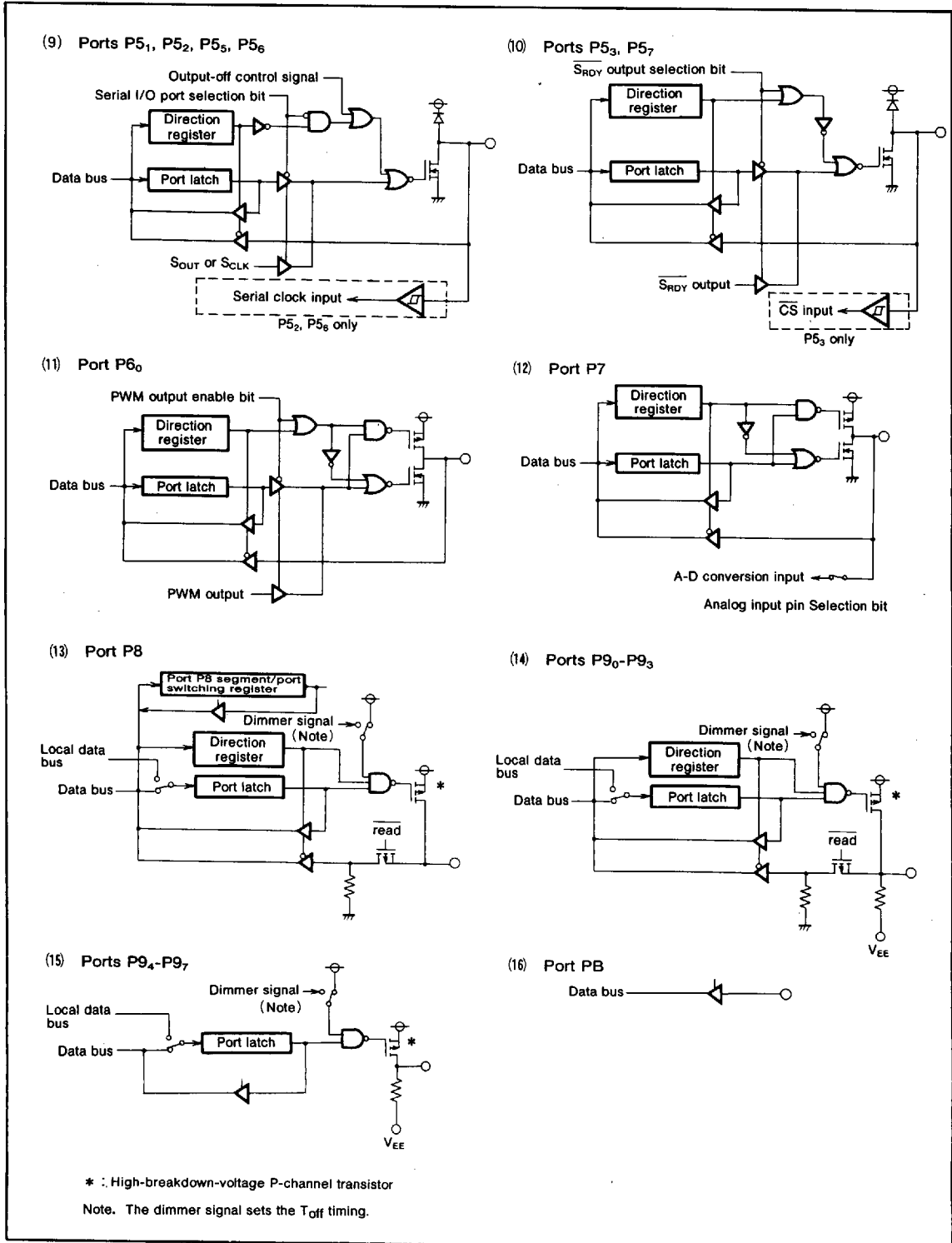


Fig. 5 Port block diagram (2)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPTS

Interrupts occur by eighteen sources: five external, twelve internal, and one software.

Interrupt Control

Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT_0 — INT_4) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge selection.
- (3) Clear the interrupt request bit which is selected to "0".
- (4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
INT ₂	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
Serial I/O1	5	FFF5 ₁₆	FFF4 ₁₆	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of final data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3 ₁₆	FFF2 ₁₆	At completion of data transfer	
Timer 1	7	FFF1 ₁₆	FFF0 ₁₆	At timer 1 underflow	
Timer 2	8	FFEF ₁₆	FFEE ₁₆	At timer 2 underflow	STP release timer underflow
Timer 3	9	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
Timer 4	10	FFEB ₁₆	FFEA ₁₆	At timer 4 underflow	
Timer 5	11	FFE9 ₁₆	FFE8 ₁₆	At timer 5 underflow	
Timer 6	12	FFE7 ₁₆	FFE6 ₁₆	At timer 6 underflow	
INT ₃	13	FFE5 ₁₆	FFE4 ₁₆	At detection of either rising or falling edge of INT ₃ input	External interrupt (active edge selectable)
INT ₄	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of INT ₄ input	External interrupt valid when INT ₄ interrupt is selected (active edge selectable)
A-D converter				At completion of A-D conversion	Valid when A-D interrupt is selected
FLD blanking	15	FFE1 ₁₆	FFE0 ₁₆	At falling of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rising of each digit	Valid when FLD digit interrupt is selected
BRK instruction	16	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses.

2. Reset function in the same way as an interrupt with the highest priority.

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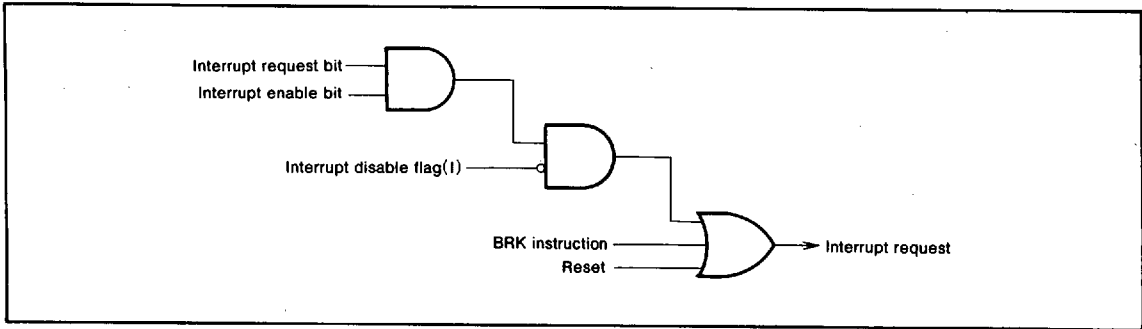


Fig. 6 Interrupt control

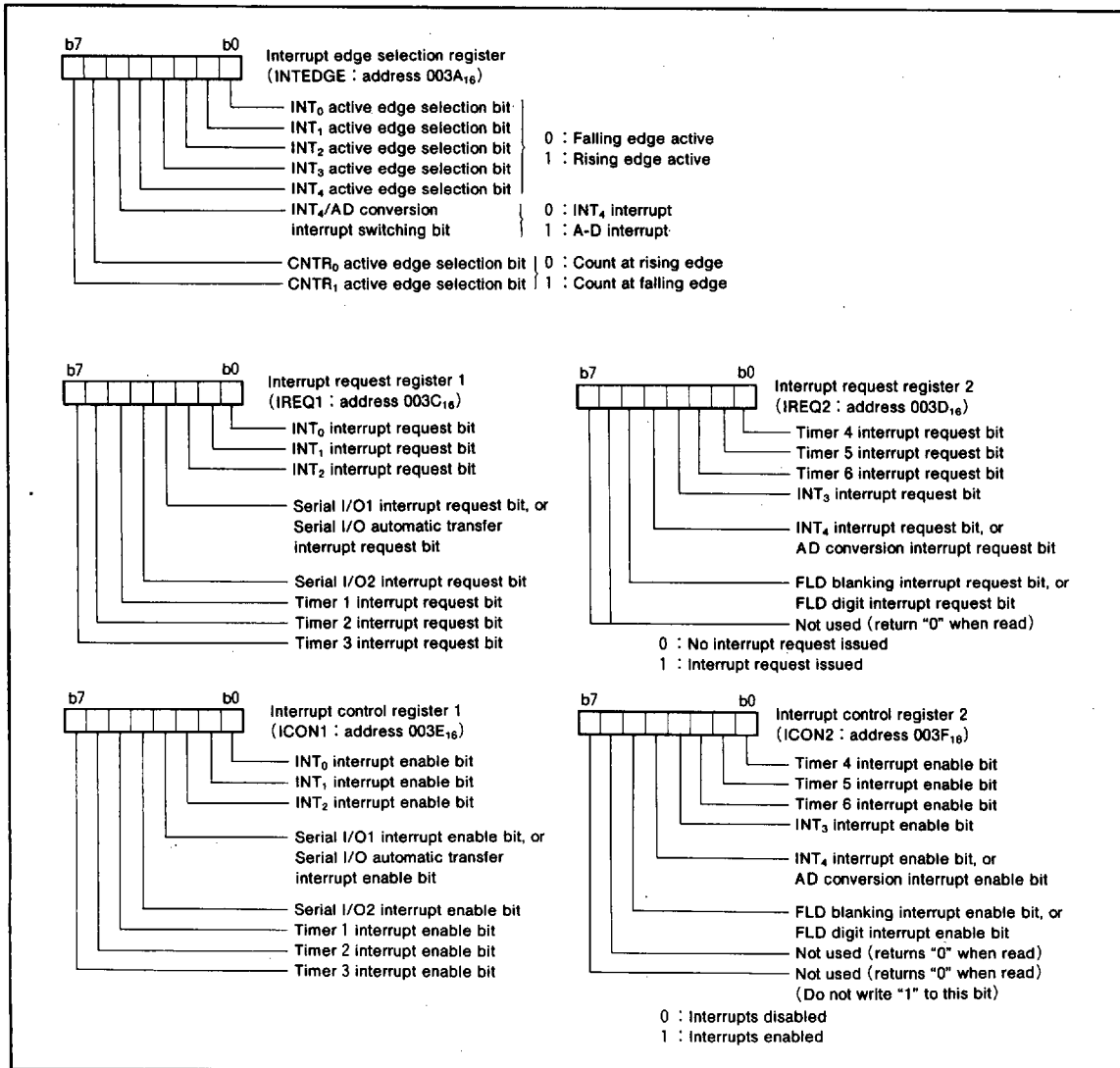


Fig. 7 Structure of Interrupt-related registers

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMERS

The 3818 group has six built-in timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are count down. When the timer reaches "00₁₆", at the next count pulse the contents of the corresponding timer latch is loaded into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".

Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

Timer 1 can also output a rectangular waveform from the P4₆/T1_{OUT} pin. The waveform changes polarity each time timer 1 overflows.

The active edge of the external signal CNTR₀ can be set by the interrupt edge selection register.

When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to "FF₁₆", and timer 2 is set to "01₁₆".

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

Timer 3 can also output a rectangular waveform from the P4₇/T3_{OUT} pin. The waveform changes polarity each time timer 3 overflows.

The active edge of the external signal CNTR₁ can be set by the interrupt edge selection register.

Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

Timer 6 can also output a rectangular waveform from the P6₁/PWM₁ pin. The waveform changes polarity each time timer 6 overflows.

Timer 6 PWM₁ Mode

Timer 6 can also output a rectangular waveform of n cycles high and m cycles low. The n is the value set in timer latch 6 (address 0025₁₆) and m is the value in the timer 6 PWM register (address 0027₁₆). If n is "0", the PWM₁ output is "L", if m is "0" and n is not "0", then the PWM₁ output is "H". In PWM mode, interrupts are generated at the rising edge of the PWM₁ output.

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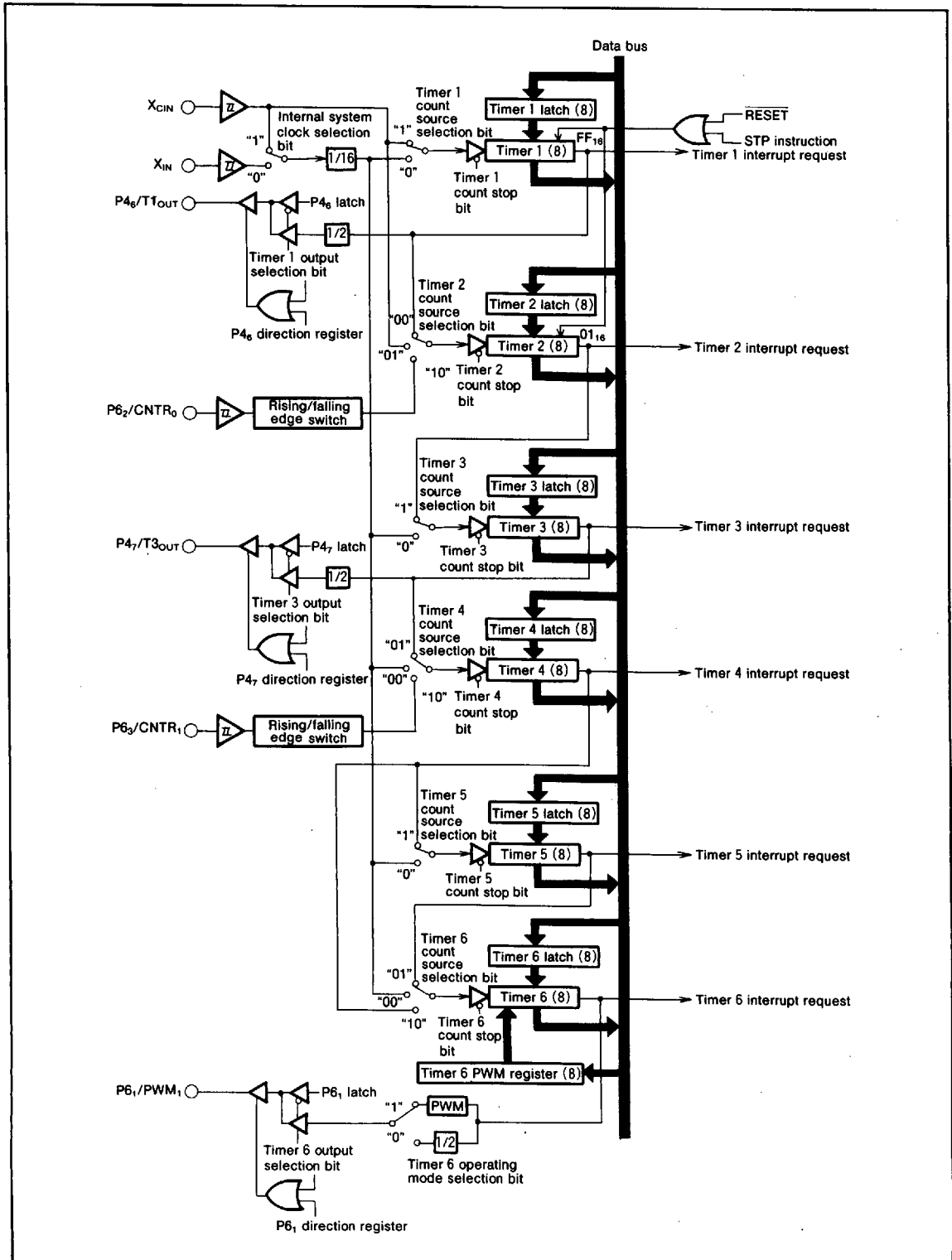


Fig. 8 Timer block diagram

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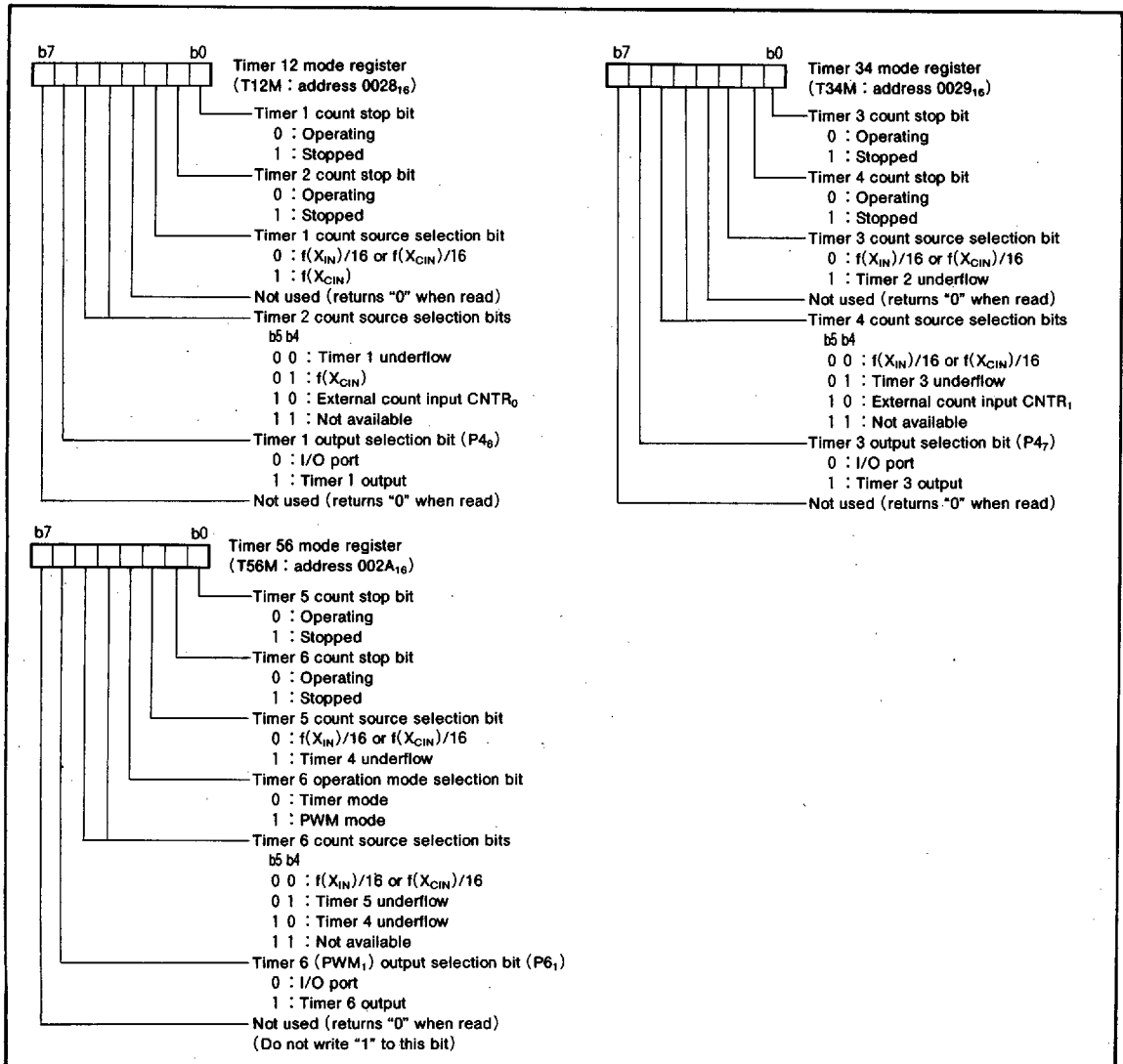


Fig. 9 Structure of timer-related registers

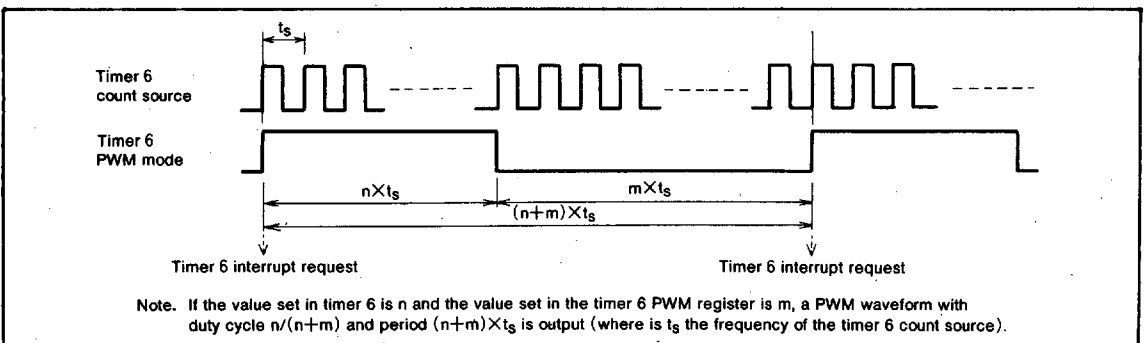


Fig. 10 Timing in timer 6 PWM₁ mode

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SERIAL I/O

The 3818 group has two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has a built-in automatic transfer function. Normal serial operation can be set via the serial I/O automatic transfer control register (address 001A₁₆).

Serial I/O2 can only be used in normal operation mode.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019₁₆ and 001D₁₆).

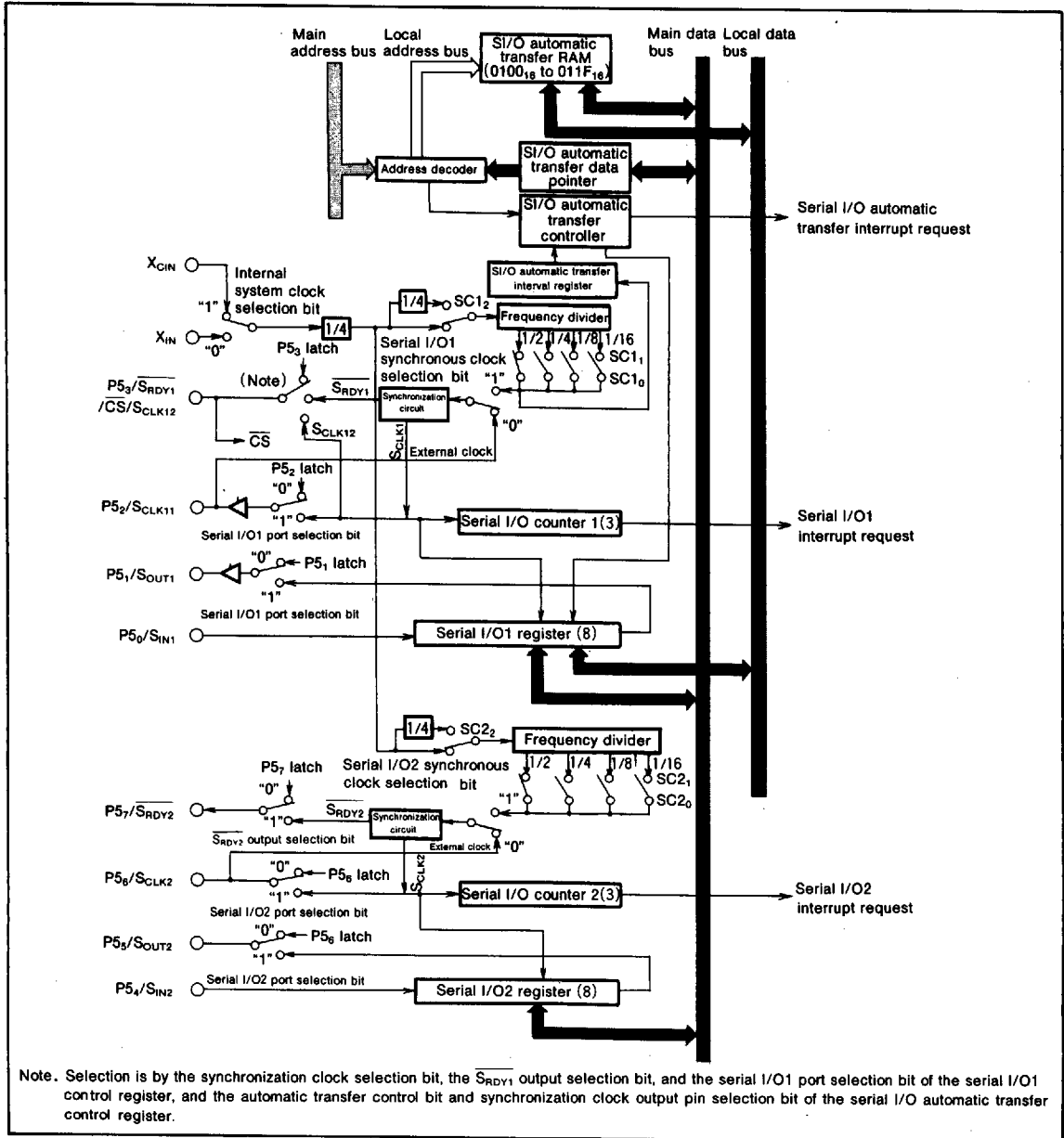


Fig. 11 Serial I/O block diagram

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Serial I/O Control Registers

(SIO1CON, SIO2CON) 0019₁₆, 001D₁₆

Each of the serial I/O control registers (addresses 0019₁₆ and 001D₁₆) contains seven bits that select various control parameters of the serial I/O function.

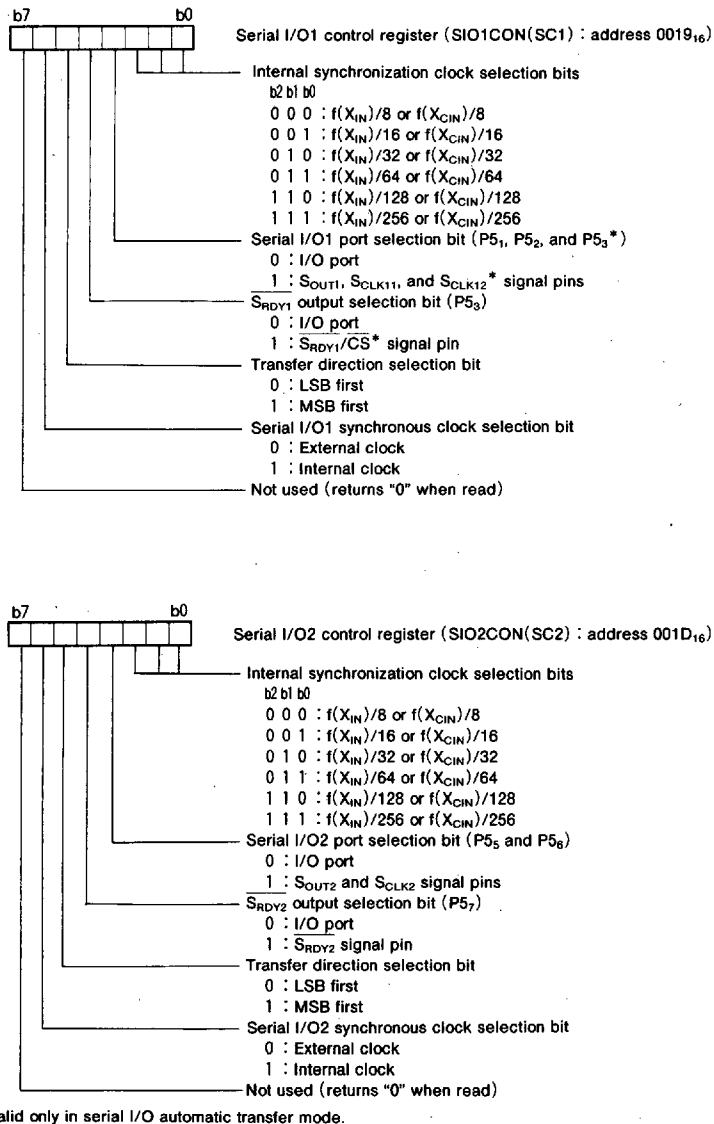


Fig. 12 Structure of serial I/O control registers

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Serial I/O ordinary Mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, for selecting of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address 001B₁₆ or 001F₁₆). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift during inputting the transfer clock is. In this case, note that the S_{OUT} pin does not go to high impedance state at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.

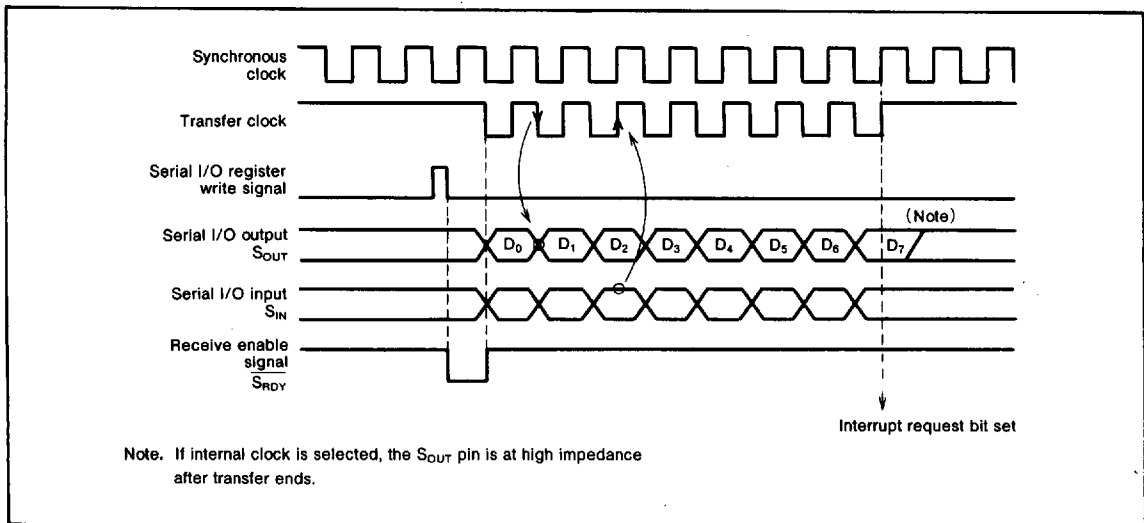


Fig. 13 Serial I/O timing in normal mode (for LSB first)

Serial I/O Automatic Transfer Mode

The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address 001A₁₆).

The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019₁₆) in the same way as for the serial I/O ordinary mode. However, note that when external clock is selected and bit 4 (the S_{RDY1} output selection bit) of the serial I/O1 control register is set to "1", port P5₃ becomes the CS input pin by setting.

Serial I/O Automatic Transfer Control Register (SIOAC) 001A₁₆

The serial I/O automatic transfer control register (address 001A₁₆) contains four bits that select various control parameters for automatic transfer.

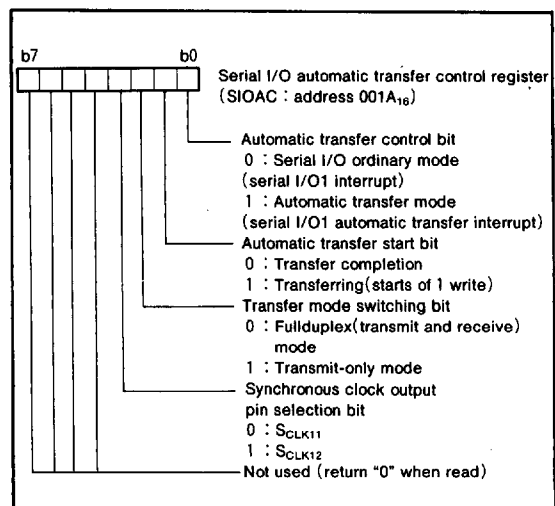


Fig. 14 Structure of serial I/O automatic transfer control register

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Serial I/O Automatic Transfer Data Pointer (SIODP) 0018₁₆

The serial I/O automatic transfer data pointer (address 0018₁₆) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100₁₆).

Set the serial I/O automatic transfer data pointer to (the number of transfer data-1), to specify the storage position of the start of data.

Serial I/O Automatic Transfer RAM

The serial I/O automatic transfer RAM is the 32 bytes from address 0100₁₆ to address 011F₁₆.

Setting of Serial I/O Automatic Transfer Data

When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100₁₆.

Serial I/O Automatic Transfer Interval Register (SIOAI) 001C₁₆

The serial I/O automatic transfer interval register (address 001C₁₆) consists of a 5-bit counter that determines the transfer interval T_i during automatic transfer.

If a value n is written to the serial I/O automatic transfer interval register, a value of $T_i = (n + 2) \times T_c$ is generated, where T_c is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

Address	BR	7	6	5	4	3	2	1	0
0100 ₁₆									
0101 ₁₆									
0102 ₁₆									
⋮									
011D ₁₆									
011E ₁₆									
011F ₁₆									

Fig. 15 Bit allocation of serial I/O automatic transfer RAM

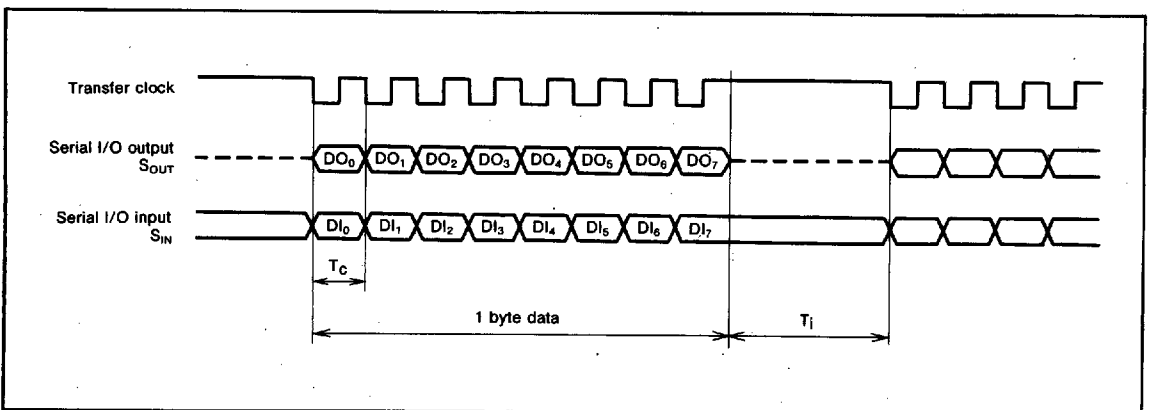


Fig. 16 Serial I/O automatic transfer interval timing

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Setting of Serial I/O Automatic Transfer Timing

Use the serial I/O control register (address 0019₁₆) and the serial I/O automatic transfer interval register (address 001C₁₆) to set the timing of serial I/O automatic transfer. The serial I/O control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval. This setting of transfer interval is valid only when internal clock is selected as the clock source.

Start of Serial I/O Automatic Transfer

Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address 001A₁₆), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to complete automatic transfer.

Operation in Serial I/O Automatic Transfer Modes

There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

Operation in FullDuplex Mode

In fullduplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.

The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted. If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.

Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00₁₆". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

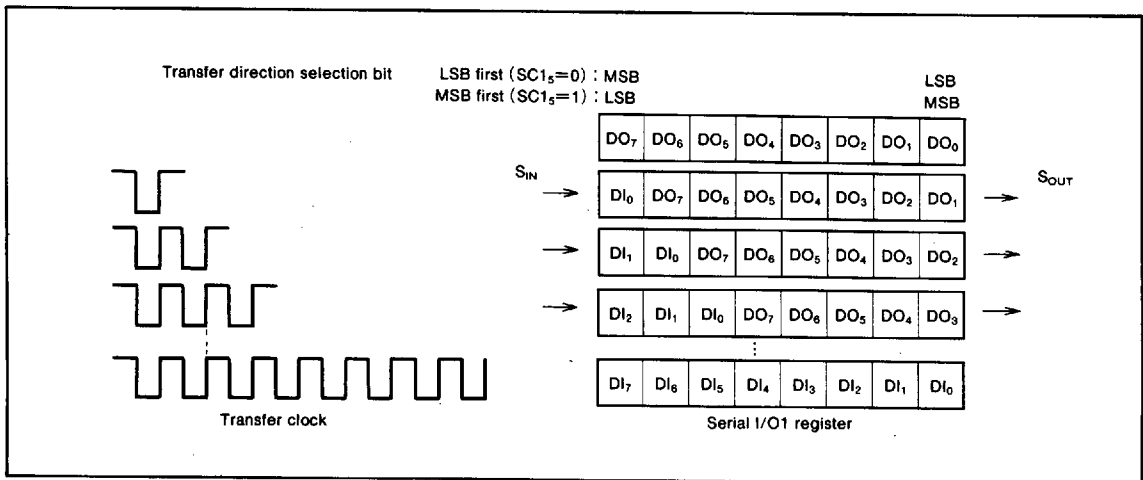


Fig. 17 Serial I/O1 register in fullduplex mode

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If Internal Clock is Selected

If internal clock is selected, the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin can be used as the $\overline{S_{RDY1}}$ pin by setting the $SC1_4$ bit to "1". If internal clock is selected, the $P5_3$ pin can be used as the synchronization clock output pin S_{CLK12} by setting the $SIOAC_3$ bit to "1". In this case, the S_{CLK11} pin is at high impedance.

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ and $P5_2/S_{CLK11}$ pins by setting bit 3 ($SC1_3$), bit 4 ($SC1_4$), and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019₁₆) and bit 3 ($SIOAC_3$) of the serial I/O automatic transfer control register (address 001A₁₆). (Refer to Table 2.)

If using the S_{CLK11} and S_{CLK12} pins for switching, set the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin to $P5_3$ by setting the $SC1_4$ bit to "0", and set the $P5_3$ direction register to input mode. Make sure that the $SIOAC_3$ bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2. S_{CLK11} and S_{CLK12} selection

$SC1_6$	$SC1_4$	$SC3_3$	$SIOAC_3$	$P5_2/S_{CLK11}$	$P5_3/S_{CLK12}$
1	0	1	0	S_{CLK11}	$P5_3$
			1	High impedance	S_{CLK12}

Note. $SC1_3$: Serial I/O1 port selection bit
 $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
 $SC1_6$: Synchronization clock selection bit
 $SIOAC_3$: Synchronization clock output pin selection bit

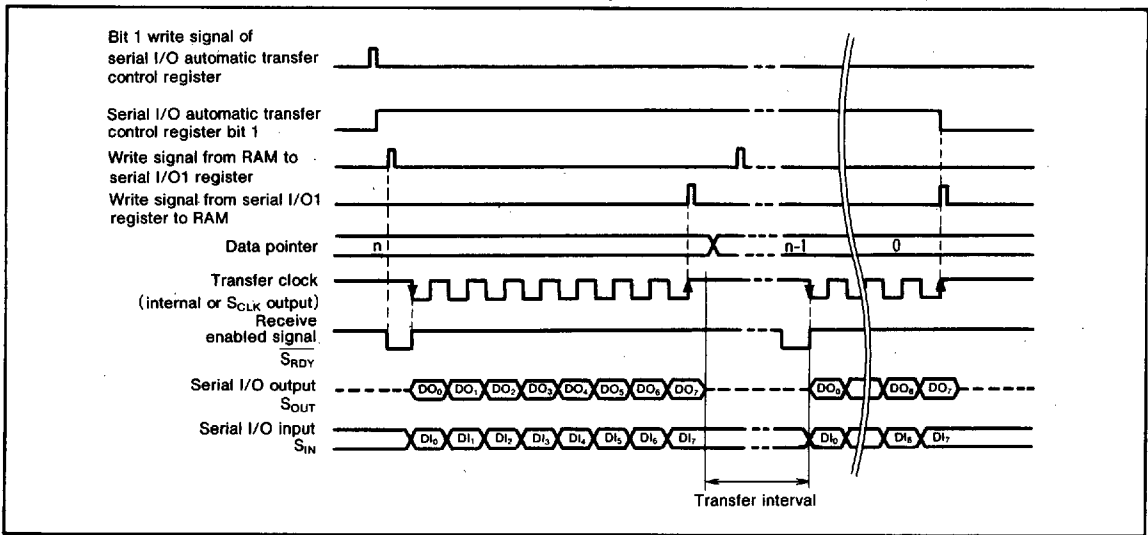


Fig. 18 Timing during serial I/O automatic transfer (Internal clock selected, $\overline{S_{RDY}}$ used)

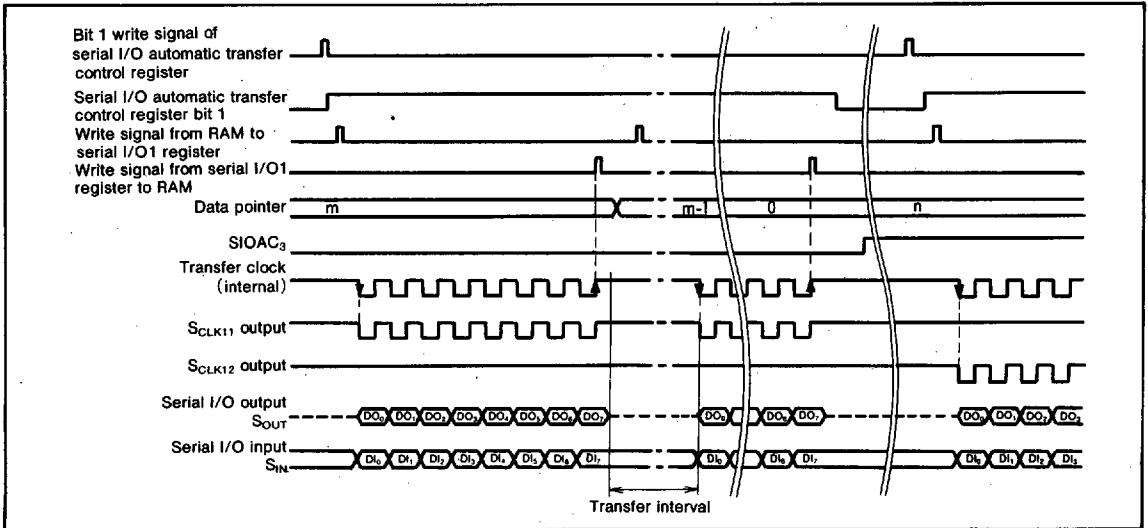


Fig. 19 Timing during serial I/O automatic transfer (internal clock selected, S_{CLK11} and S_{CLK12} used)

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If External Clock is Selected

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin S_{OUT} and the internal transfer clock can be controlled from the outside by setting the $\overline{S_{RDY1}}$ and $\overline{CS}$ (input) pins.

When the $\overline{CS}$ input is "L", the S_{OUT} pin and the internal transfer clock are enabled. When the $\overline{CS}$ input is "H", the S_{OUT} pin is at high impedance and the internal transfer clock is at "H".

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin by setting bit 4 ($SC1_4$) and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_h) and bit 0 ($SIOAC_0$) of the serial I/O automatic transfer control register (address 001A_h).

Make sure that the $\overline{CS}$ pin switches from "L" to "H" or from "H" to "L" while the transfer clock (S_{CLK} input) is "H" after one byte of data has been transferred.

If external clock is selected, make sure that the external clock goes "L" after at least 9 cycles of the internal system clock ϕ after the start bit is set. Leave at least 11 cycles of the system clock ϕ free for the transfer interval after one byte of data has been transferred.

If $\overline{CS}$ input is not being used, note that the S_{OUT} pin will not go high impedance, even after transfer is completed.

If $\overline{CS}$ input is not being used, or if $\overline{CS}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

Table 3. $P5_3/\overline{S_{RDY1}}/\overline{CS}$ selection

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note. $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
 $SC1_6$: Synchronization clock selection bit
 $SIOAC_0$: Automatic transfer control bit

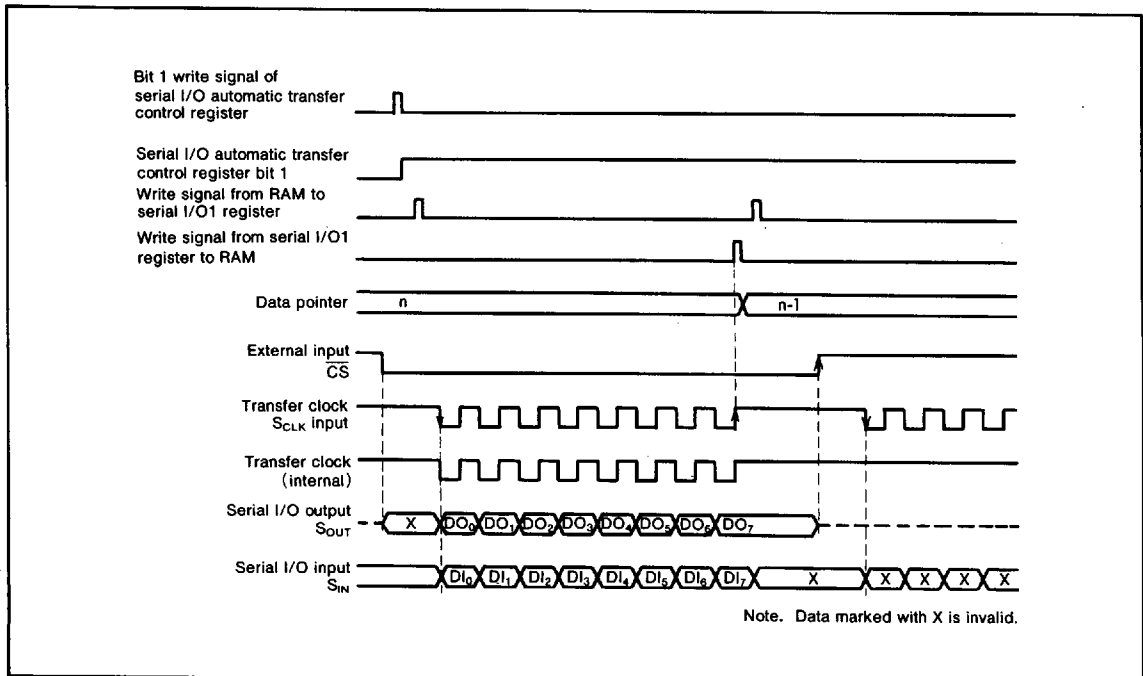


Fig. 20 Timing during serial I/O automatic transfer (external clock selected)

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PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

The 3818 group has a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 8MHz, the minimum resolution bit width is 250ns and the cycle period is 4096 μ s. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes $f(X_{IN})=8\text{MHz}$.

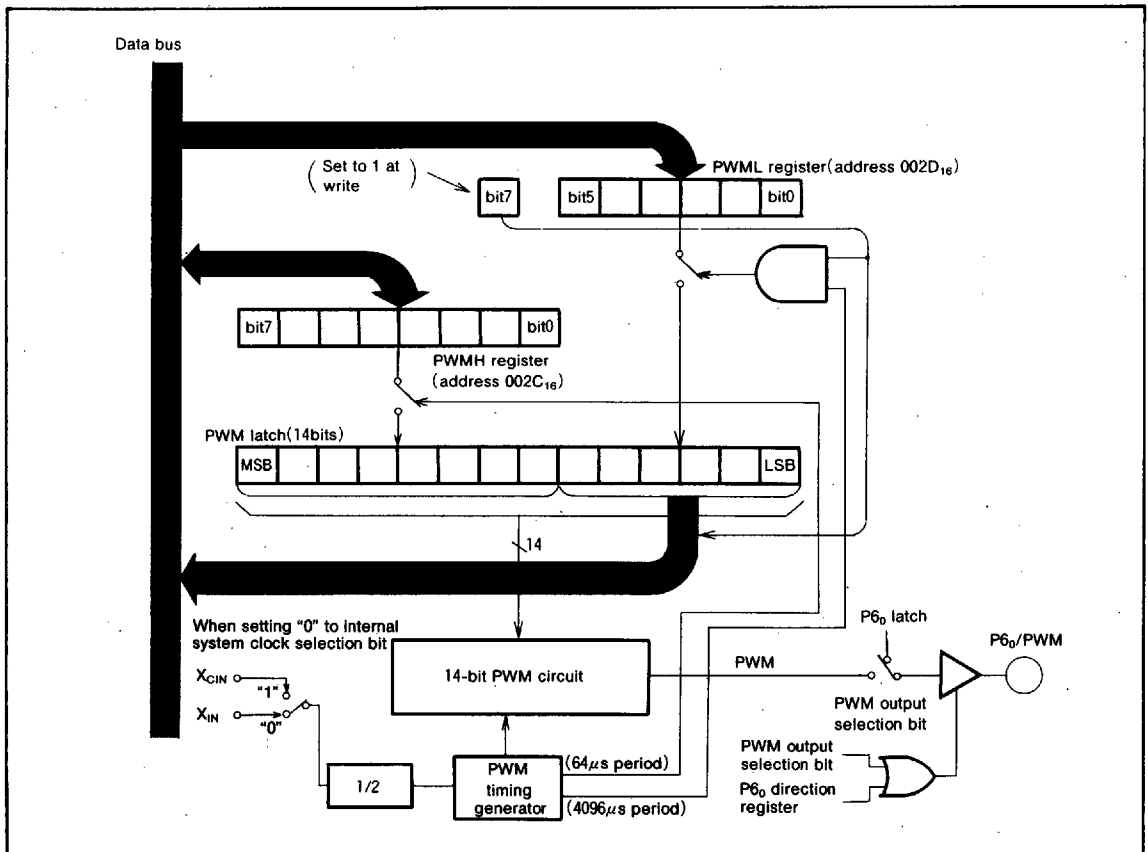


Fig. 21 PWM block diagram

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Data Set-up

The PWM output pin also functions as port P6₀. Set port P6₀ to be the PWM output pin by setting bit 0 of the PWM mode register (address 002B₁₆). The high-order eight bits of output data are set in the high-order PWM register PWMH (address 002C₁₆) and the low-order six bits are set in the low-order PWM register PWML (address 002D₁₆).

Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 4096 μ s), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 64 μ s). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 4. Relationship between lower 6 bits of data and period set by the ADD bit

Lower 6 Bits of Data (PWML)	Sub-periods t_m Lengthened ($m=0$ to 63)
0 0 0 0 0 0	None
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

PWM Operation

The timing of the 14-bit PWM function is shown in Fig. 24. The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is $256 \times \tau$ (64 μ s) long. The signal is "H" for a length equal to N times τ , where τ is the minimum resolution (250ns).

The contents of the low-order six bits of data enable the lengthening of the high signal by τ (250ns). As shown in Fig. 21, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 24, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the high-order eight bits of the 14-bit data are 03₁₆ and the low-order six bits are 05₁₆, the length of the "H"-level output in sub-periods $t_8, t_{24}, t_{32}, t_{40},$ and t_{56} is 4 τ , and its length 3τ in all other sub-periods.

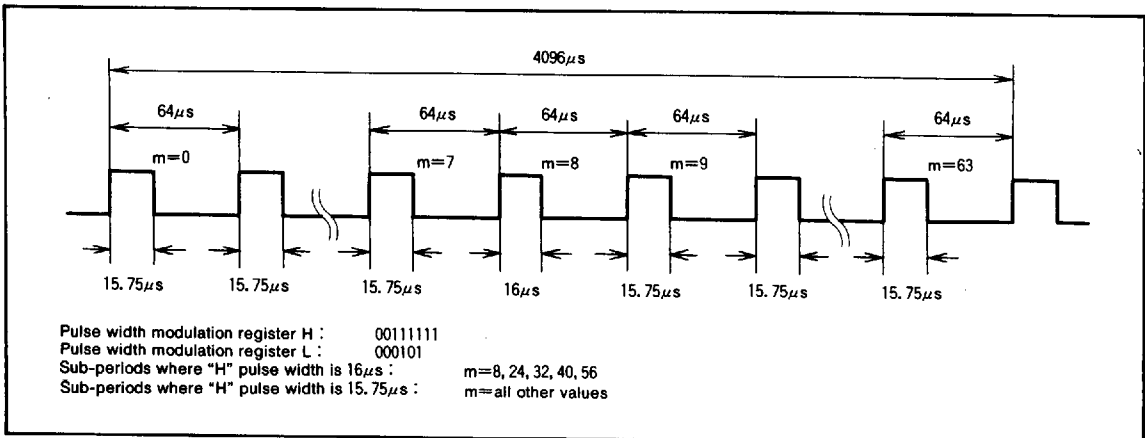


Fig. 22 PWM timing

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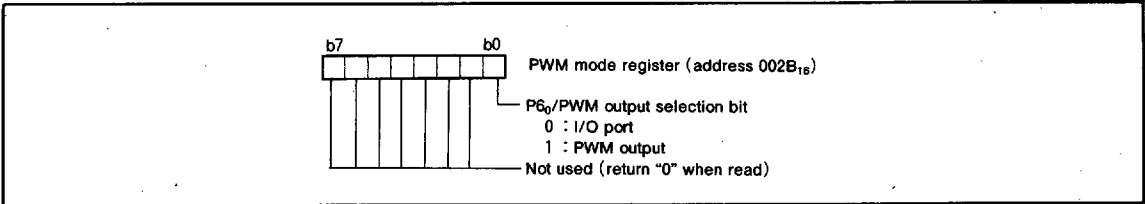


Fig. 23 Structure of PWM mode register

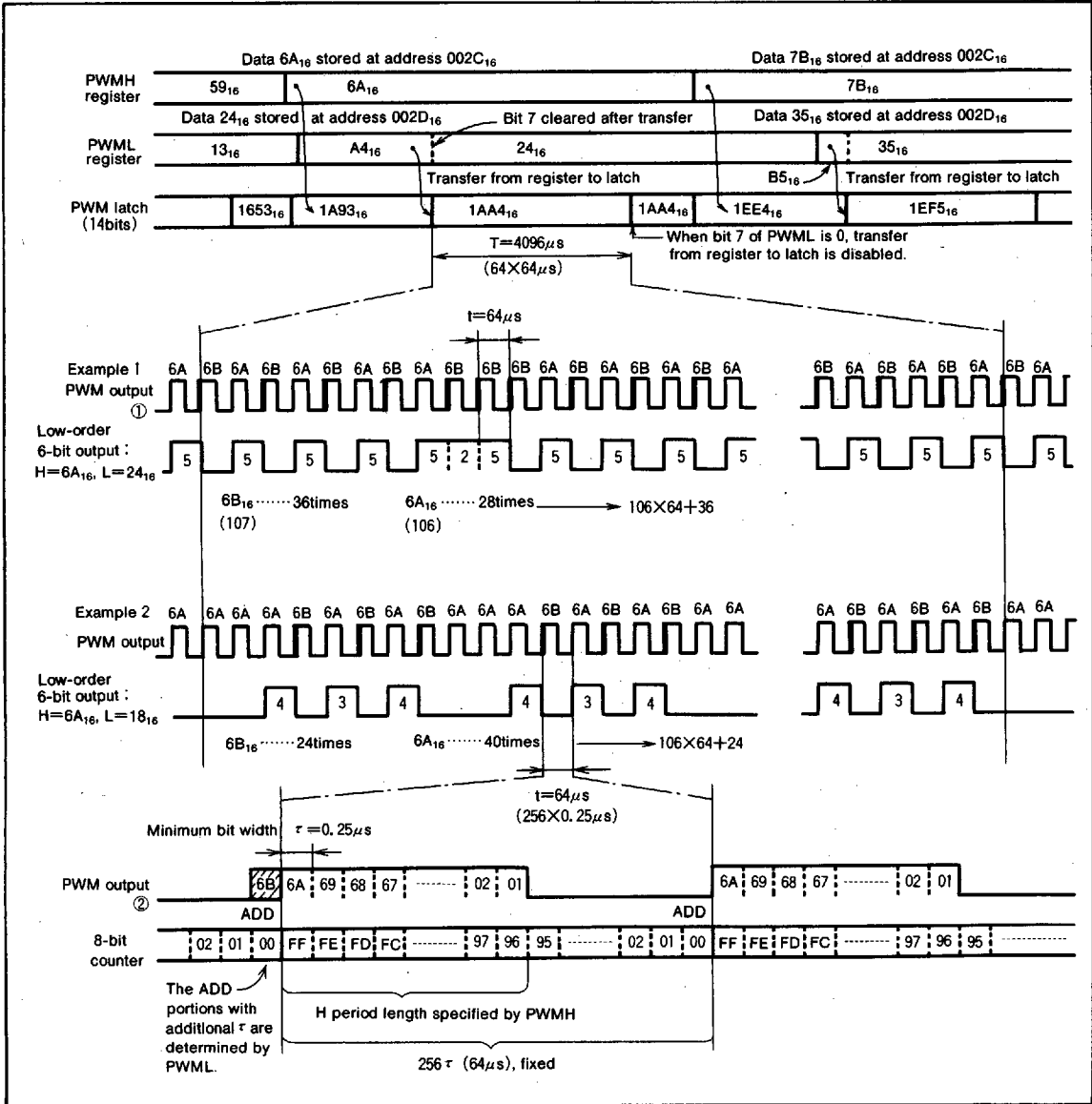


Fig. 24 14-bit PWM timing

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A-D CONVERTER

The functional blocks of the A-D converter are described below.

A-D Conversion Register (AD) 0031₁₆

The A-D conversion register is a read-only register that contains the result of an A-D conversion. This register should not be read during an A-D conversion.

A-D Control Register (ADCON) 0030₁₆

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports $P7_7/AN_7$ to $P7_0/AN_0$.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 500kHz during A-D conversion.

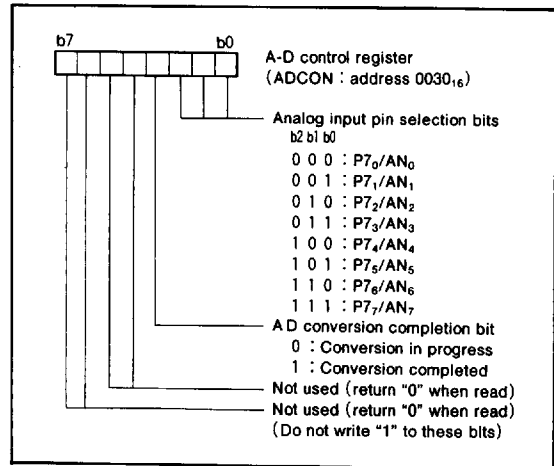


Fig. 25 Structure of A-D control register

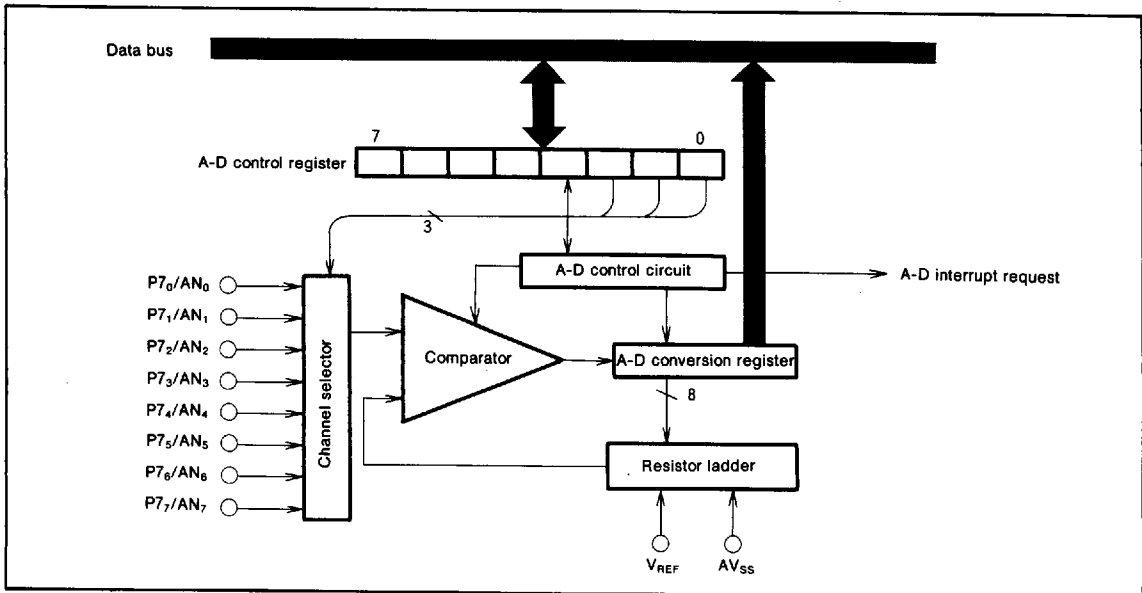


Fig. 26 A-D converter block diagram

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FLD CONTROLLER

The 3818 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 24 pins for segments
- 16 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Port P3 segment/digit switching register

- Port P0 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- 48-byte FLD automatic display RAM

Eight to twenty-four pins can be used as segment pins and four to sixteen pins can be used as digit pins.

Note that only 32 pins (maximum) can be used as segment and digit pins.

In the FLD automatic display mode ports P₁₀ to P₁₃ function as digit pins DIG₈ to DIG₁₁ automatically.

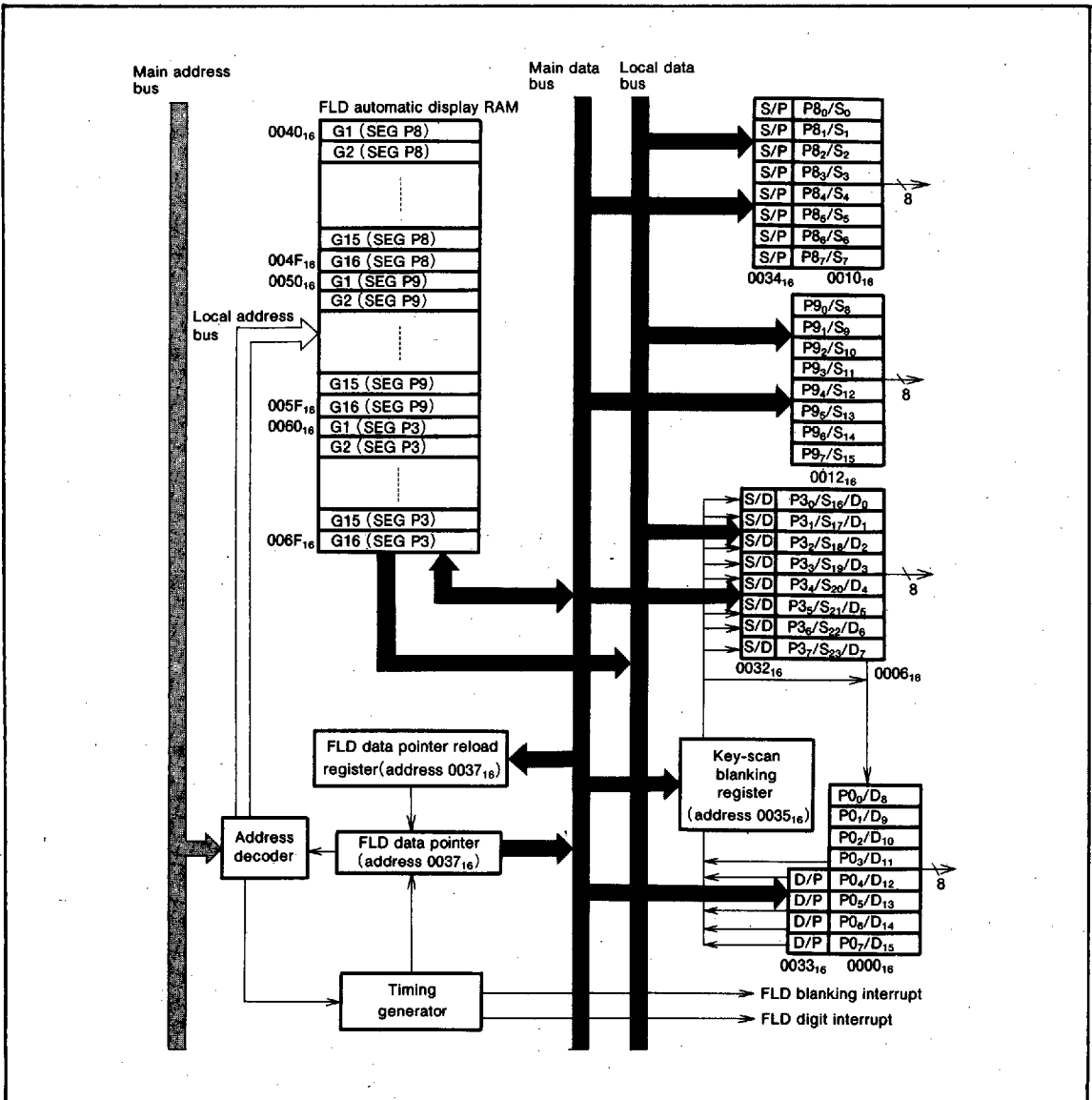


Fig. 27 FLD control circuit block diagram

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FLDC Mode Register (FLDM) 0036₁₆

The FLDC mode register (address 0036₁₆) is a seven bit control register which is used to control the FLD automatic display.

Key-scan Blanking Register (KSCN) 0035₁₆

The key-scan blanking register (address 0035₁₆) is a two bit register which sets the blanking period T_{scan} between the last digit and the first digit of the next cycle.

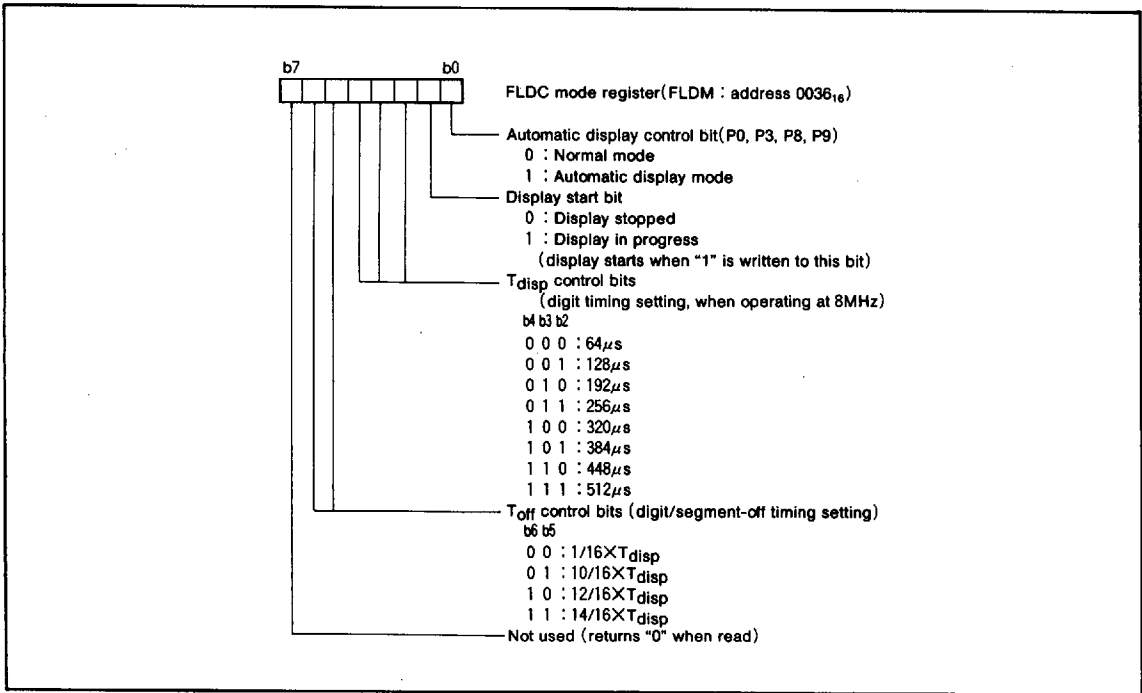


Fig. 28 Structure of FLDC mode register (FLDM)

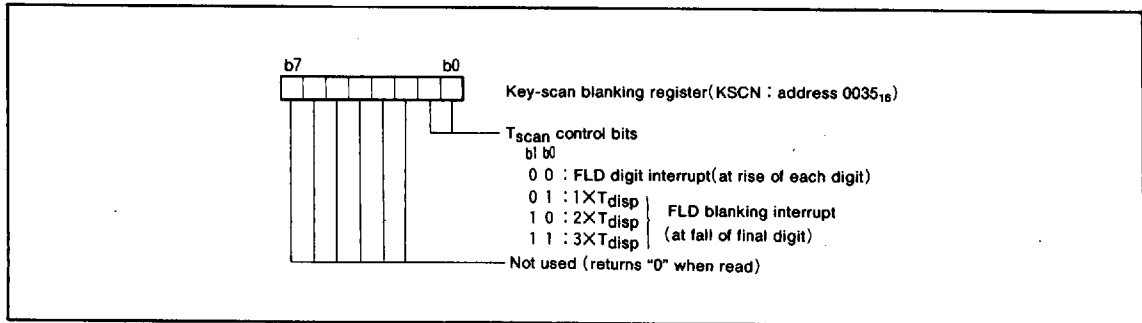


Fig. 29 Structure of key-scan blanking register (KSCN)

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FLD Automatic Display Pins

The FLD automatic display function of Ports P3, P0, P9, and P8 is selected by setting the automatic display control bit of

the FLDC mode register (address 0036₁₆) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 5. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
P8 ₀ -P8 ₇	SEG ₀ -SEG ₇ or P8 ₀ -P8 ₇	The individual bits of the Port P8 segment/port switching register (address 0034 ₁₆) can be used to set each pin to either segment ("1") or normal port input ("0").
P9 ₀ -P9 ₇	SEG ₈ -SEG ₁₅	None (segment only)
P3 ₀ -P3 ₇	SEG ₁₆ -SEG ₂₃ or DIG ₀ -DIG ₇	The individual bits of the Port P3 segment/digit switching register (address 0032 ₁₆) can be used to set each pin to segment ("1") or digit ("0"). (Note)
P0 ₀ -P0 ₃	DIG ₈ -DIG ₁₁	None (digit only, use all bits always)
P0 ₄ -P0 ₇	DIG ₁₂ -DIG ₁₅ or P0 ₄ -P0 ₇	The individual bits of the Port P0 digit/port switching register (address 0033 ₁₆) can be used to set each pin to digit ("1") or normal port output ("0"). (Note)

Note. Always set digits in sequence.

Number of segments Number of digits	16 4	8 12	16 10	24 8	16 16
Port P8 (has Port P8 segment/ port switching register)	0 P8₀ 0 P8₁ 0 P8₂ 0 P8₃ 0 P8₄ 0 P8₅ 0 P8₆ 0 P8₇	0 P8₀ 0 P8₁ 0 P8₂ 0 P8₃ 0 P8₄ 0 P8₅ 0 P8₆ 0 P8₇	0 P8₀ 0 P8₁ 0 P8₂ 0 P8₃ 1 SEG₄ 1 SEG₅ 1 SEG₆ 1 SEG₇	1 SEG₀ 1 SEG₁ 1 SEG₂ 1 SEG₃ 1 SEG₄ 1 SEG₅ 1 SEG₆ 1 SEG₇	1 SEG₀ 1 SEG₁ 1 SEG₂ 1 SEG₃ 1 SEG₄ 1 SEG₅ 1 SEG₆ 1 SEG₇
Port P9 (segment only)	SEG₈ SEG₉ SEG₁₀ SEG₁₁ SEG₁₂ SEG₁₃ SEG₁₄ SEG₁₅	SEG₈ SEG₉ SEG₁₀ SEG₁₁ SEG₁₂ SEG₁₃ SEG₁₄ SEG₁₅	SEG₈ SEG₉ SEG₁₀ SEG₁₁ SEG₁₂ SEG₁₃ SEG₁₄ SEG₁₅	SEG₈ SEG₉ SEG₁₀ SEG₁₁ SEG₁₂ SEG₁₃ SEG₁₄ SEG₁₅	SEG₈ SEG₉ SEG₁₀ SEG₁₁ SEG₁₂ SEG₁₃ SEG₁₄ SEG₁₅
Port P3 (has Port P3 segment/ digit switching register)	1 SEG₁₆ 1 SEG₁₇ 1 SEG₁₈ 1 SEG₁₉ 1 SEG₂₀ 1 SEG₂₁ 1 SEG₂₂ 1 SEG₂₃	0 DIG₀ → G12 0 DIG₁ → G11 0 DIG₂ → G10 0 DIG₃ → G9 0 DIG₄ → G8 0 DIG₅ → G7 0 DIG₆ → G6 0 DIG₇ → G5	1 SEG₁₆ 1 SEG₁₇ 1 SEG₁₈ 1 SEG₁₉ 0 DIG₄ → G10 0 DIG₅ → G9 0 DIG₆ → G8 0 DIG₇ → G7	1 SEG₁₆ 1 SEG₁₇ 1 SEG₁₈ 1 SEG₁₉ 1 SEG₂₀ 1 SEG₂₁ 1 SEG₂₂ 1 SEG₂₃	0 DIG₀ → G16 0 DIG₁ → G15 0 DIG₂ → G14 0 DIG₃ → G13 0 DIG₄ → G12 0 DIG₅ → G11 0 DIG₆ → G10 0 DIG₇ → G9
Port P0 (has Port P0 digit/port switching register)	DIG₈ → G4 DIG₉ → G3 DIG₁₀ → G2 DIG₁₁ → G1 0 P0₄ 0 P0₅ 0 P0₆ 0 P0₇	DIG₈ → G4 DIG₉ → G3 DIG₁₀ → G2 DIG₁₁ → G1 0 P0₄ 0 P0₅ 0 P0₆ 0 P0₇	DIG₈ → G6 DIG₉ → G5 DIG₁₀ → G4 DIG₁₁ → G3 1 DIG₁₂ → G2 1 DIG₁₃ → G1 0 P0₆ 0 P0₇	DIG₈ → G8 DIG₉ → G7 DIG₁₀ → G6 DIG₁₁ → G5 1 DIG₁₂ → G4 1 DIG₁₃ → G3 1 DIG₁₄ → G2 1 DIG₁₅ → G1	DIG₈ → G8 DIG₉ → G7 DIG₁₀ → G6 DIG₁₁ → G5 1 DIG₁₂ → G4 1 DIG₁₃ → G3 1 DIG₁₄ → G2 1 DIG₁₅ → G1

Fig. 30 Segment/digit setting example

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FLD Automatic Display RAM

The FLD automatic display RAM area is the 48 bytes from addresses 0040_{16} to $006F_{16}$. The FLD automatic display RAM area can be used to store 3-byte data items for a maximum of 16 digits. Addresses 0040_{16} to $004F_{16}$ are used for P8 segment data, addresses 0050_{16} to $005F_{16}$ are used for P9 segment data, and addresses 0060_{16} to $006F_{16}$ are used for P3 segment data.

FLD Data Pointer and FLD Data Pointer Reload Register

The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P3.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0037_{16} and are 6-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer.

The actual memory address is the value of the data pointer plus 40_{16} , 50_{16} , or 60_{16} .

The contents of the FLD data pointer indicate the first address of segment P3 (the content of the FLD data pointer reload register) at the start of automatic display. The content of the FLD data pointer changes repeatedly as follows: when transferring the segment P3 data to the segment, the content decreases by -16 ; when transferring the segment P9 data to the segment, it decreases by -16 ; when transferring the segment P8 data to the segment, it increases by $+31$. After it reaches 00_{16} , the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, three bytes of data for the P3, P9, and P8 segments of one digit are transferred.

Address \ Bit	7	6	5	4	3	2	1	0	
0040_{16}	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← Final digit (final data of segment P8)
0041_{16}	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment P8 data area
$004E_{16}$	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
$004F_{16}$	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← Final digit (final data of segment P9)
0050_{16}	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0051_{16}	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	Segment P9 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
$005E_{16}$	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	← Final digit (final data of segment P3)
$005F_{16}$	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0060_{16}	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	Segment P3 data area
0061_{16}	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
$006E_{16}$	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
$006F_{16}$	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	

Fig. 31 FLD automatic display RAM and bit allocation

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Data Setup

When data is stored in the FLD automatic display RAM, the end of segment P8 data is stored at address 0040₁₆, the end of segment P9 data is stored at address 0050₁₆, and the end of segment P3 data is stored at address 0060₁₆. The head of each of the segment P8, P9, and P3 data is stored at an address that is the number of digits—1 away from the corresponding address 0040₁₆, 0050₁₆, 0060₁₆.

Set the value (the number of digits—1) to the low-order four bits of the FLD data pointer reload register. "1" is always written to bit 5, and "0" is always written to bit 4. Note that "0" is always read from bit 5 or 4 during a read.

For 17 segments and 15 digits
 (FLD data pointer reload register=14)

Address	Bit 7	6	5	4	3	2	1	0
0040 ₁₆								
0041 ₁₆								
0042 ₁₆								
0043 ₁₆								
0044 ₁₆								
0045 ₁₆								
0046 ₁₆								
0047 ₁₆								
0048 ₁₆								
0049 ₁₆								
004A ₁₆								
004B ₁₆								
004C ₁₆								
004D ₁₆								
004E ₁₆								
004F ₁₆								
0050 ₁₆								
0051 ₁₆								
0052 ₁₆								
0053 ₁₆								
0054 ₁₆								
0055 ₁₆								
0056 ₁₆								
0057 ₁₆								
0058 ₁₆								
0059 ₁₆								
005A ₁₆								
005B ₁₆								
005C ₁₆								
005D ₁₆								
005E ₁₆								
005F ₁₆								
0060 ₁₆								
0061 ₁₆								
0062 ₁₆								
0063 ₁₆								
0064 ₁₆								
0065 ₁₆								
0066 ₁₆								
0067 ₁₆								
0068 ₁₆								
0069 ₁₆								
006A ₁₆								
006B ₁₆								
006C ₁₆								
006D ₁₆								
006E ₁₆								
006F ₁₆								

For 24 segments and 8 digits
 (FLD data pointer reload register=7)

Address	Bit 7	6	5	4	3	2	1	0
0040 ₁₆								
0041 ₁₆								
0042 ₁₆								
0043 ₁₆								
0044 ₁₆								
0045 ₁₆								
0046 ₁₆								
0047 ₁₆								
0048 ₁₆								
0049 ₁₆								
004A ₁₆								
004B ₁₆								
004C ₁₆								
004D ₁₆								
004E ₁₆								
004F ₁₆								
0050 ₁₆								
0051 ₁₆								
0052 ₁₆								
0053 ₁₆								
0054 ₁₆								
0055 ₁₆								
0056 ₁₆								
0057 ₁₆								
0058 ₁₆								
0059 ₁₆								
005A ₁₆								
005B ₁₆								
005C ₁₆								
005D ₁₆								
005E ₁₆								
005F ₁₆								
0060 ₁₆								
0061 ₁₆								
0062 ₁₆								
0063 ₁₆								
0064 ₁₆								
0065 ₁₆								
0066 ₁₆								
0067 ₁₆								
0068 ₁₆								
0069 ₁₆								
006A ₁₆								
006B ₁₆								
006C ₁₆								
006D ₁₆								
006E ₁₆								
006F ₁₆								

Note.  Shaded areas are not used.

Fig. 32 Example of using the FLD automatic display RAM.

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Timing Setting

The digit timing (T_{disp}) and digit/segment turn-off timing (T_{off}) can be set by the FLDC mode register (address 0036_{16}). The scan timing (T_{scan}) can be set by the key-scan blanking register (address 0035_{16}).

Note that flickering will occur if the repetition frequency ($1/(T_{disp} \times \text{number of digits} + T_{scan})$) is an integral multiple of the digit timing T_{disp} .

FLD Start

To perform FLD automatic display, you have to use the following registers.

- Port P3 segment/digit switching register
- Port P0 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- FLD data pointer
- FLDC mode register

of the FLDC mode register (address 0036_{16}), and the automatic display is started by writing "1" to bit 1.

During automatic display bit 1 always keeps "1", automatic display can be interrupted by writing "0" to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period T_{scan} .

1. Write "0" to bit 0 (automatic display control bit) of FLDC mode register (address 0036_{16}).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write "1" (automatic display mode) to bit 0 of FLDC mode register (address 0036_{16}).

Note on performance of key-scan in the above 1 to 3 order.

1. Do not write "0" to bit 1 of FLDC mode register (address 0036_{16}).
2. Do not write "1" to the port corresponding to the digit.

Automatic display mode is activated by writing "1" to bit 0

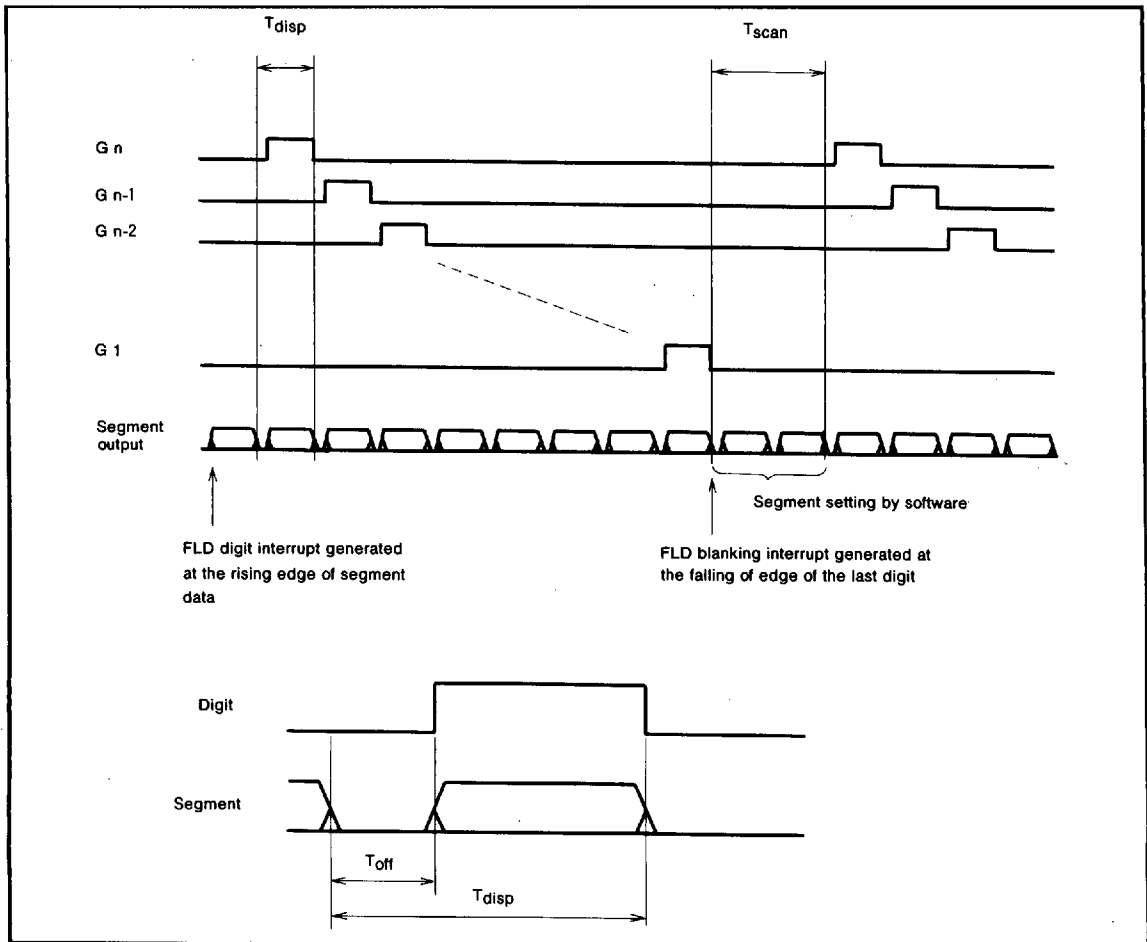


Fig. 33 FLDC timing

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RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

High-Speed Operation Start Mode

In high-speed operation start mode, to reset the microcomputer occurs, the RESET pin is held at an "L" level for $2\mu\text{s}$ or more. Then is returned to an "H" level (the power source voltage should be between 4.0V and 5.5V), reset is released. Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation begins until after 13 X_{IN} clock cycles are completed. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte).

Low-Speed Operation Start Mode

In low-speed operation start mode, to reset the microcomputer occurs, the RESET pin is held at an "L" level for $2\mu\text{s}$ or more. Then is returned to an "H" level (the power source voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte). If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})=32.768\text{kHz}$). Immediately after a poweron, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.

Note on Use

Make sure that the reset input voltage is less than 0.8V in high-speed operation start mode, or less than 0.5V in low-speed operation start mode.

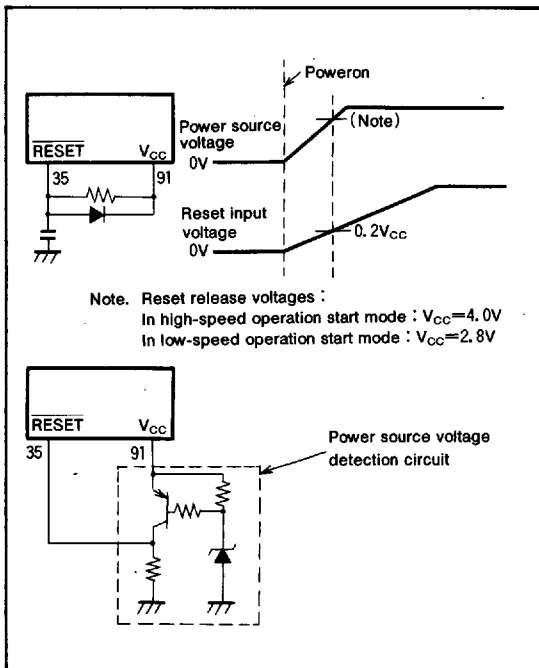


Fig. 34 Poweron reset circuit example

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Address Register contents			Address Register contents		
(1) Port P0 register	(0 0 0 0 ₁₆)...	00 ₁₆	(31) Timer 12 mode register	(0 0 2 8 ₁₆)...	00 ₁₆
(2) Port P1 register	(0 0 0 2 ₁₆)...	00 ₁₆	(32) Timer 34 mode register	(0 0 2 9 ₁₆)...	00 ₁₆
(3) Port P1 direction register	(0 0 0 3 ₁₆)...	00 ₁₆	(33) Timer 56 mode register	(0 0 2 A ₁₆)...	00 ₁₆
(4) Port P2 register	(0 0 0 4 ₁₆)...	00 ₁₆	(34) PWM control register	(0 0 2 B ₁₆)...	00 ₁₆
(5) Port P2 direction register	(0 0 0 5 ₁₆)...	00 ₁₆	(35) A-D control register	(0 0 3 0 ₁₆)...	08 ₁₆
(6) Port P3 register	(0 0 0 6 ₁₆)...	00 ₁₆	(36) Port P3 segment/digit	(0 0 3 2 ₁₆)...	00 ₁₆
(7) Port P4 register	(0 0 0 8 ₁₆)...	00 ₁₆	switching register		
(8) Port P4 direction register	(0 0 0 9 ₁₆)...	00 ₁₆	(37) Port P0 digit/port switching register	(0 0 3 3 ₁₆)...	00 ₁₆
(9) Port P5 register	(0 0 0 A ₁₆)...	00 ₁₆	(38) Port P8 segment/port	(0 0 3 4 ₁₆)...	00 ₁₆
(10) Port P5 direction register	(0 0 0 B ₁₆)...	00 ₁₆	switching register		
(11) Port P6 register	(0 0 0 C ₁₆)...	00 ₁₆	(39) Key-scan blanking register	(0 0 3 5 ₁₆)...	00 ₁₆
(12) Port P6 direction register	(0 0 0 D ₁₆)...	00 ₁₆	(40) FLDC mode register	(0 0 3 6 ₁₆)...	00 ₁₆
(13) Port P7 register	(0 0 0 E ₁₆)...	00 ₁₆	(41) High-breakdown-voltage port	(0 0 3 8 ₁₆)...	00 ₁₆
(14) Port P7 direction register	(0 0 0 F ₁₆)...	00 ₁₆	control register		
(15) Port P8 register	(0 0 1 0 ₁₆)...	00 ₁₆	(42) Interrupt edge selection register	(0 0 3 A ₁₆)...	00 ₁₆
(16) Port P8 direction register	(0 0 1 1 ₁₆)...	00 ₁₆	(43) CPU mode register	(0 0 3 B ₁₆)...	* * 1 0 0 0 0 0
(17) Port P9 register	(0 0 1 2 ₁₆)...	00 ₁₆	(44) Interrupt request register 1	(0 0 3 C ₁₆)...	00 ₁₆
(18) Port P9 direction register	(0 0 1 3 ₁₆)...	F0 ₁₆	(45) Interrupt request register 2	(0 0 3 D ₁₆)...	00 ₁₆
(19) Port PA register	(0 0 1 4 ₁₆)...	00 ₁₆	(46) Interrupt control register 1	(0 0 3 E ₁₆)...	00 ₁₆
(20) Port PA direction register	(0 0 1 5 ₁₆)...	00 ₁₆	(47) Interrupt control register 2	(0 0 3 F ₁₆)...	00 ₁₆
(21) Serial I/O1 control register	(0 0 1 9 ₁₆)...	00 ₁₆	(48) Processor status register	(P S)...	X X X X X 1 X X
(22) Serial I/O automatic transfer	(0 0 1 A ₁₆)...	00 ₁₆	(49) Program counter	(P C _H)...	Contents of address FFFD ₁₆
control register				(P C _L)...	Contents of address FFFC ₁₆
(23) Serial I/O automatic transfer	(0 0 1 C ₁₆)...	00 ₁₆			
interval register					
(24) Serial I/O2 control register	(0 0 1 D ₁₆)...	00 ₁₆			
(25) Timer 1 register	(0 0 2 0 ₁₆)...	FF ₁₆			
(26) Timer 2 register	(0 0 2 1 ₁₆)...	01 ₁₆			
(27) Timer 3 register	(0 0 2 2 ₁₆)...	FF ₁₆			
(28) Timer 4 register	(0 0 2 3 ₁₆)...	FF ₁₆			
(29) Timer 5 register	(0 0 2 4 ₁₆)...	FF ₁₆			
(30) Timer 6 register	(0 0 2 5 ₁₆)...	FF ₁₆			

Note. * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option.
X : Undefined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values.

Fig. 35 Internal status at reset

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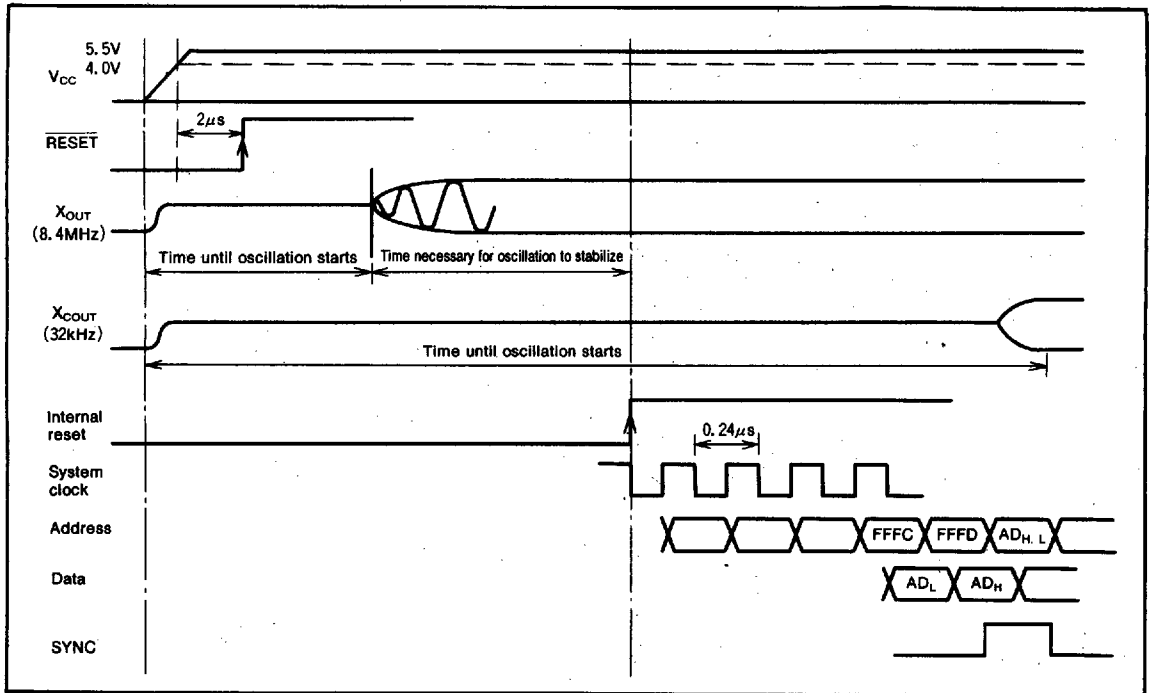


Fig. 36 Reset sequence in high-speed operation mode

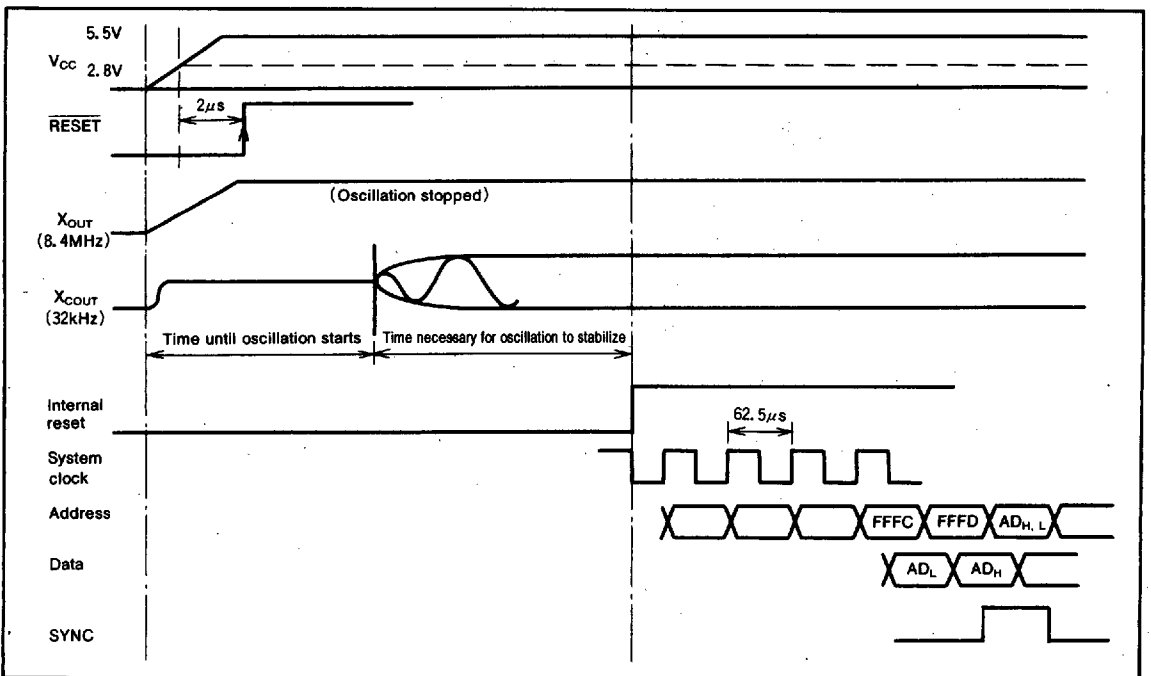


Fig. 37 Reset sequence in low-speed operation mode

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CLOCK GENERATING CIRCUIT

To supply a clock signal, input it to the X_{IN} (X_{CIN}) pin and make the X_{OUT} (X_{COUT}) pin open. If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS} , and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

High-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{IN} . Immediately after poweron, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address 003B₁₆) to "1".

Low-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{CIN} . Immediately after poweron, only the X_{CIN} clock starts oscillating. To set the internal clock ϕ to high-speed operation mode, first set bit 6 (CM_6) of the CPU mode register (address 003B₁₆) to "0", the set bit 7 (CM_7) to "0". Note that the program must allow time for oscillation to stabilize.

Oscillation Control

Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level. Timer 1 is set to "FF₁₆" and timer 2 is set to "01₁₆".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing an STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-Speed Mode

If the internal clock is generated from the sub-clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN} . To stop the main clock, set bit 6 (CM_6) of the CPU mode register (003B₁₆) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN} - X_{COUT} drivability can be reduced, allowing even lower power con-

sumption ($20\mu A$ with $f(X_{CIN}) = 32kHz$). To reduce the X_{CIN} - X_{COUT} drivability, clear bit 5 (CM_5) of the CPU mode register (003B₁₆) to "0". At reset or when an STP instruction is executed, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

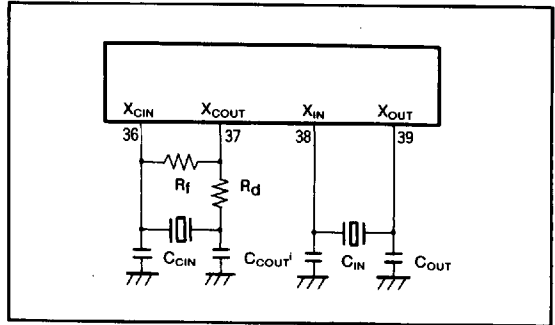


Fig. 38 Ceramic resonator circuit

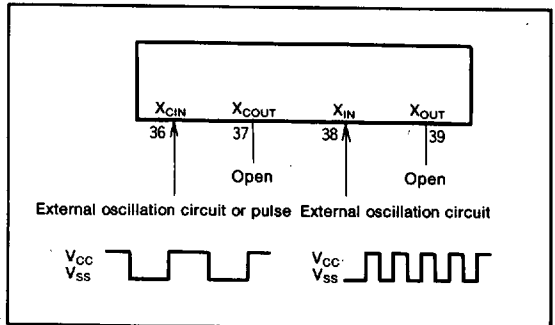


Fig. 39 External clock input circuit

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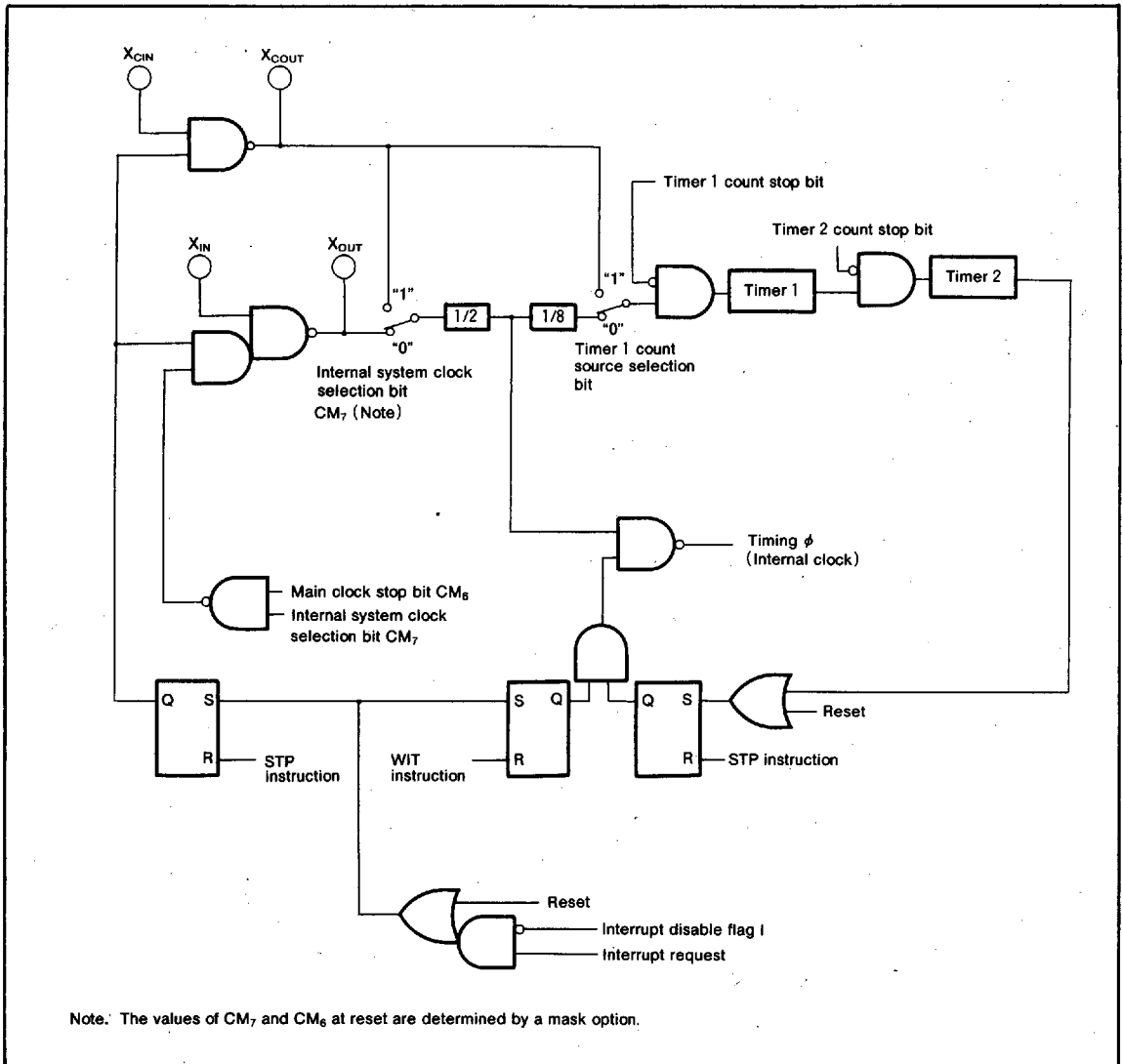


Fig. 40 System clock generation circuit block diagram

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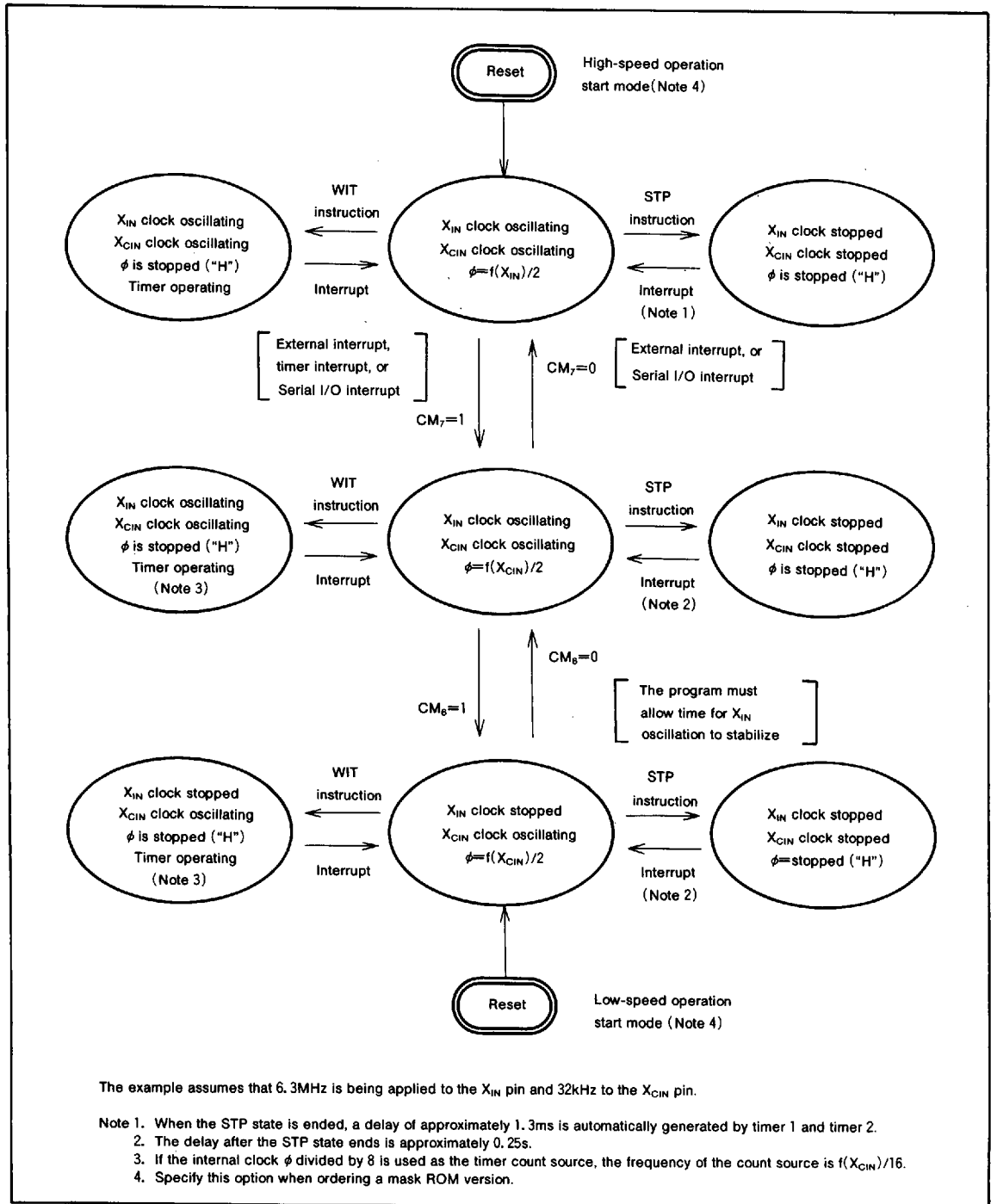


Fig. 41 State transitions of system clock

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NOTES ON PROGRAMMING
Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.

After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index.
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Do not write "1" to bit 0 of the port P4 direction register (address 0009₁₆).

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

Instruction Execution Timing

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

The X_{COUT} drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(X_{IN})$ is 500kHz or more during an A-D conversion.

Do not execute the STP or WIT instruction during A-D conversion.

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DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form
(three identical copies)

If required, specify the following option on the Mask Confirmation Form:

- Operation start mode switching option

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Package	Name of Programming Adapter
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 42 is recommended to verify programming.

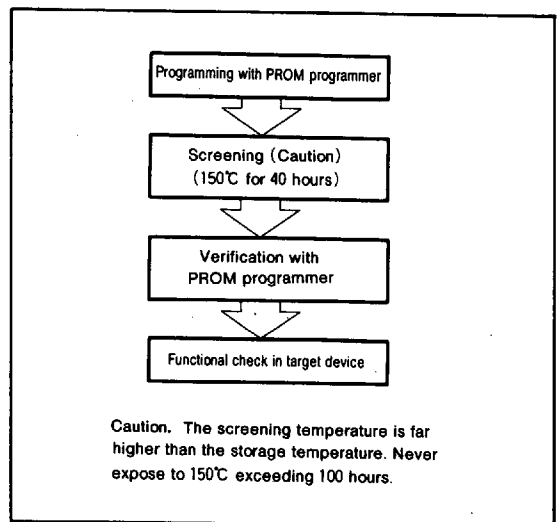


Fig. 42 Programming and testing of One Time PROM version

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS} . Output transistors are cut off.	-0.3 to 7.0	V
V_{EE}	Pull-down power source voltage		$V_{CC}-40$ to $V_{CC}+0.3$	V
V_I	Input voltage P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₁ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , PA ₀ -PA ₇ , PB ₀ , PB ₁		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage P4 ₀		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage P8 ₀ -P8 ₇ , P9 ₀ -P9 ₃		$V_{CC}-40$ to $V_{CC}+0.3$	V
V_I	Input voltage RESET, X _{IN}		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage X _{CIN}		-0.3 to $V_{CC}+0.3$	V
V_O	Output voltage P0 ₀ -P0 ₇ , P3 ₀ -P3 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇		$V_{CC}-40$ to $V_{CC}+0.3$	V
V_O	Output voltage P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₁ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , PA ₀ -PA ₇ , X _{OUT} , X _{COUT}		-0.3 to $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	600	mW
T_{opr}	Operating temperature		-10 to 85	°C
T_{stg}	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 4.0$ to 5.5V , $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage				V
	High-speed operation mode	4.0	5.0	5.5	
	Low-speed operation mode	2.8	5.0	5.5	
V_{SS}	Power source voltage		0		V
V_{EE}	Pull-down power source voltage	$V_{CC}-38$		V_{CC}	V
V_{REF}	Reference input voltage	2		V_{CC}	V
AV_{SS}	Analog power source voltage		0		V
V_{IA}	Analog input voltage	0		V_{CC}	V
V_{IH}	"H" input voltage P1 ₀ -P1 ₇ , P4 ₁ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , PA ₀ -PA ₇ , PB ₀ , PB ₁	$0.75V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage P2 ₀ -P2 ₇	$0.4V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage P4 ₀	$0.75V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage P8 ₀ -P8 ₇ , P9 ₀ -P9 ₃	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage RESET	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage X _{IN} , X _{CIN}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage P1 ₀ -P1 ₇ , P4 ₁ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , PA ₀ -PA ₇ , PB ₀ , PB ₁	0		$0.25V_{CC}$	V
V_{IL}	"L" input voltage P2 ₀ -P2 ₇	0		$0.16V_{CC}$	V
V_{IL}	"L" input voltage P4 ₀	0		$0.25V_{CC}$	V
V_{IL}	"L" input voltage P8 ₀ -P8 ₇ , P9 ₀ -P9 ₃	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage RESET	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage X _{IN} , X _{CIN}	0		$0.2V_{CC}$	V

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RECOMMENDED OPERATING CONDITIONS ($V_{CC}=4.0$ to $5.5V$, $T_a=-10$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0-P0_7$, $P1_0-P1_7$, (Note 1) $P2_0-P2_7$, $P3_0-P3_7$, $P8_0-P8_7$, $P9_0-P9_7$			-240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1-P4_7$, $P6_0-P6_7$, (Note 1) $P7_0-P7_7$, PA_0-PA_7			-60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P5_0-P5_7$, $P6_1-P6_7$, (Note 1) $P7_0-P7_7$, PA_0-PA_7			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$ (Note 1)			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0-P0_7$, $P1_0-P1_7$, (Note 1) $P2_0-P2_7$, $P3_0-P3_7$, $P8_0-P8_7$, $P9_0-P9_7$			-120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1-P4_7$, $P6_0-P6_7$, (Note 1) $P7_0-P7_7$, PA_0-PA_7			-30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P5_0-P5_7$, $P6_1-P6_7$, $P7_0-P7_7$, (Note 1) PA_0-PA_7			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$ (Note 1)			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0-P0_7$, $P3_0-P3_7$, $P8_0-P8_7$, (Note 2) $P9_0-P9_7$			-40	mA
$I_{OH(peak)}$	"H" peak output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, (Note 2) $P6_0-P6_7$, $P7_0-P7_7$, PA_0-PA_7			-10	mA
$I_{OL(peak)}$	"L" peak output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, (Note 2) $P6_1-P6_7$, $P7_0-P7_7$, PA_0-PA_7			10	mA
$I_{OL(peak)}$	"L" peak output current $P5_0-P5_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$ (Note 2)			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0-P0_7$, $P3_0-P3_7$, (Note 3) $P8_0-P8_7$, $P9_0-P9_7$			-18	mA
$I_{OH(avg)}$	"H" average output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, (Note 3) $P6_0-P6_7$, $P7_0-P7_7$, PA_0-PA_7			-5.0	mA
$I_{OL(avg)}$	"L" average output current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P6_1-P6_7$, $P7_0-P7_7$, PA_0-PA_7			5.0	mA
$I_{OL(avg)}$	"L" average output current $P5_0-P5_7$ (Note 3)			5.0	mA
$I_{OL(avg)}$	"L" average output current $P6_0$ (Note 3)			1.5	mA
$f(CNTR_0)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			8.4	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, Note 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.

2. The peak output current is the peak current flowing in each port.

3. The average output current is an average value measured over 100ms.

4. When the oscillation frequency has a duty cycle of 50%.

5. When using the microcomputer in low-speed operation mode, make sure that the sub-clock input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to $5.5V$, $T_a = -10$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0-P0_7$, $P3_0-P3_7$, $P8_0-P8_7$, $P9_0-P9_7$	$I_{OH} = -18mA$	$V_{CC} - 2.0$			V
V_{OH}	"H" output voltage $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P6_0-P6_7$, $P7_0-P7_7$, PA_0-PA_7	$I_{OH} = -10mA$	$V_{CC} - 2.0$			V
V_{OL}	"L" output voltage $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P5_0-P5_7$, $P6_1-P6_7$, $P7_0-P7_7$, PA_0-PA_7	$I_{OL} = 10mA$			2.0	V
V_{OL}	"L" output voltage $P6_0$	$I_{OL} = 1.5mA$			0.5	V
$V_{T+} - V_{T-}$	Hysteresis INT_0-INT_4 , S_{IN1} , S_{IN2} , S_{CLK1} , S_{CLK2} , $CNTR_0$, $CNTR_1$	When using a non-port function		0.4		V
$V_{T+} - V_{T-}$	Hysteresis $RESET$, X_{IN}	$RESET : V_{CC} = 2.8V$ to $5.5V$		0.5		V
$V_{T+} - V_{T-}$	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P5_0-P5_7$, $P6_0-P6_7$, $P7_0-P7_7$, PA_0-PA_7 , PB_0 , PB_1	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current $P4_0$	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current $P8_0-P8_7$, $P9_0-P9_3$ (Note 1)	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current $RESET$, X_{CIN}	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current X_{IN}	$V_i = V_{CC}$		4.0		μA
I_{IL}	"L" input current $P1_0-P1_7$, $P2_0-P2_7$, $P4_1-P4_7$, $P5_0-P5_7$, $P6_0-P6_7$, $P7_0-P7_7$, PA_0-PA_7 , PB_0 , PB_1	$V_i = V_{SS}$			-5.0	μA
I_{IL}	"L" input current $P4_0$	$V_i = V_{SS}$			-5.0	μA
I_{IL}	"L" input current $P8_0-P8_7$, $P9_0-P9_3$ (Note 1)	$V_i = V_{SS}$			-5.0	μA
I_{IL}	"L" input current $RESET$, X_{CIN}	$V_i = V_{SS}$			-5.0	μA
I_{IL}	"L" input current X_{IN}	$V_i = V_{SS}$		-4.0		μA
I_{LOAD}	Output load current $P0_0-P0_7$, $P3_0-P3_7$, $P9_0-P9_7$	$V_{EE} = V_{CC} - 36V$, $V_{OL} = V_{CC}$, Output transistors "off"	150	500	900	μA
I_{LEAK}	Output leakage current $P0_0-P0_7$, $P3_0-P3_7$, $P8_0-P8_7$, $P9_0-P9_7$	$V_{EE} = V_{CC} - 38V$, $V_{OL} = V_{CC} - 38V$, Output transistors "off" (Except for reset)			-10	μA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power source current	* High-speed mode $f(X_{IN}) = 8.4MHz$ $f(X_{CIN}) = 32kHz$ Output transistors "off" A-D converter operating		10	20	mA
		* High-speed mode $f(X_{IN}) = 8.4MHz$ (in WIT state) $f(X_{CIN}) = 32kHz$ Output transistors "off" A-D converter stopped		1.5		mA
		* Low-speed mode $f(X_{IN}) =$ stopped, $f(X_{CIN}) = 32kHz$ Low-power dissipation mode set ($CM_5 = 0$) Output transistors "off"		60	200	μA
		* Low-speed mode $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32kHz$ (in WIT state) Low-power dissipation mode set ($CM_5 = 0$) Output transistors "off"		20	40	μA
		All oscillation stopped (in STP state)		0.1	1.0	μA
		Output transistors "off"			10	

Note 1. Except when reading ports $P8_0-P8_7$ or ports $P9_0-P9_3$.

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A-D CONVERTER CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=-10 to 85°C, high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	V _{CC} =V _{REF} =5.12V		±1	±2.5	LSB
T _{CONV}	Conversion time		49		50	t _C (φ)
I _{VREF}	Reference input current	V _{REF} =5V	50	150	200	μA
I _{IA}	Analog port input current			0.5	5.0	μA
R _{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=-10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _W (RESET)	Reset input "L" pulse width		2.0			μs
t _C (X _{IN})	Main clock input cycle time (X _{IN} input)		119			ns
t _{WH} (X _{IN})	Main clock input "H" pulse width		40			ns
t _{WL} (X _{IN})	Main clock input "L" pulse width		40			ns
t _C (X _{CIN})	Sub-clock input cycle time (X _{CIN} input)		20			μs
t _{WH} (X _{CIN})	Sub-clock input "H" pulse width		5.0			μs
t _{WL} (X _{CIN})	Sub-clock input "L" pulse width		5.0			μs
t _C (CNTR)	CNTR ₀ , CNTR ₁ input cycle time		4.0			μs
t _{WH} (CNTR)	CNTR ₀ , CNTR ₁ input "H" pulse width		1.6			μs
t _{WL} (CNTR)	CNTR ₀ , CNTR ₁ input "L" pulse width		1.6			μs
t _{WH} (INT)	INT ₀ -INT ₄ input "H" pulse width		80			ns
t _{WL} (INT)	INT ₀ -INT ₄ input "L" pulse width		80			ns
t _C (SCLK)	Serial I/O clock input cycle time		1.0			μs
t _{WH} (SCLK)	Serial I/O clock input "H" pulse width		400			ns
t _{WL} (SCLK)	Serial I/O clock input "L" pulse width		400			ns
t _{SU} (SCLK-S _{IN})	Serial I/O input setup time		200			ns
t _H (SCLK-S _{IN})	Serial I/O input hold time		200			ns

SWITCHING CHARACTERISTICS (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=-10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output "H" pulse width	C _L =100pF, R _L =1kΩ	t _C (SCLK) /2-160			ns
t _{WL} (SCLK)	Serial I/O clock output "L" pulse width	C _L =100pF, R _L =1kΩ	t _C (SCLK) /2-160			ns
t _d (SCLK-S _{OUT})	Serial I/O output delay time				0.2t _C (SCLK)	ns
t _v (SCLK-S _{OUT})	Serial I/O output hold time		0			ns
t _f (SCLK)	Serial I/O clock output falling time	C _L =100pF, R _L =1kΩ			40	ns
t _r (Pch-strg)	P-channel high-breakdown voltage output rising time (Note 1)	C _L =100pF, V _{EE} =V _{CC} -36V		55		ns
t _r (Pch-weak)	P-channel high-breakdown voltage output rising time (Note 2)	C _L =100pF, V _{EE} =V _{CC} -36V		1.8		μs

Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038₁₆) is at "0".2. When bit 0 of the high-breakdown voltage port control register (address 0038₁₆) is at "1".

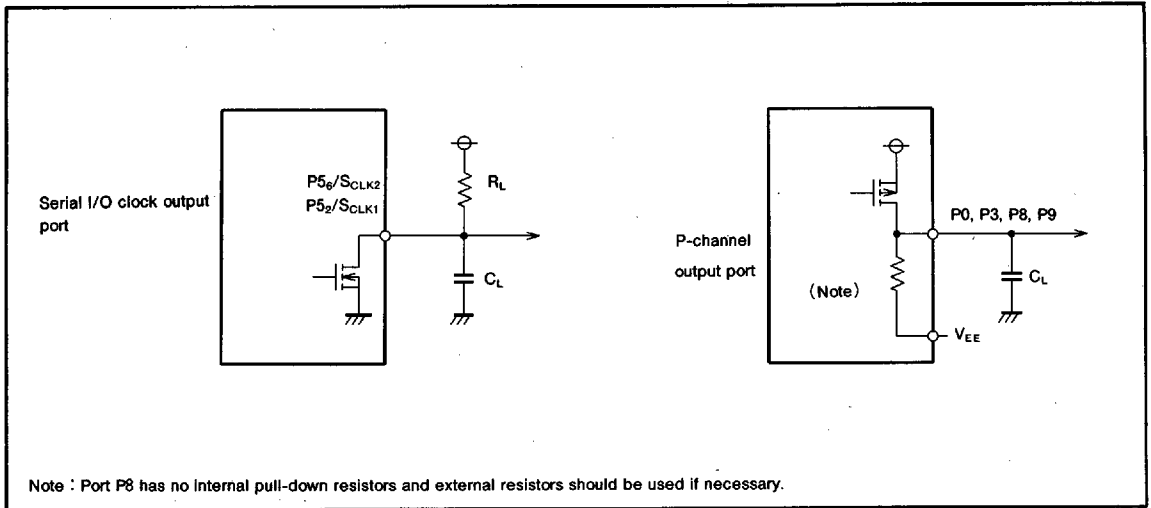


Fig. 43 Output switching characteristics measurement circuit

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Timing Chart

