



September 2000

QFET™

FQB5N80 / FQI5N80

800V N-Channel MOSFET

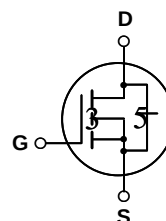
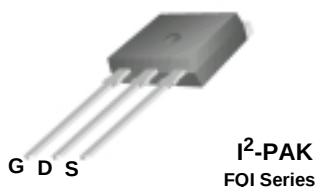
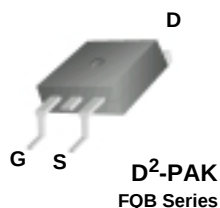
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

Features

- 4.8A, 800V, $R_{DS(on)} = 2.6\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 25 nC)
- Low C_{rss} (typical 11 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB5N80 / FQI5N80	Units
V_{DSS}	Drain-Source Voltage	800	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	4.8	A
	- Continuous ($T_C = 100^\circ\text{C}$)	3.04	A
I_{DM}	Drain Current - Pulsed (Note 1)	19.2	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	590	mJ
I_{AR}	Avalanche Current (Note 1)	4.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	14	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	140	W
	- Derate above 25°C	1.12	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.89	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.9	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.4\text{ A}$	--	2.0	2.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 2.4\text{ A}$ (Note 4)	--	4.9	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	950	1250	pF
C_{oss}	Output Capacitance		--	95	125	pF
C_{rss}	Reverse Transfer Capacitance		--	11	15	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 4.8\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	22	55	ns
t_r	Turn-On Rise Time		--	60	130	ns
$t_{d(off)}$	Turn-Off Delay Time		--	55	120	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 4.8\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	25	33	nC
Q_{gs}	Gate-Source Charge		--	5.6	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.8	A		
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	19.2	A		
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.8 A	--	--	1.4	V	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 4.8 A,	(Note 4)	--	610	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs		--	4.7	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 48\text{ mH}, I_{AS} = 4.8\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.8\text{ A}, dI/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

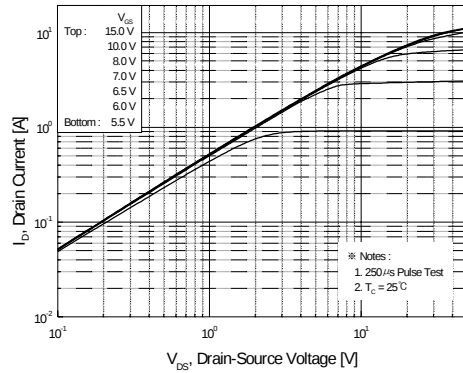


Figure 1. On-Region Characteristics

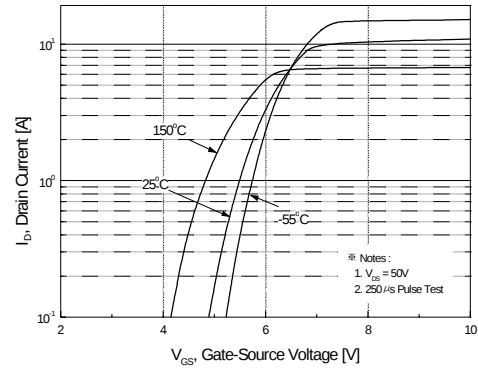


Figure 2. Transfer Characteristics

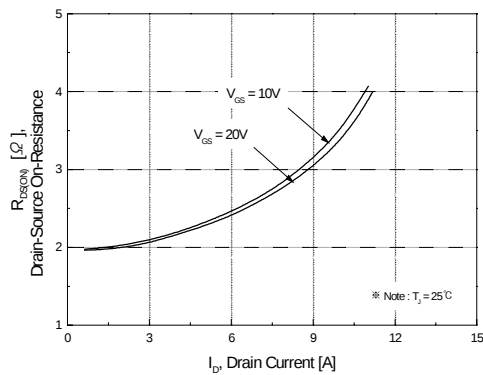


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

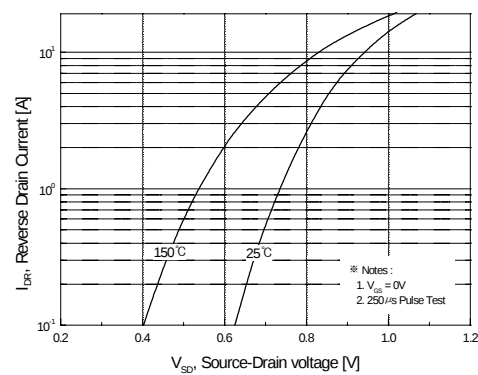


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

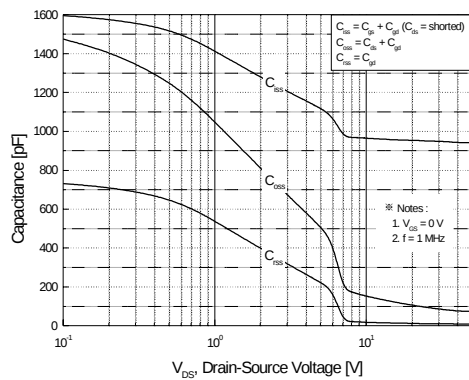


Figure 5. Capacitance Characteristics

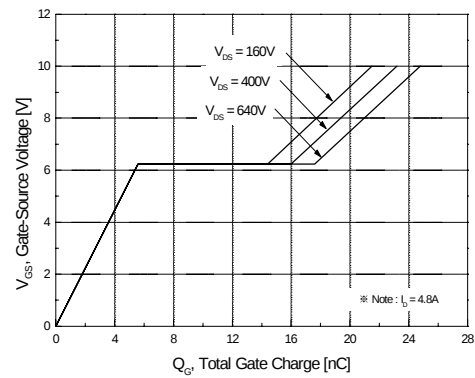


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

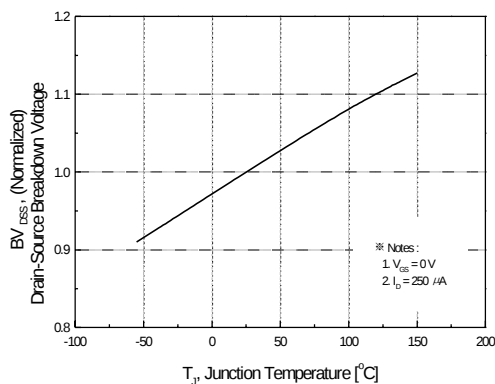


Figure 7. Breakdown Voltage Variation vs. Temperature

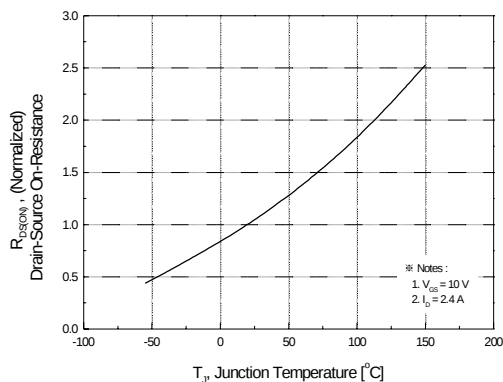


Figure 8. On-Resistance Variation vs. Temperature

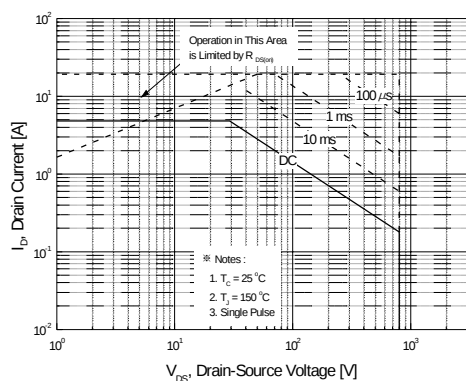


Figure 9. Maximum Safe Operating Area

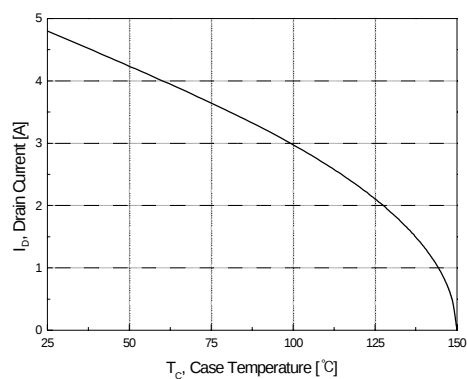


Figure 10. Maximum Drain Current vs. Case Temperature

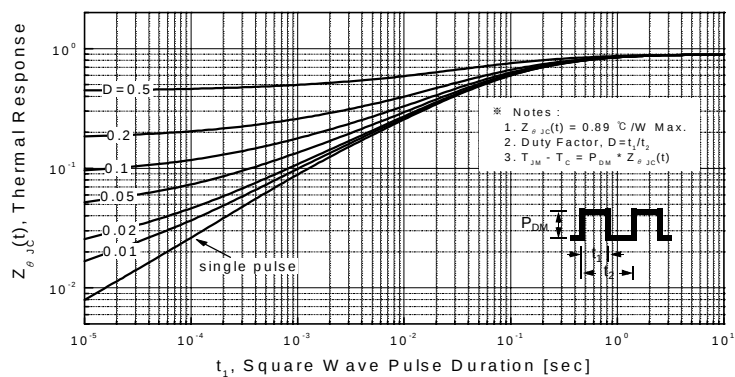


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Technical drawing of a 10-pin D-subminiature connector, showing three views: front, side, and top. Dimensions are in millimeters.

Front View:

- Overall width: 9.90 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height (from base): 1.40 ± 0.20
- Pin pitch: 2.54 TYP
- Pin diameter: 0.80 ± 0.10
- Internal width (between pins): 1.27 ± 0.10
- Internal height (between pins): 4.90 ± 0.20
- Internal width (between pins): 0.80 ± 0.10
- Internal height (between pins): 9.20 ± 0.20
- Internal width (between pins): 1.20 ± 0.20

Side View:

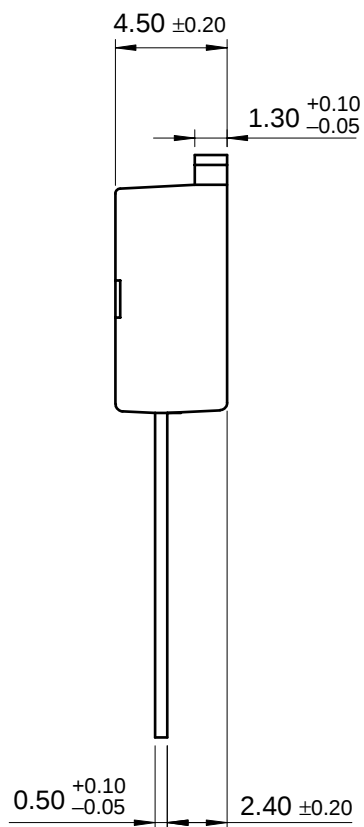
- Overall width: 4.50 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height (from base): $1.30^{+0.10}_{-0.05}$
- Pin pitch: 2.54 ± 0.30
- Pin diameter: $0.50^{+0.10}_{-0.05}$
- Internal width (between pins): 2.40 ± 0.20
- Internal height (between pins): 2.00 ± 0.10
- Internal width (between pins): 0.10 ± 0.15
- Internal height (between pins): 9.20 ± 0.20
- Internal width (between pins): 0.80 ± 0.10
- Internal height (between pins): 4.90 ± 0.20
- Internal width (between pins): 1.20 ± 0.20

Top View:

- Overall width: 10.00 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height (from base): 1.75
- Pin pitch: 2.54 TYP
- Pin diameter: 0.80 ± 0.10
- Internal width (between pins): 1.27 ± 0.10
- Internal height (between pins): 4.90 ± 0.20
- Internal width (between pins): 0.80 ± 0.10
- Internal height (between pins): 9.20 ± 0.20
- Internal width (between pins): 1.20 ± 0.20

FQ̇B5N80 / FQ̇I5N80

Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view dimensions are: overall width 9.90 ±0.20 mm (0.40 in), overall height 13.08 ±0.20 mm (0.515 in), and pin spacing 2.54 TYP mm. The side view dimensions are: pin diameter 1.27 ±0.10 mm (0.05 in), pin length 10.08 ±0.20 mm (0.397 in), and pin angle 45°. The connector body dimensions are: body width 9.90 ±0.20 mm (0.40 in), body height 9.20 ±0.20 mm (0.362 in), and body thickness 1.20 ±0.20 mm (0.047 in). The connector body has a central circular feature.



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