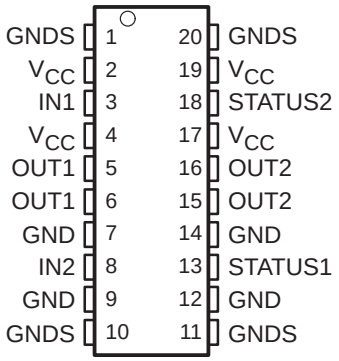
- **Low Quiescent Supply Current of 20 μA**
- **Optimized for Low-Power/Battery-Operated Applications**
- **Two Input Control Lines for Reduced Microcontroller Overhead**
- **Internal Current Shutdown of 5 A**
- **40 V Load Dump Rating**
- **Integrated Fault Protection and Diagnostics**
- **CMOS Compatible Schmitt Trigger Inputs for High Noise Immunity**

DWP PACKAGE
(TOP VIEW)



description

The TPIC0108B is a PWM control intelligent H-bridge designed specifically for dc motor applications. The device provides forward, reverse, and brake modes of operation. A logic supply voltage of 5 V is internally derived from V_{CC}.

The TPIC0108B has an extremely low $r_{DS(on)}$, 280 mΩ typical, to minimize system power dissipation. The control inputs (IN1 and IN2) greatly simplify the microcontroller overhead requirement. The device has a low quiescent supply current of 20 μA to suit a wide range of automotive and industrial battery-operated applications.

The TPIC0108B provides protection against over-voltage, over-current, over-temperature, and cross conduction faults. Fault diagnostics can be obtained by monitoring the STATUS1 and STATUS2 terminals and the two input control lines. STATUS1 is an open-drain output suitable for wired-or connection. STATUS2 is a push-pull output that provides a latched status output. Under-voltage protection ensures that the outputs, OUT1 and OUT2, will be disabled when V_{CC} is less than the under-voltage detection voltage $V_{(UVCC)}$.

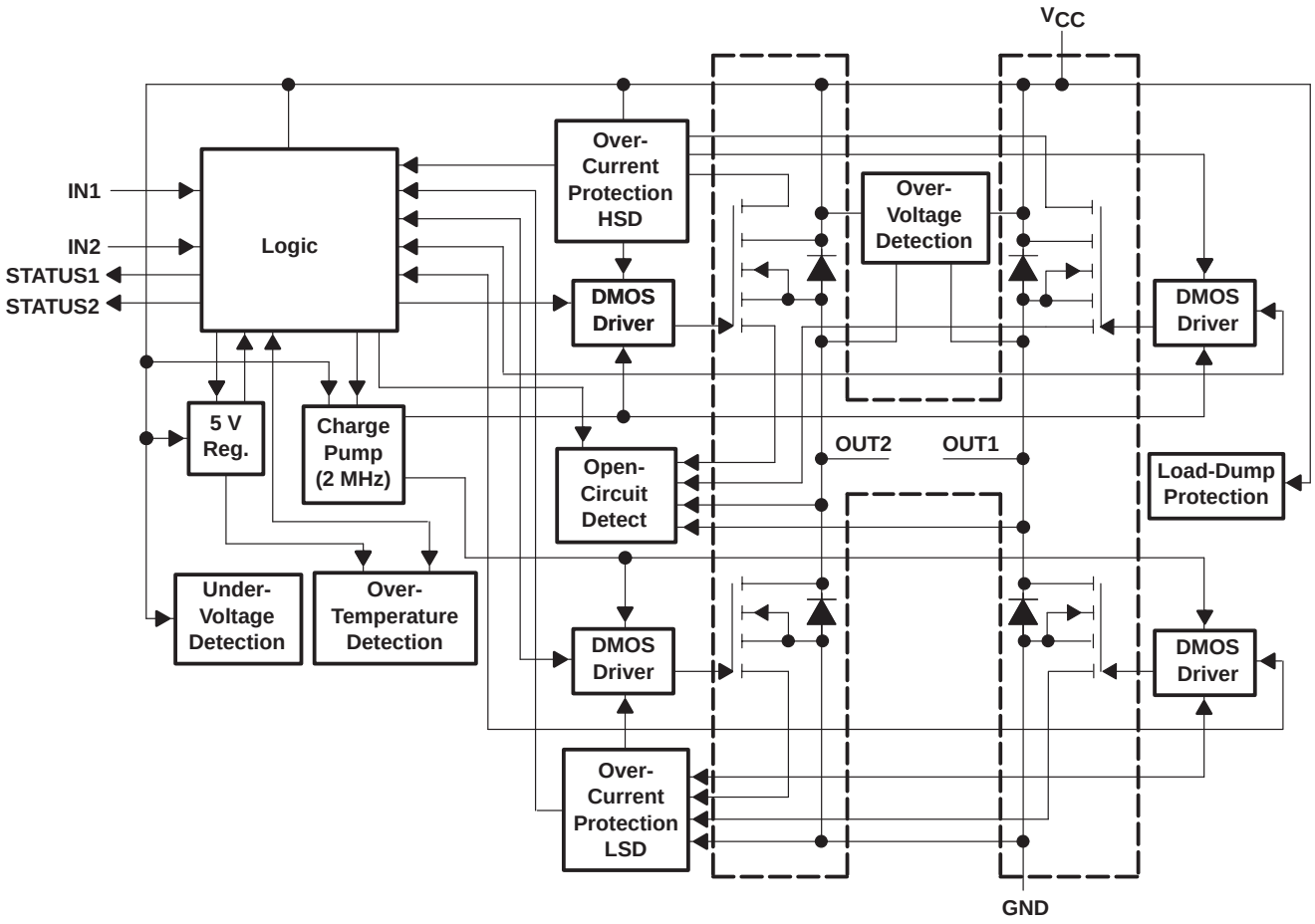
The TPIC0108B is designed using TI's LinBiCMOS™ process. LinBiCMOS allows the integration of low power CMOS structures, precision bipolar cells, and low impedance DMOS transistors.

The TPIC0108B is offered in a 20-pin thermally enhanced small-outline package (DWP) and is characterized for operation over the operating case temperature of –40°C to 125°C.

FUNCTION TABLE

IN1	IN2	OUT1	OUT2	MODE
0	0	Z	Z	Quiescent supply current mode
0	1	LS	HS	Motor turns clockwise
1	0	HS	LS	Motor turns counter clockwise
1	1	HS	HS	Brake, both HSDs turned on hard

block schematic

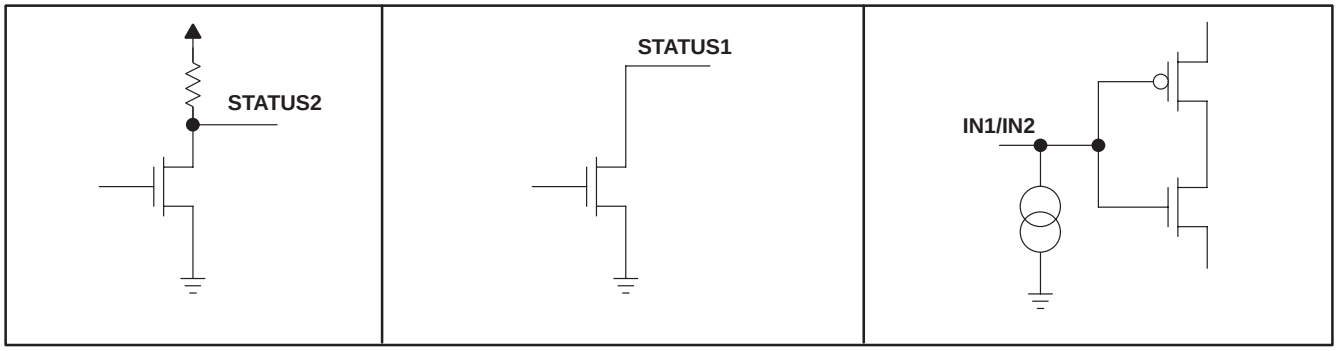


Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	7, 9, 12, 14	I	Power ground
GNDS	1, 10, 11, 20	I	Substrate ground
IN1	3	I	Control input
IN2	8	I	Control input
OUT1	5, 6	O	Half-H output. DMOS output
OUT2	15, 16	O	Half-H output. DMOS output
STATUS1	13	O	Status output
STATUS2	18	O	Latched status output
V_{CC}	2, 4, 17, 19	I	Supply voltage

NOTE: It is mandatory that all four ground terminals plus at least one substrate terminal are connected to the system ground. Use all V_{CC} and OUT terminals.

schematics of inputs and outputs



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Power supply voltage range, V_{CC} . . . . . –0.3 V to 33 V
Logic input voltage range, V_{IN} . . . . . –0.3 V to 7 V
Load dump (for 400 ms; T_C = 25°C) . . . . . 40 V
Status output voltage range, $V_{O(status)}$ . . . . . –0.3 V to 7 V
Continuous power dissipation, T_C = 25°C . . . . . 25 W
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
25 W	–0.2 W/°C	16 W	5 W

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	6	18	V
Operating case temperature, T_C	–40	125	°C
Switching frequency, f_{PWM}		2	kHz

electrical characteristics over recommended operating case temperature range and V_{CC} = 5 V to 6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-resistance (per transistor) $I_{(BR)}$ = 1 A	LSD	T_J = 25°C			550	mΩ
			T_J = 150°C			850	
		HSD	T_J = 25°C			600	mΩ
			T_J = 150°C			870	
$I_{(QCD)}$	Open circuit detection current			10	40	100	mA
$V_{(UVCC(OFF))}$	Under voltage detection on V_{CC}, switch off voltage		See Note 1			5	V
$V_{(UVCC(ON))}$	Under voltage detection on V_{CC}, switch on voltage		See Note 1			5.2	V
$V_{(STL)}$	STATUS low output voltage		I_O = 100 μA, See Note 1			0.8	V
$V_{(ST2H)}$	STATUS2 high output voltage		I_O = 20 μA, See Note 1	3		5.4	V
$I_{(ST(OFF))}$	STATUS output leakage current		$V_{(ST)}$ = 5 V, See Note 1			5	μA
V_{IL}	Low level logic input voltage			–0.3		0.5	V
V_{IH}	High level logic input voltage			3.6		7	V
ΔV_I	Hysteresis of input voltage			0.3			V
I_{IH}	High level logic input current		V_{IH} = 3.5 V	2	10	50	μA

NOTE 1: The device functions according to the function table for V_{CC} between $V_{(UVCC)}$ and 5 V (no parameters specified). STATUS outputs are not defined for V_{CC} less than $V_{(UVCC)}$.

electrical characteristics over recommended operating case temperature and supply voltage ranges (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-resistance (per transistor) I_{BR} = 1 A	LSD	T_J = 25°C	V_{CC} = 6 V to 9 V			380	mΩ
				V_{CC} = 9 V to 18 V		280	340	
			T_J = 150°C	V_{CC} = 6 V to 9 V			620	
				V_{CC} = 9 V to 18 V		400	560	
		HSD	T_J = 25°C	V_{CC} = 6 V to 9 V			430	mΩ
				V_{CC} = 9 V to 18 V		280	340	
			T_J = 150°C	V_{CC} = 6 V to 9 V			640	
				V_{CC} = 9 V to 18 V		400	560	
$I_{(QB)}$	Quiescent battery current		T_J = 25°C	V_{CC} = 13.2 V			20	µA
$I_{(QCD)}$	Open circuit detection current				10	40	100	mA
T_{SDS}	Static thermal shutdown temperature		See Notes 3 and 4		140			°C
T_{SDD}	Dynamic thermal shutdown temperature		See Notes 3 and 5		160			°C
I_{CS}	Current shutdown limit		V_{CC} = 6 V to 9 V		4.8		7.5	A
			V_{CC} = 9 V to 18 V		5		7.5	
$I_{(CON)}$	Continuous bridge current		T_J = 125°C, Operating lifetime 10,000 hours, (see Figure 1)				3	A
$V_{(OVCC)}$	Over voltage detection on V_{CC}				27		36	V
$V_{(STL)}$	STATUS low output voltage		I_O = 100 µA				0.8	V
$V_{(ST2H)}$	STATUS2 high output voltage		I_O = 20 µA		3.9		5.4	V
$I_{(ST(OFF))}$	STATUS output leakage current		$V_{(ST)}$ = 5 V				5	µA
V_{IL}	Low level logic input voltage				–0.3		0.8	V
V_{IH}	High level logic input voltage				3.6		7	V
ΔV_I	Hysteresis of input voltage				0.3			V
I_{IH}	High level logic input current		V_{IH} = 3.5 V		2	10	50	µA

NOTES: 2. The device functions according to the function table for V_{CC} between 18 V and $V_{(OVCC)}$, but only up to a maximum supply voltage of 33 V (no parameters specified). Exposure beyond 18 V for extended periods may affect device reliability.
3. Exposure beyond absolute-maximum-rated condition of junction temperature may affect device reliability.
4. No temperature gradient between DMOS transistor and temperature sensor.
5. With temperature gradient between DMOS transistor and temperature sensor in a typical application (DMOS transistor as heat source).

switching characteristics over recommended operating case temperature and supply voltage ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{out(on)}$	High-side driver turn-on time	$V_{DS(on)}$<1 V at 1 A,	V_{CC} = 13.2 V			100	µs
	Low-side driver turn-on time					100	
SR	Slew rate, low-to-high sinusoidal (δV/δt)	V_{CC} = 13.2 V,	I_O = 1 A resistive load	1		6	V/µs
	Slew rate, high-to-low sinusoidal (δV/δt)			1		6	
$t_{d(QCD)}$	Under current spike duration to trigger open circuit detection	V_{CC} = 5 V to 18 V		1		10	ms
$t_{d(CS)}$	Delay time for over current shutdown			5	10	25	µs

thermal resistance

PARAMETER		MIN	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		97	°C/W

PARAMETER MEASUREMENT INFORMATION

Maximum continuous bridge current versus time based on 50 FITs at 100,000 hours operating life (90% confidence model)

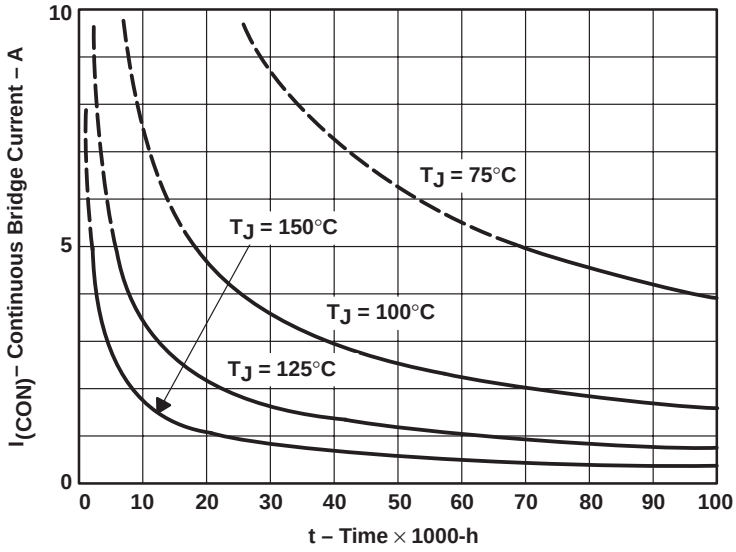


Figure 1. Electromigration Reliability Data

Example:

Average continuous bridge current, I_{CON}	Average junction temperature, T_J	Operating lifetime of device based on electromigration
2 A	125°C	>20,000 h
3 A	125°C	>10,000 h

PARAMETER MEASUREMENT INFORMATION

operating wave forms

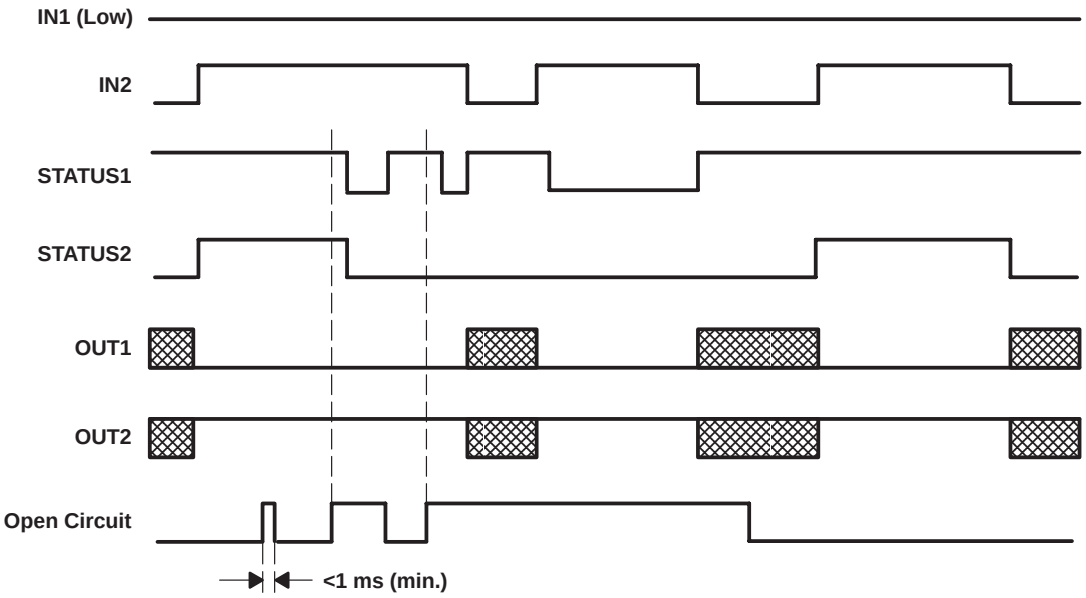


Figure 2. Open Circuit

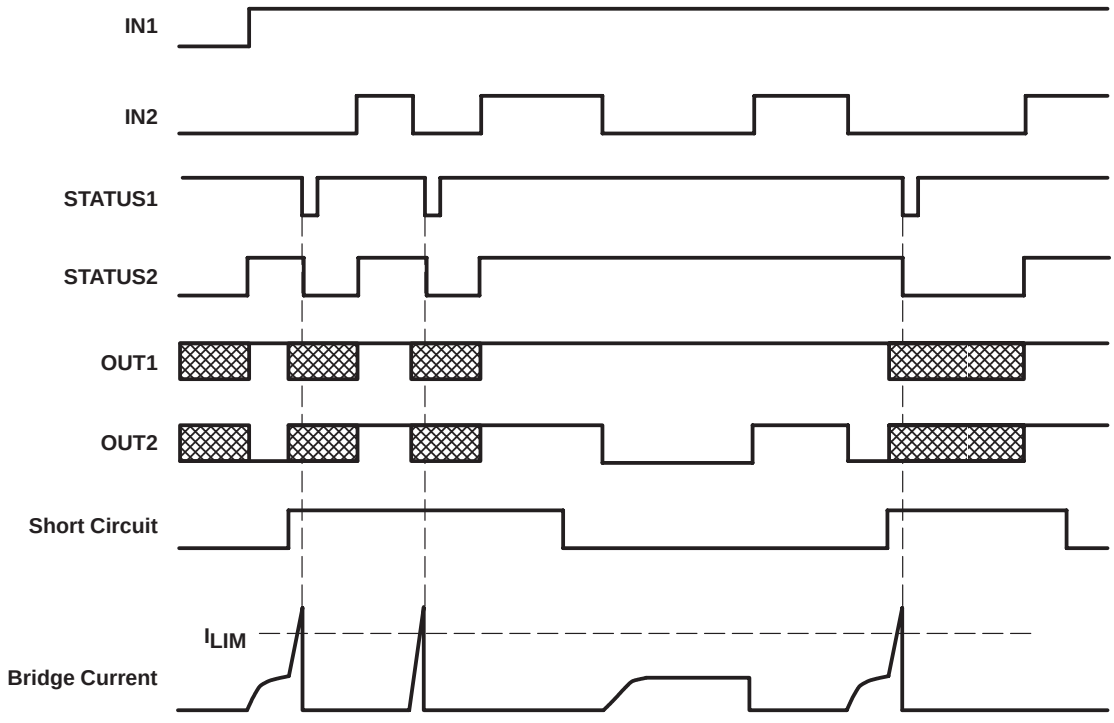


Figure 3. Short Circuit (e.g., OUT2 to V_{CC})

PARAMETER MEASUREMENT INFORMATION

operating wave forms (continued)

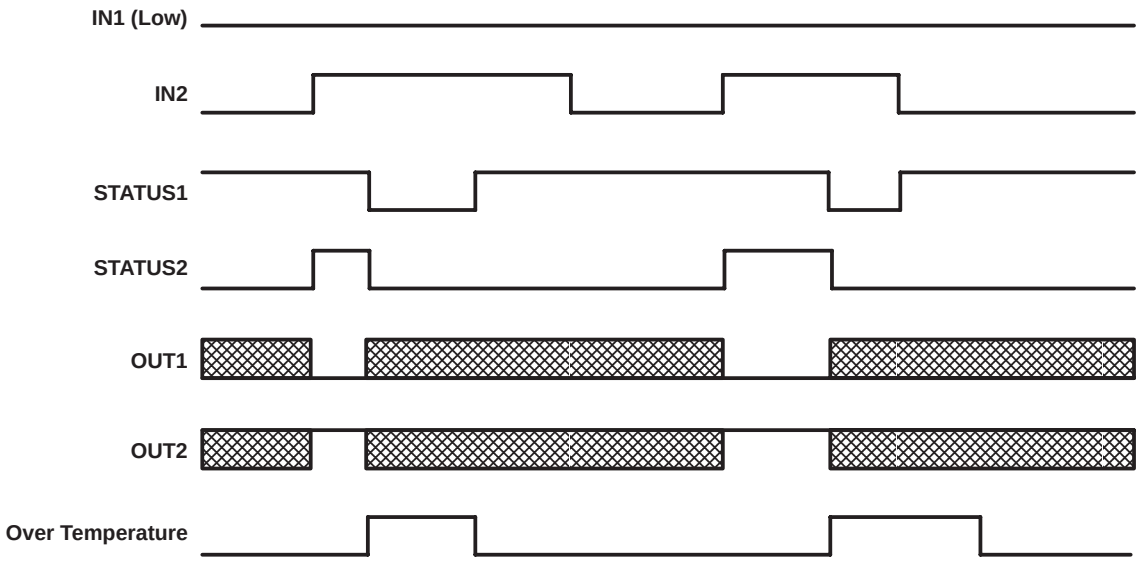


Figure 4. Over Temperature

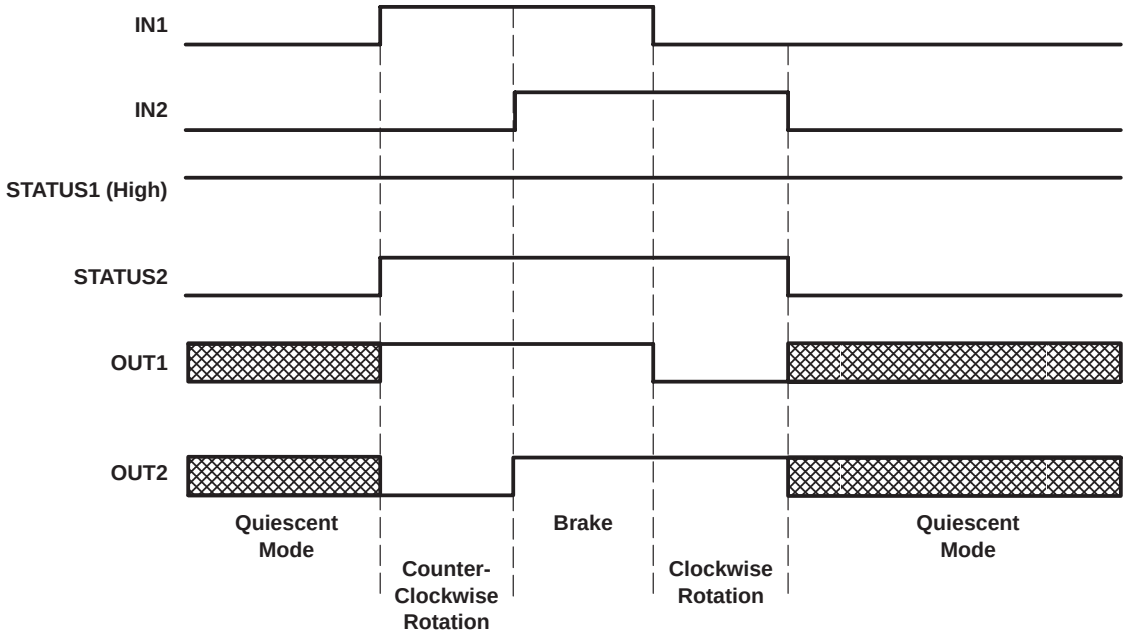


Figure 5. No Fault

PRINCIPLES OF OPERATION

protective functions and diagnostics†

over current/short circuit‡

The TPIC0108B detects shorts to V_{CC}, ground, or across the load being driven, by comparing the V_{DS} voltage drop across the DMOS outputs against the threshold voltage. The DMOS outputs of the TPIC0108B will be disabled and the fault flags will be generated 10 μs after an over-current or short-circuit fault is detected. This 10 μs delay is long enough to serve as a de-glitch filter for high current transients, yet short enough to prevent damage to the DMOS outputs. The DMOS outputs remain latched off until either IN1 or IN2 input is toggled.

In cases where the outputs have a continuous short-to-ground or when enabled from quiescent mode with a short-to-ground already exists (current rise time faster than 0.5 A/μs in both instances), the over-current shutdown threshold will decrease to 3 A to reduce power dissipation. This reduction to 3 A is achieved since the DMOS outputs will not be fully enhanced when the over-current threshold is reached if the current rise time exceeds 0.5 A/μs. Over-current and/or short-circuit protection is provided up to V_{CC} = 16.5 V and a junction temperature of 90°C.

over temperature

The TPIC0108B disables all DMOS outputs and the fault flags will be set when $T_J \geq 140°C$ (min.). The DMOS outputs remain latched off until either IN1 or IN2 input is toggled.

under voltage

The TPIC0108B disables all DMOS outputs when $V_{CC} \leq V_{(UVCC)}$. The outputs will be re-enabled when $V_{CC} \geq V_{(UVCC)}$. No fault flags are set when under-voltage lockout occurs.

over voltage

In order to protect the DMOS outputs from damage caused by excessive supply voltage, the TPIC0108B disables all outputs when $V_{CC} \geq V_{(OVCC)}$. Once $V_{CC} \leq V_{(OVCC)}$, either IN1 or IN2 input must be toggled to re-enable the DMOS outputs.

cross conduction

Monitoring circuitry for each transistor detects whether the particular transistor is active to prevent the HSD or LSD of the corresponding half H-bridge from conducting.

open circuit

During operation, the bridge current is controlled continuously. If the bridge current is >10 mA (min.) for a period >1 ms (min.), the fault flags are set. However, the output transistors will not be disabled.

† All limits mentioned are typical values unless otherwise noted.
‡ If a short circuit occurs (i.e., the over-current detection circuitry is activated) at a supply voltage higher than 16.5 V and a junction temperature higher than 90°C, damage to the device may occur.

PRINCIPLES OF OPERATION

DIAGNOSTICS TABLE (see Note 6)

FLAG	IN1	IN2	OUT1	OUT2	STATUS1†	STATUS2
Normal operation	0	0	Z	Z	1	0‡
	0	1	LS	HS	1	1
	1	0	HS	LS	1	1
	1	1	HS	HS	1	1
Open circuit between OUT1 and OUT2	0	0	Z	Z	1	0‡
	0	1	LS	HS	0	0
	1	0	HS	LS	0	0
	1	1	HS	HS	1	1
Short circuit from OUT1 to OUT2 (see Notes 7 and 8)	0	1	X	X	0	0
	1	0	X	X	0	0
Short circuit from OUT1 to GND (see Notes 7 and 8)	1	0	X	X	0	0
	1	1	X	X	0	0
Short circuit from OUT2 to GND (see Notes 7 and 8)	0	1	X	X	0	0
	1	1	X	X	0	0
Short circuit from OUT1 to V_{CC} (see Notes 7 and 8)	0	1	X	X	0	0
Short circuit from OUT2 to V_{CC} (see Notes 7 and 8)	1	0	X	X	0	0
Over temperature (see Note 9)	0	0	Z	Z	1	0‡
	0	1	Z	Z	0	0
	1	0	Z	Z	0	0
	1	1	Z	Z	0	0

† When wired with a pull-up resistor
‡ In quiescent mode, STATUS2 is pulled down to GND via an internal resistor.

SYMBOL	VALUE
0	Logic low
1	Logic high
HS	High-side MOSFET conducting
LS	Low-side MOSFET conducting
Z	No output transistors conducting
X	Voltage level undefined

NOTES: 6. All input combinations not stated result in STATUS output = 1.
7. STATUS1 active for a minimum of 3 μs.
8. STATUS2 active until an input is toggled.
9. Quiescent current consumption can occur only when the temperature drops below the thermal switch-off temperature.

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-RESISTANCE vs JUNCTION TEMPERATURE

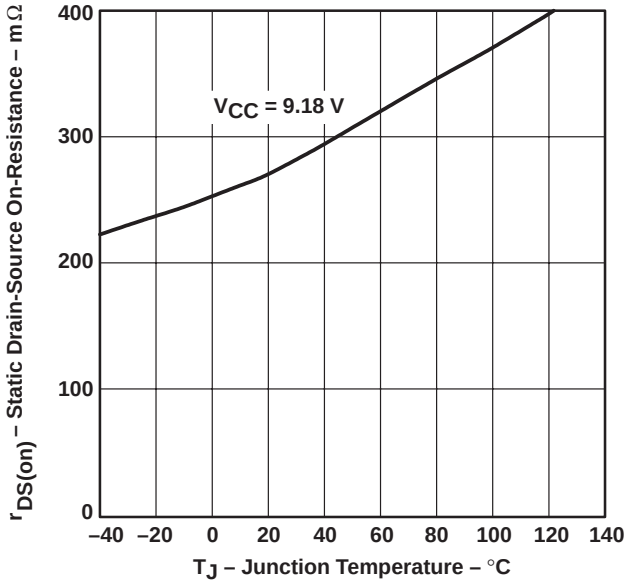


Figure 6

STATIC-DRAIN-SOURCE ON-RESISTANCE vs SUPPLY VOLTAGE

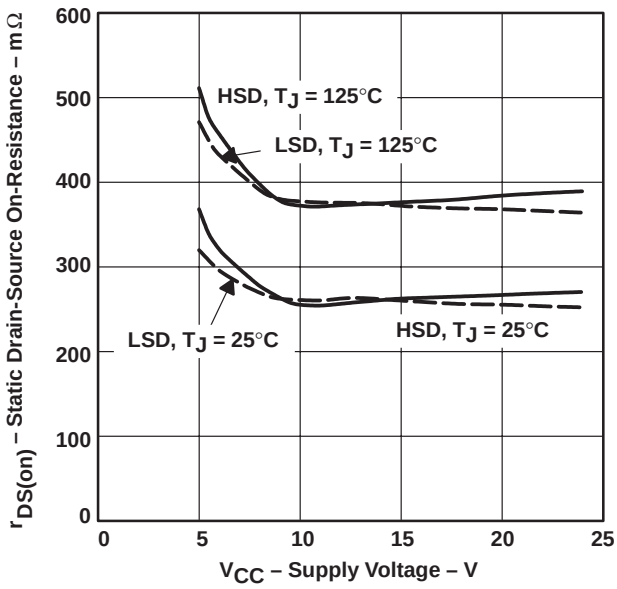


Figure 7

OUTPUT STAGE TURN-ON TIME vs JUNCTION TEMPERATURE

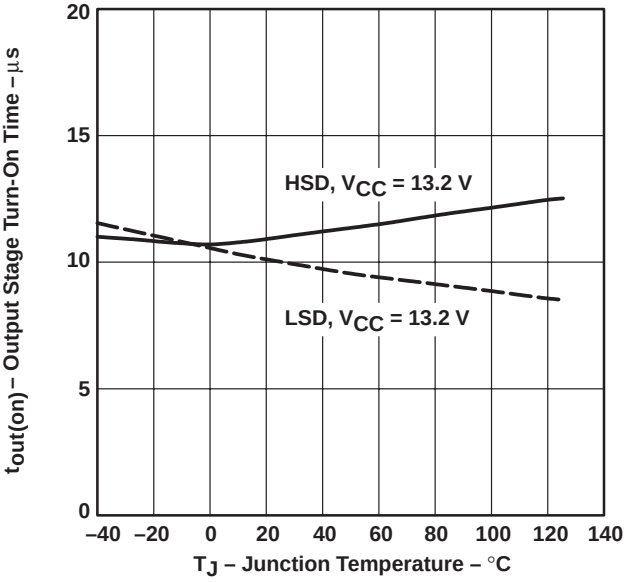


Figure 8

QUIESCENT BATTERY CURRENT vs JUNCTION TEMPERATURE

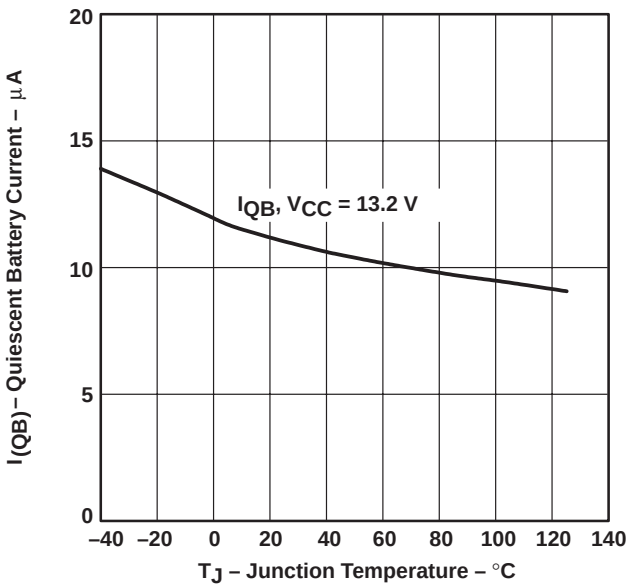
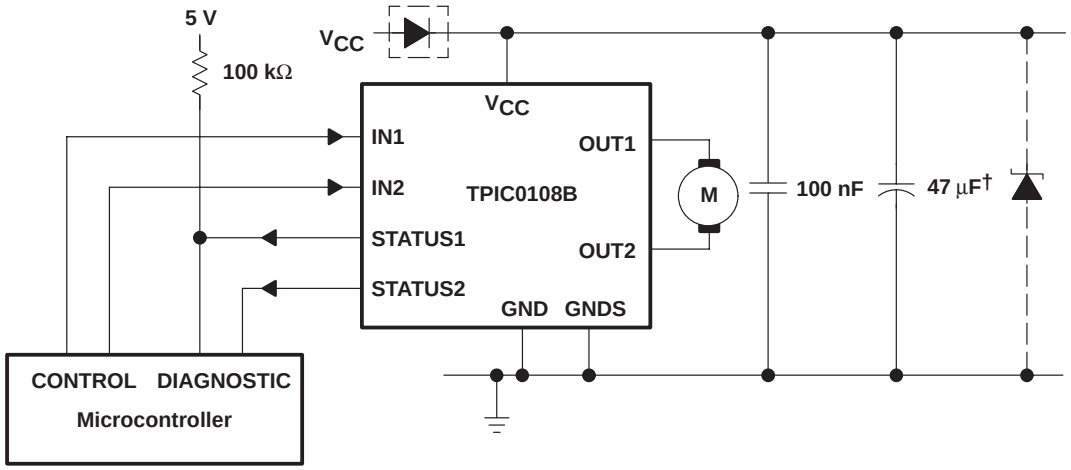


Figure 9

APPLICATION INFORMATION



† Necessary for isolating supply voltage or interruption (e.g., 47 μF).

NOTE: If a STATUS output is not connected to the appropriate microcontroller input, it shall remain unconnected.

recirculation current mode

When an inductive load (motor) is switched from one control mode to another, (i.e., forward to reverse) the TPIC0108B automatically enters a special recirculation current mode condition. This condition allows fast elimination of the recirculation currents caused by inductive switching. Once these currents have subsided to an acceptable level, the device automatically enters the requested state. This feature eliminates the need for either internally or externally connected free wheeling diodes and protects the TPIC0108B from damage due to high inductive voltage transients.

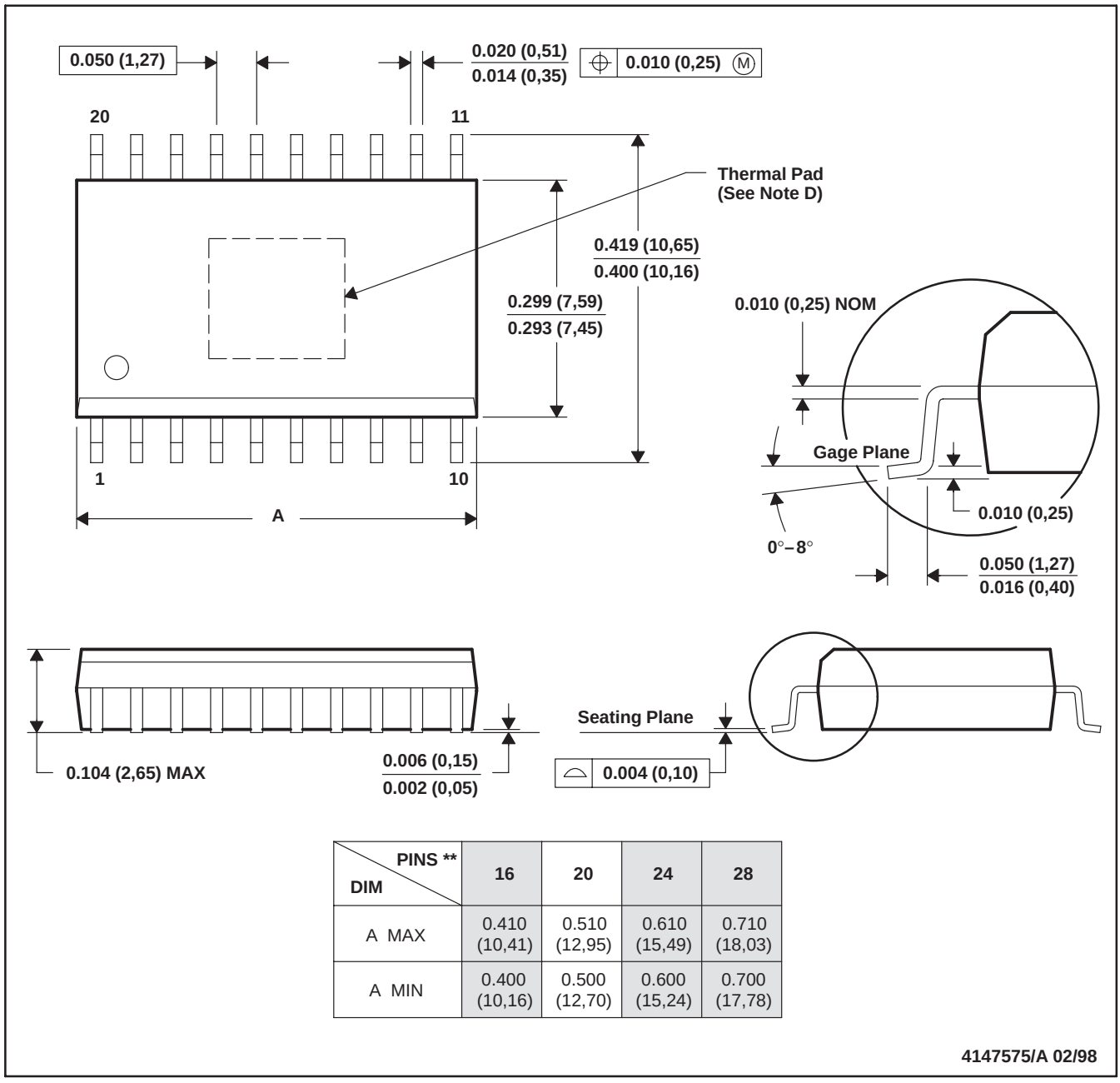
The recirculation current mode condition is triggered when the voltage at the HSD output voltage exceeds typically V_{CC} + 0.7 V. In this condition, a diode inherent in the HSD structure turns on. Simultaneously internal control circuitry turns on the opposite HSD, thus providing a current path for the recirculating currents.

Using TPIC0108B in PWM operation brake mode shall be applied before going into quiescent mode.

MECHANICAL DATA

DWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/A 02/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

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