TOSHIBA MOS MEMORY PRODUCTS

TMM2018AP-25, TMM2018AP-35, TMM2018AP-45

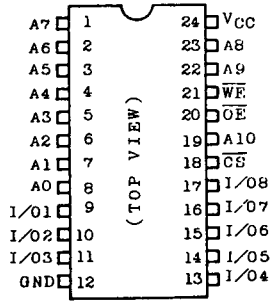
DESCRIPTION

The TMM2018AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2018AP is most suitable for use in cache memory and high speed storage.
The TMM2018AP is offered in a 24 pin standard plastic package with 0.3 inch width for high density assembly.
The TMM2018AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  - t_{ACC}=25ns: TMM2018AP-25
  - t_{ACC}=35ns: TMM2018AP-35
  - t_{ACC}=45ns: TMM2018AP-45
- Low power dissipation
  - I_{CC}=150mA: TMM2018AP-25
  - I_{CC}=135mA: TMM2018AP-35
  - I_{CC}=135mA: TMM2018AP-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature: $\overline{CS}$=V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pin standard plastic package, 0.3 inch width.

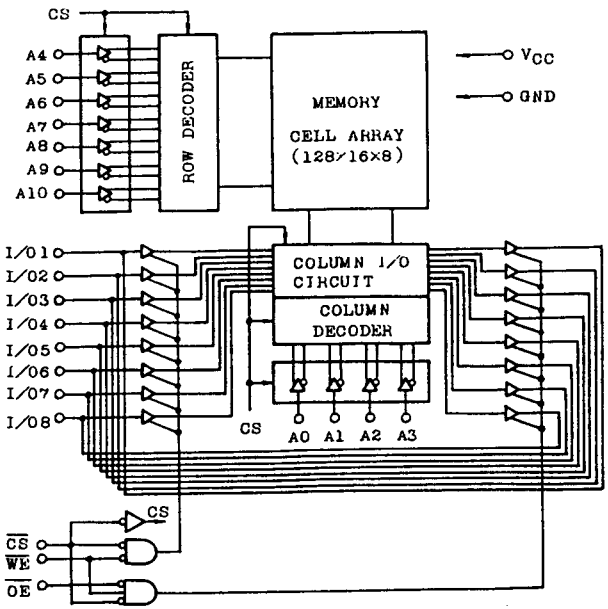
PIN CONNECTION



PIN NAMES

A0 ∿ A10	Address Inputs
I/O1 ∿ I/O8	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}	Input Voltage	-3.5 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5 ∿ 7.0	V
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	

* Pulse Width: 10ns, DC: -0.5V (MIN.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0 ∿ V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0 ∿ V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	150	mA
			-35	-	135	
			-45	-	135	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0 ∿ 5.5V		-	40	

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	
t_{CLZ}	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t_{CHZ}	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OHZ}	Output Disable to Output in High-Z	-	12	-	15	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t_{DS}	Data Set Up Time	12	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

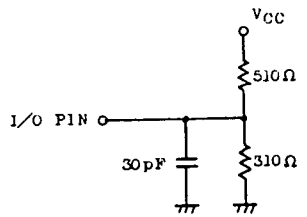
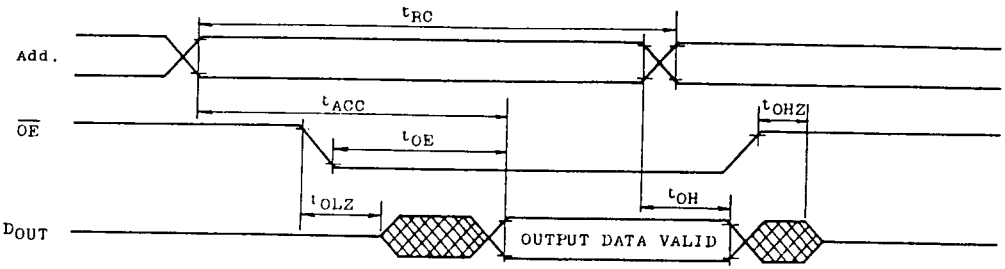


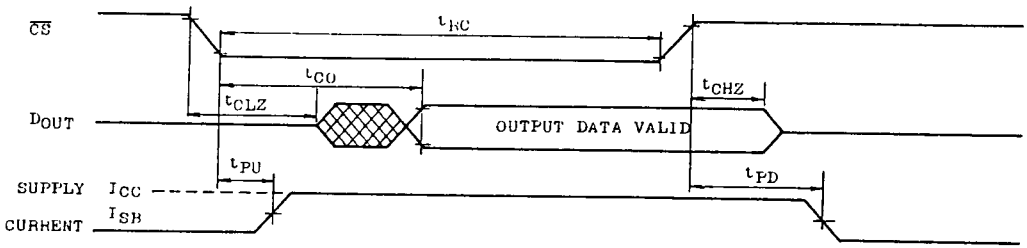
Fig.1 OUTPUT LOAD

TIMING WAVEFORMS

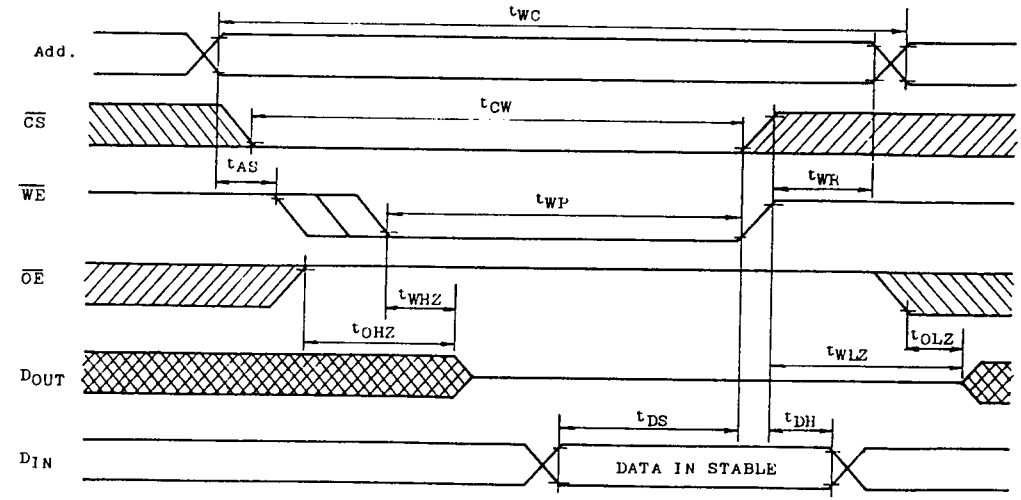
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



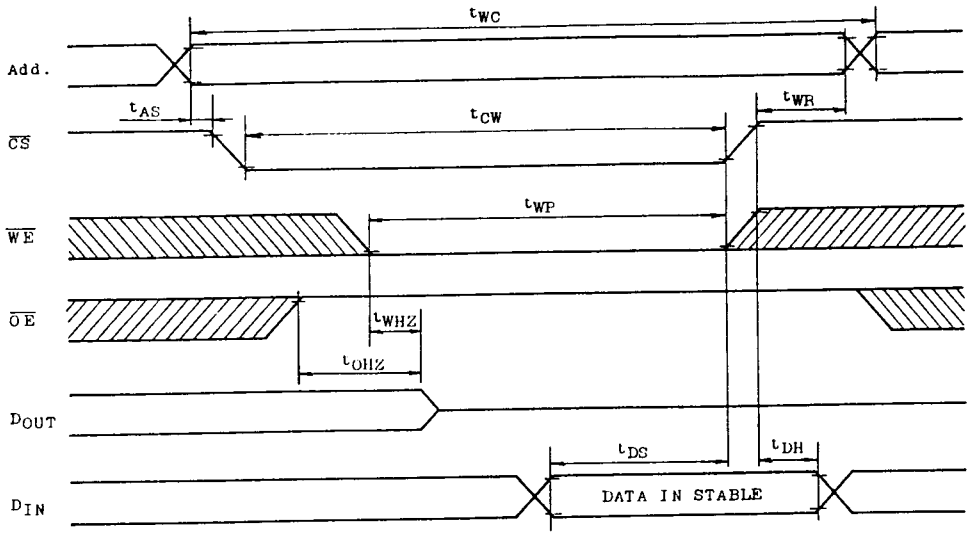
READ CYCLE 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



WRITE CYCLE 1.



WRITE CYCLE 2.

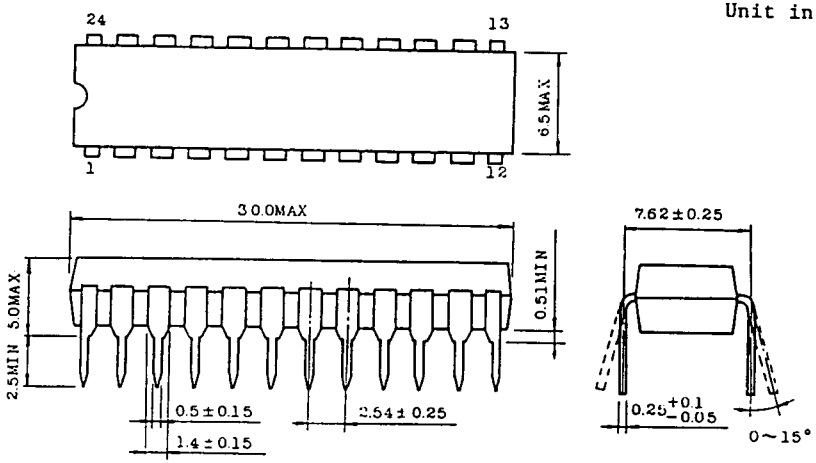


Note: 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.