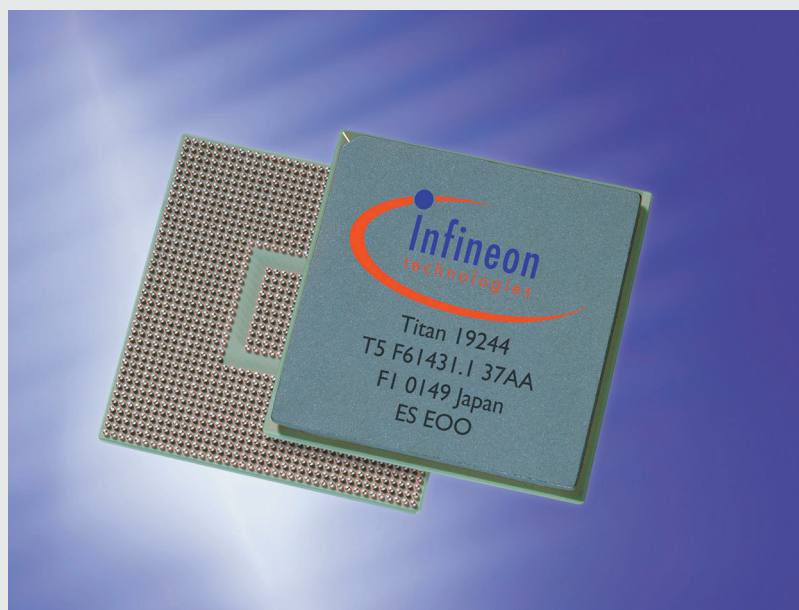


Semiconductor Solutions for High Speed Communications and Fiber Optic Applications

The Titan 19244 is a highly integrated single chip quad-port STS-192 SONET/SDH TDM framer and pointer processor device.

The Titan 19244 provides section, line, and path overhead processing for quad STS-192/STM-64. The framer itself takes four 10 Gbit/s (16-bit bus at 622 Mbit/s) channels on the line side interface, which is compliant with SFI-4 standard. The framer outputs four STS-192 SONET links on the system side. The system block diagram on the next page depicts a configuration for a quad OC-192 TDM framer and pointer processor application. The Titan 19244 is compliant with SONET/SDH standards ITU G.707, Bellcore GR-253, GR-1377, and ANSI T1.105.



Applications

- SONET/SDH Digital Cross-Connects
- SONET/SDH Terminal Multiplexers
- Long Haul and Metro Network ADM
- Dense Wave Division Multiplexers
- SONET/SDH Add/Drop Multiplexers
- Multi-Service Provisioning Platforms

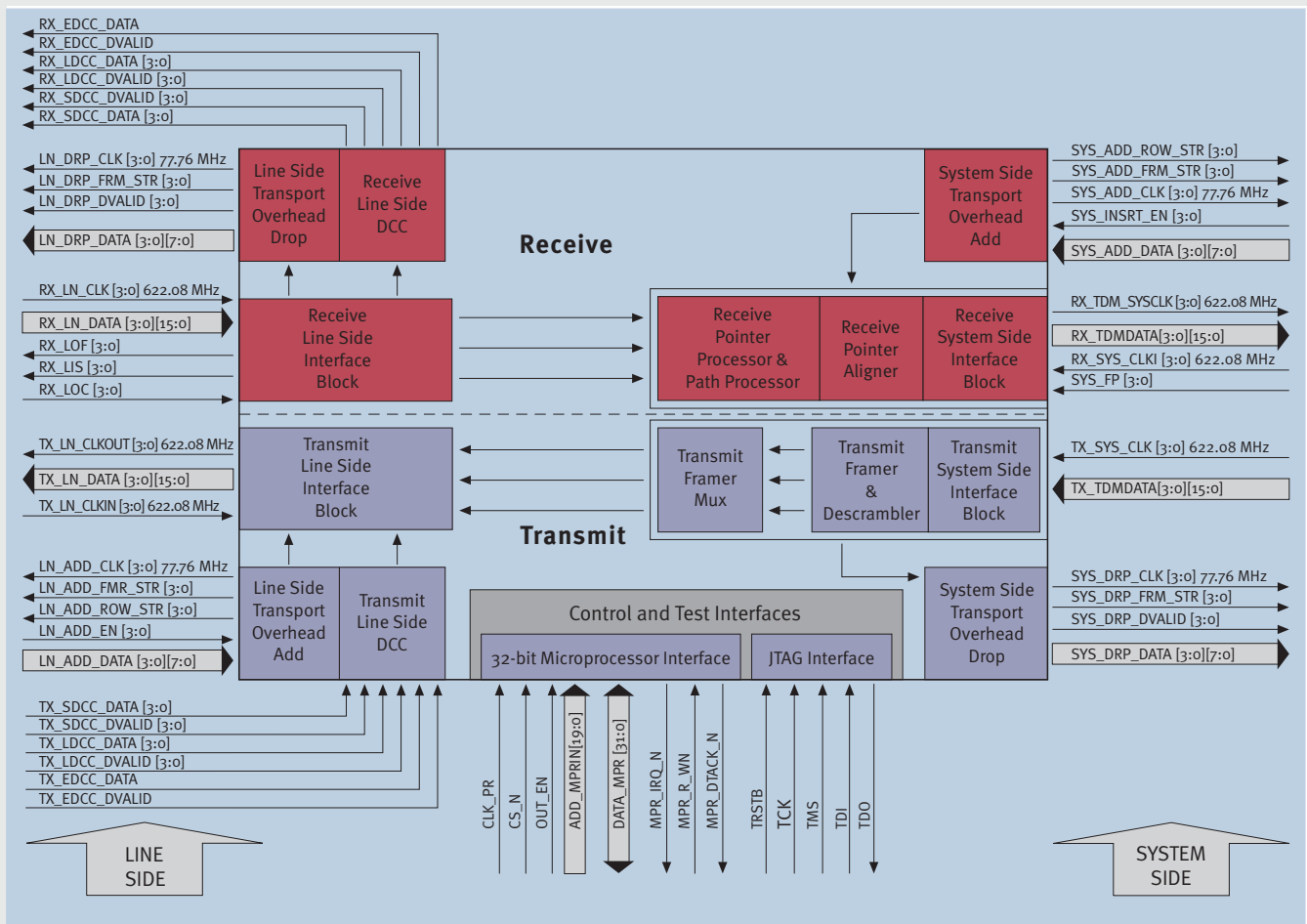
Features

- Quad-port STS-192/STM-64 SONET/SDH framer and pointer processor
- Terminates and generates section and line overhead layer for STS-192/STM-64
- Supports pointer processing at STS-1 granularity for STS-192/STM-64
- Supports flexible concatenation of payloads STS-2c, STS-3c, STS-4c, STS-5c, ... STS-12c, ... STS-48c, ... STS-192c
- Performs frame synchronous scrambling and de-scrambling of STS-192
- Drops/Inserts section and line overhead data bytes in the receive/transmit direction onto an external bus on both line side & system side
- Drops/Inserts Data Communications Channel (DCC) bytes D1-D3, D4-D12 on a serial link
- Provides hardware assistance for APS via K1 & K2 bytes. A separate APS interrupt port is provided per port for quad STS-192/STM-64
- Supports external timing mode
- Detects Severely Errored Framing (SEF), Loss Of Signal (LOS), Loss Of Frame (LOF), Loss Of Pointer (LOP), and Loss Of Clock (LOC)
- Monitors Line Alarm Indication Signal (AIS-L), Line Remote Defect Indication (RDI-L), and Line Remote Error Indication (REI-L)
- Handles section trace identifier (Jo) and path trace identifier (J1) processing
- Calculates, monitors, and counts the Section BIP-8 (B1), Line BIP-8N (B2), and Path BIP-8 (B3) errors
- Supports BER algorithm for Signal Fail (SF) and Signal Degrade (SD)
- Supports Terminal Loopback and Facility Loopback
- Supports Path REI error counting and Path RDI monitoring
- Supports detection of path unequipped and payload label mismatch (Signal Label Mismatch)
- Provides four 16-bit LVDS parallel buses operating at 622 Mbit/s on the line side for quad STS-192
- Compliant with SFI-4 standard on the Line Side Interface
- Provides four 16-bit LVDS parallel buses at 622 MHz (STS-192 SONET links) on the system side
- Supports IEEE1149.1 JTAG testing
- Supports a 32-bit MPC860 Motorola microprocessor interface
- Meets ITU G.707, GR-253, GR-1377, and ANSI T1.105
- 1413-pin flip-chip BGA package

T i t a n 1 9 2 4 4

SONET/SDH Framer & Pointer Processor





Block Diagram

Advantages

- Low power
- Small footprint
- High integration
- STS-768 support
- SONET/SDH support

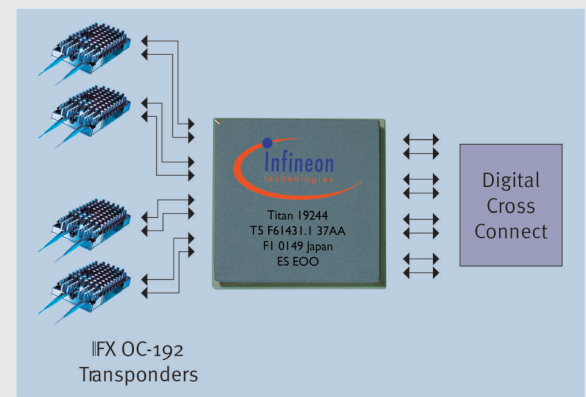
Standards

- GR-253
- GR-1377
- ITU G.707
- ANSI T1.105

Specifications

- 622 MHz LVDS I/Os
- 1413 ball FCBGA package
- Full-scan; JTAG; MemBIST
- 0 °C to 70 °C temperature range
- <12 W power requirement (typ.)

Note: Specifications subject to change without notice.



Application Example

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