FEATURES

- **1000MHz min. operating frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **800ps max. clock to output**
- **Single-ended outputs**
- **Asynchronous Master Reset**
- **Dual clocks**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E167**
- **Available in 28-pin PLCC package**

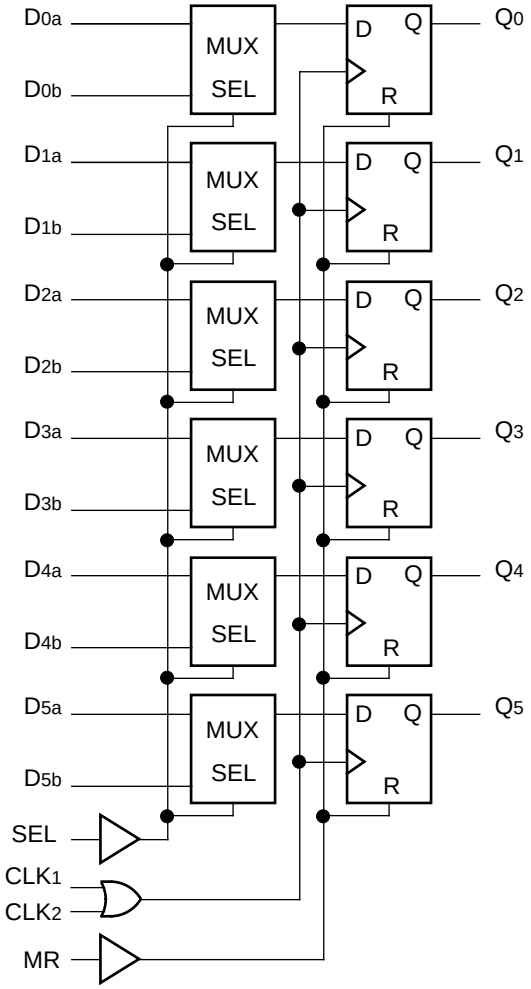
DESCRIPTION

The SY10/100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK_1, CLK_2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK_1 or CLK_2 (or both).

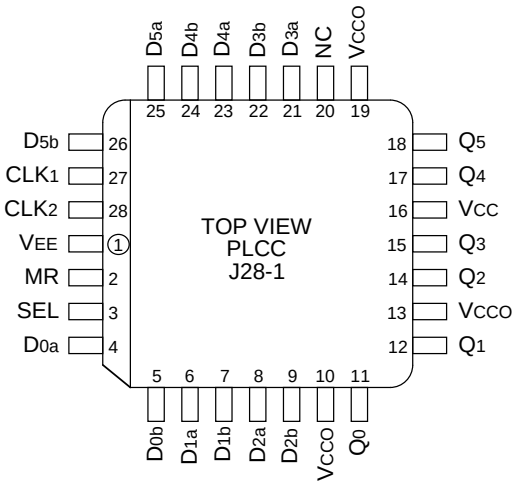
The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

When a logic HIGH is applied to the Master Reset (MR) signal, it operates asychronously to take all outputs Q to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0a}–D_{5a}	Input Data a
D_{0b}–D_{5b}	Input Data b
SEL	Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0–Q_5	Data Outputs
V_{CCO}	V_{CC} to Output

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Issue Date: February, 1998

TRUTH TABLE

SEL	Data
H	a
L	b

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	94	113	—	94	113	—	94	113		
	100E	—	94	113	—	94	113	—	108	130		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1000	1400	—	1000	1400	—	1000	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	450	650	800	450	650	800	450	650	800		
	MR	450	650	850	450	650	850	450	650	850		
t_S	Set-up Time										ps	—
	D	100	–50	—	100	–50	—	100	–50	—		
	SEL	275	125	—	275	125	—	275	125	—		
t_H	Hold Time										ps	—
	D	300	50	—	300	50	—	300	50	—		
	SEL	75	–125	—	75	–125	—	75	–125	—		
t_{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E167JC	J28-1	Commercial
SY10E167JCTR	J28-1	Commercial
SY100E167JC	J28-1	Commercial
SY100E167JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)