
TBB1002

Twin Build in Biasing Circuit MOS FET IC
VHF/UHF RF Amplifier

HITACHI

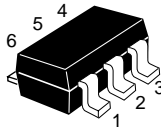
ADE-208-987F (Z)
7th. Edition
Dec. 2000

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at $C = 200 \text{ pF}$, $R_s = 0$ conditions.
- Provide mini mold packages; CMPAK-6

Outline

CMPAK-6



1. Gate-1(1)
2. Source
3. Drain(1)
4. Drain(2)
5. Gate-2
6. Gate-1(2)

- Notes:
1. Marking is "BM".
 2. TBB1002 is individual type number of HITACHI TWIN BBFET.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	P_{ch}^{*3}	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

Electrical Characteristics (Ta = 25°C)

The below specification are applicable for UHF unit (FET1)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5V$, $V_{G2S} = 4V$, $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5V$, $V_{G1S} = 5V$, $I_D = 100\mu A$
Drain current	$I_{D(op)}$	13	17	21	mA	$V_{DS} = 5V$, $V_{G1} = 5V$ $V_{G2S} = 4V$, $R_G = 100k\Omega$
Forward transfer admittance	$ y_{fs} $	21	26	31	mS	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$ $R_G = 100k\Omega$, $f = 1kHz$
Input capacitance	C_{iss}	1.4	1.8	2.2	pF	$V_{DS} = 5V$, $V_{G1} = 5V$
Output capacitance	C_{oss}	1.0	1.4	1.8	pF	$V_{G2S} = 4V$, $R_G = 100k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.02	0.04	pF	$f = 1MHz$
Power gain	PG	16	21	—	dB	$V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$ $R_G = 100k\Omega$, $f = 900MHz$ $Z_i = S11^*$, $Z_o = S22^*(\cdot PG)$
Noise figure	NF	—	1.7	2.5	dB	$Z_i = S11_{opt}$ ($\cdot NF$)

Electrical Characteristics (Ta = 25°C)

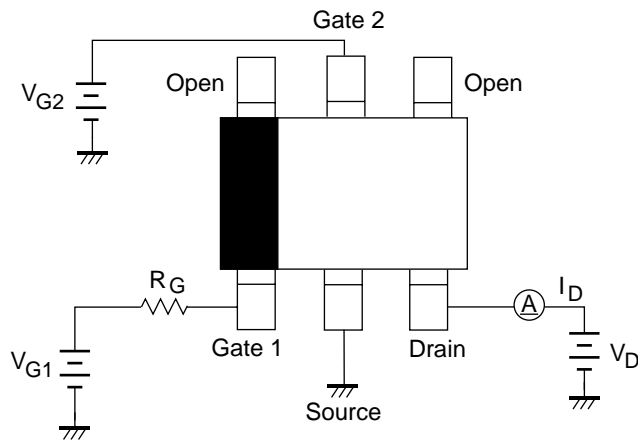
The below specification are applicable for VHF unit (FET2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5V$, $V_{G2S} = 4V$, $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5V$, $V_{G1S} = 5V$, $I_D = 100\mu A$
Drain current	$I_{D(op)}$	14	18	22	mA	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$
Forward transfer admittance	$ y_{fs} $	20	25	30	mS	$V_{DS} = 5V$, $V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 82k\Omega$, $f = 1kHz$
Input capacitance	C_{iss}	2.2	2.6	3.0	pF	$V_{DS} = 5V$, $V_{G1} = 5V$
Output capacitance	C_{oss}	1.2	1.6	2.0	pF	$V_{G2S} = 4V$, $R_G = 82k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.03	0.05	pF	$f = 1MHz$
Power gain	PG	22	27	—	dB	$V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$
Noise figure	NF	—	1.2	1.7	dB	$R_G = 82k\Omega$, $f = 200MHz$

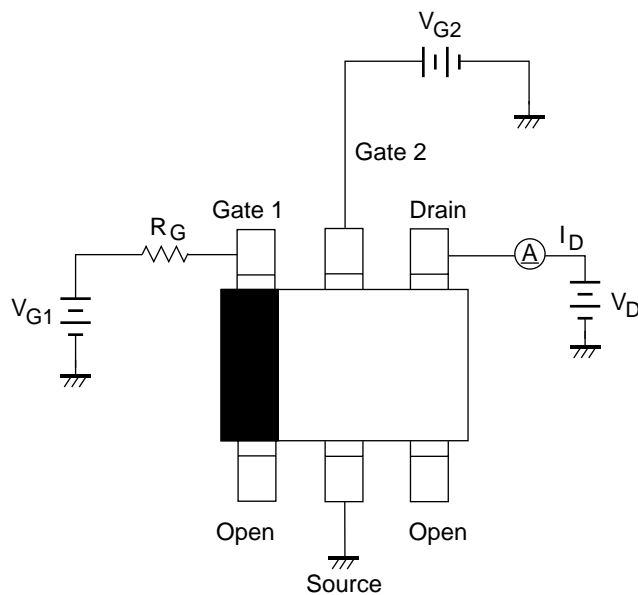
Test Circuits

- DC Biasing Circuit for Operating Characteristic Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF , PG)

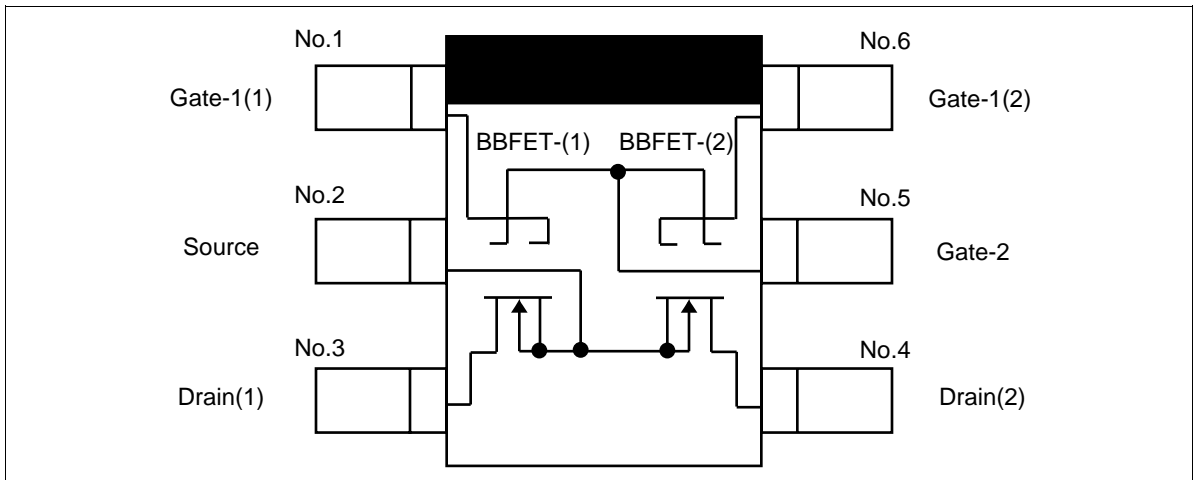
Measurment of FET1



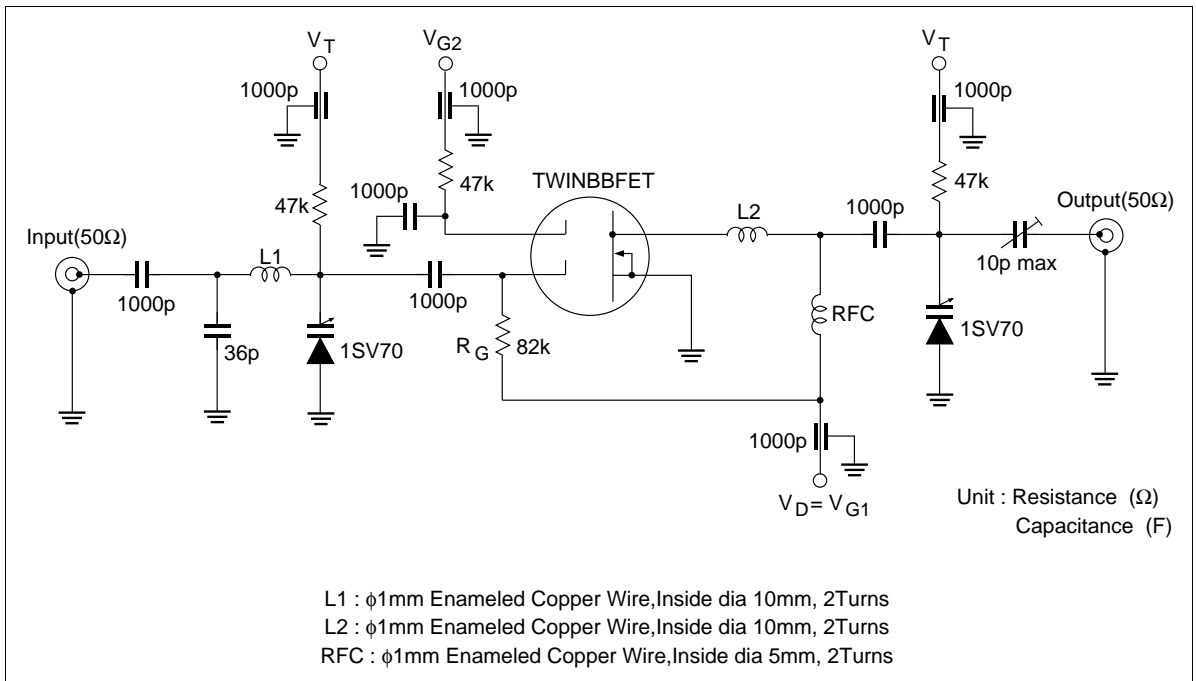
Measurment of FET2



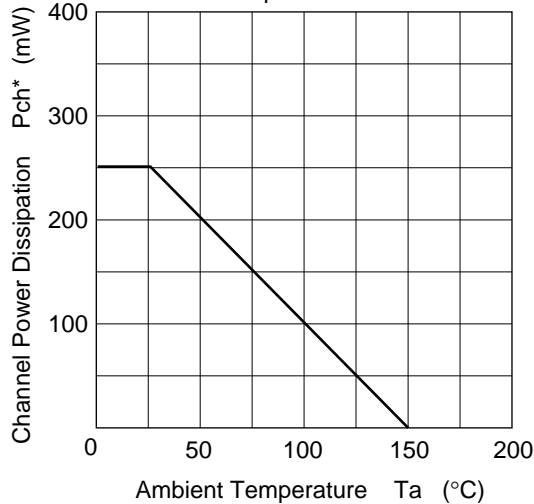
• Equivalent Circuit



• 200 MHz Power Gain, Noise Figure Test Circuit

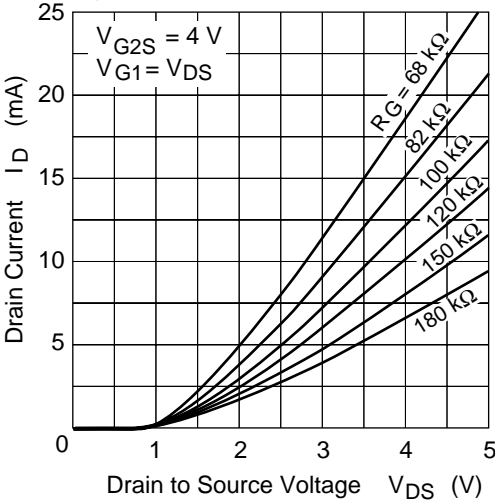


Maximum Channel Power
Dissipation Curve

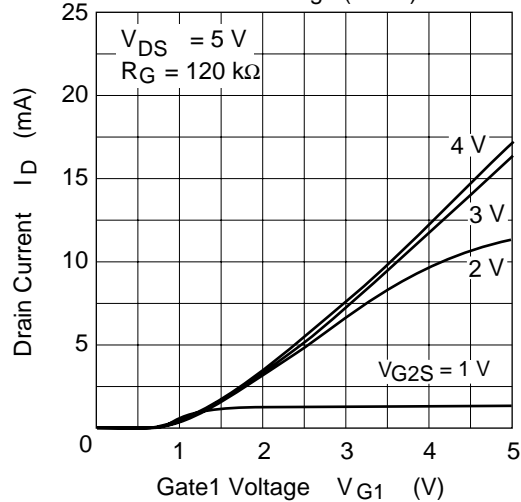


* Value on the glass epoxy board (49mm \times 38mm \times 1mm)

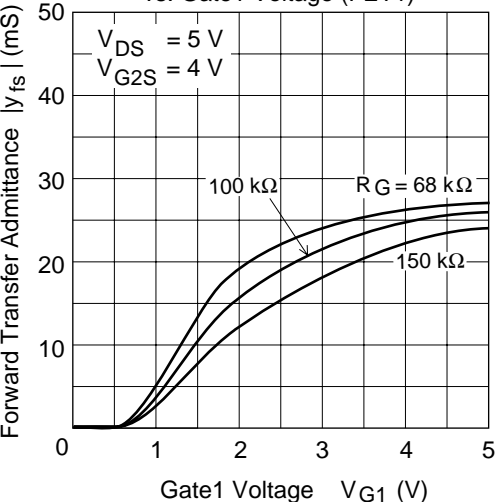
Typical Output Characteristics (FET1)



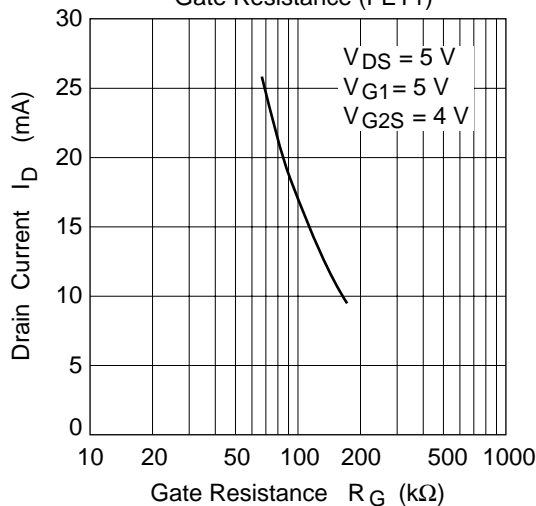
Drain Current vs.
Gate1 Voltage (FET1)



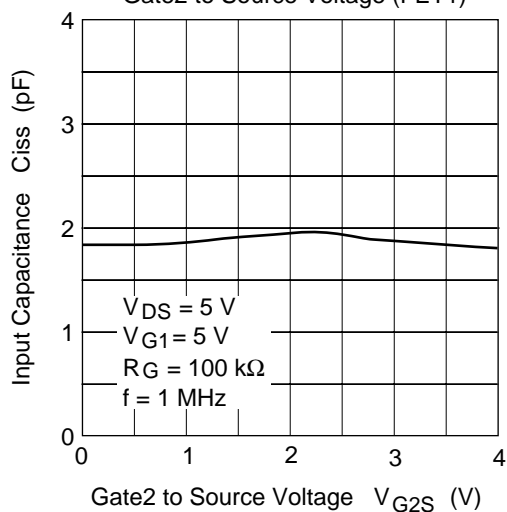
Forward Transfer Admittance
vs. Gate1 Voltage (FET1)



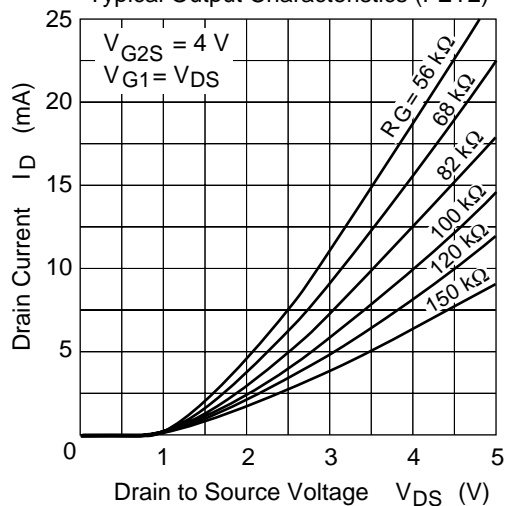
Drain Current vs.
Gate Resistance (FET1)



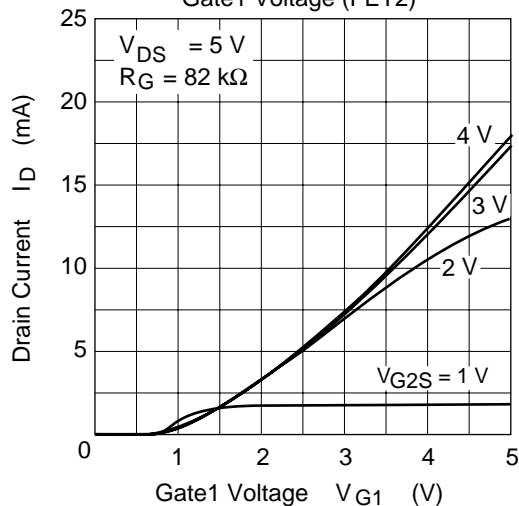
Input Capacitance vs.
Gate2 to Source Voltage (FET1)

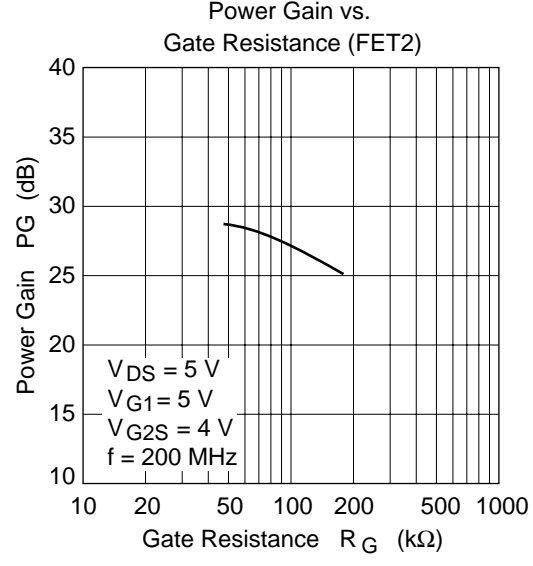
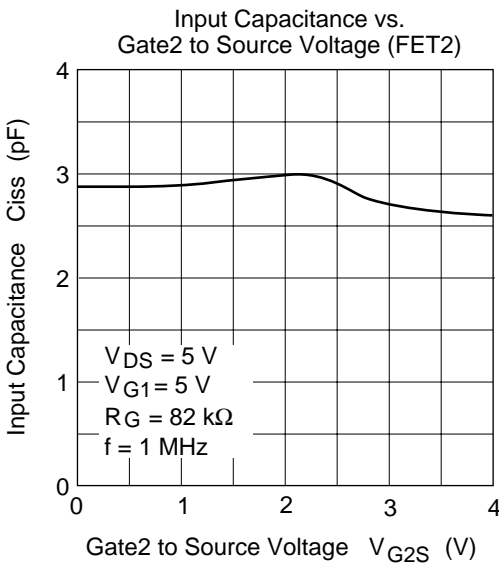
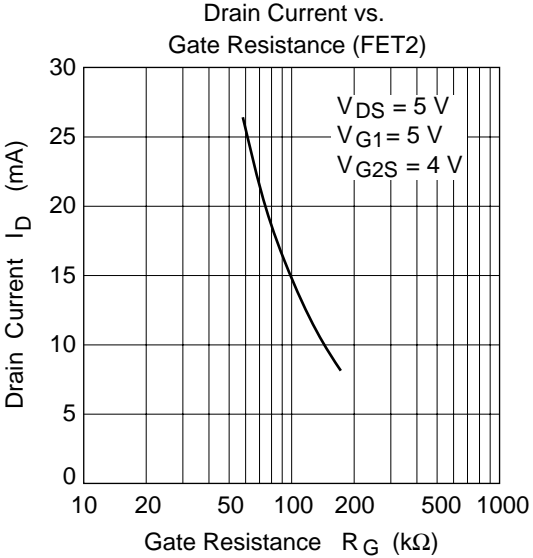
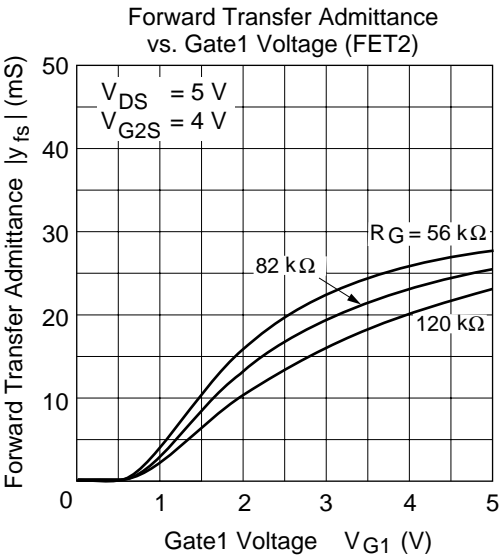


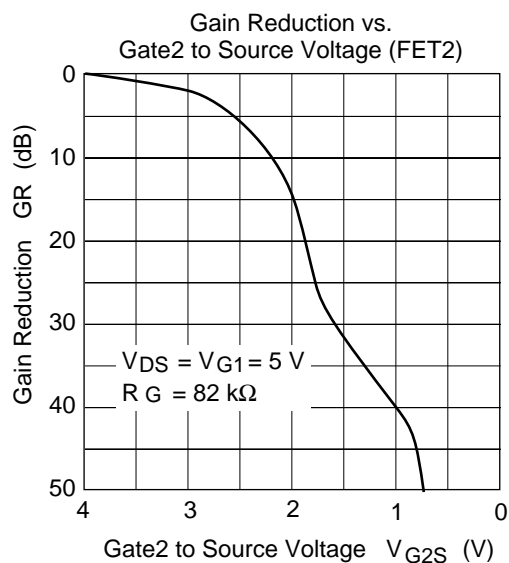
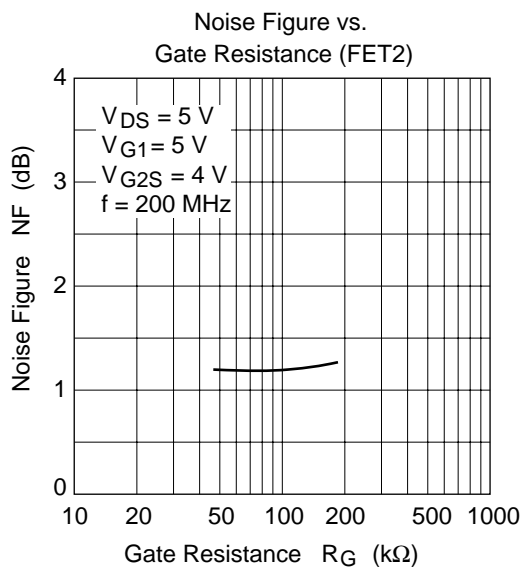
Typical Output Characteristics (FET2)



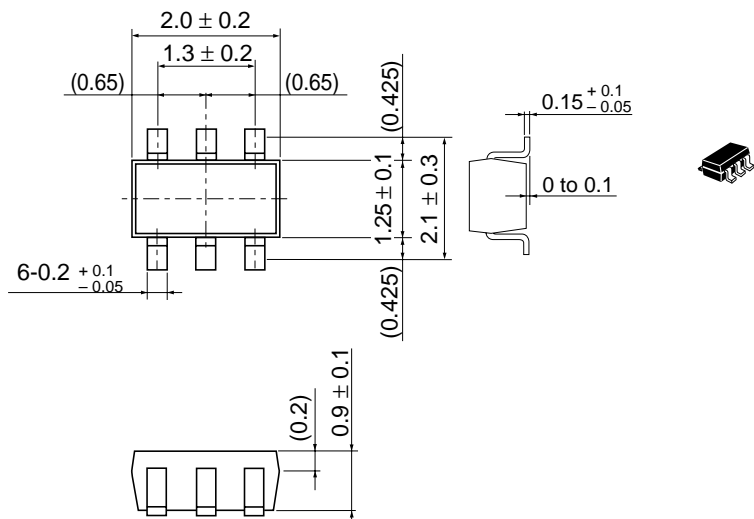
Drain Current vs.
Gate1 Voltage (FET2)







Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: http://semiconductor.hitachi.com/
	Europe	: http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax: <65>-538-6933/538-3877
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
URL: <http://www.hitachi.com.hk>

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