HM62G36256 Series

8M Synchronous Fast Static RAM
(256k-word × 36-bit)

HITACHI

ADE-203-1139 (Z)
Preliminary
Rev. 0.0
Jan. 10, 2000

Description

The HM62G36256 is a synchronous fast static RAM organized as 256-kword × 36-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 119-bump BGA.

Note: All power supply and ground pins must be connected for proper operation of the device.

Features

- Power supply: 3.3 V +10%, –5%
- Clock frequency: 200 MHz to 250 MHz
- Internal self-timed late write
- Byte write control (4 byte write selects, one for each 9-bit)
- Optional ×18 configuration
- HSTL compatible I/O
- Programmable impedance output drivers
- User selective input trip-point
- Differential, HSTL clock inputs
- Asynchronous $\overline{\mathrm{G}}$ output control
- Asynchronous sleep mode
- Limited set of boundary scan JTAG IEEE 1149.1 compatible
- Protocol: Single clock register-register mode

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

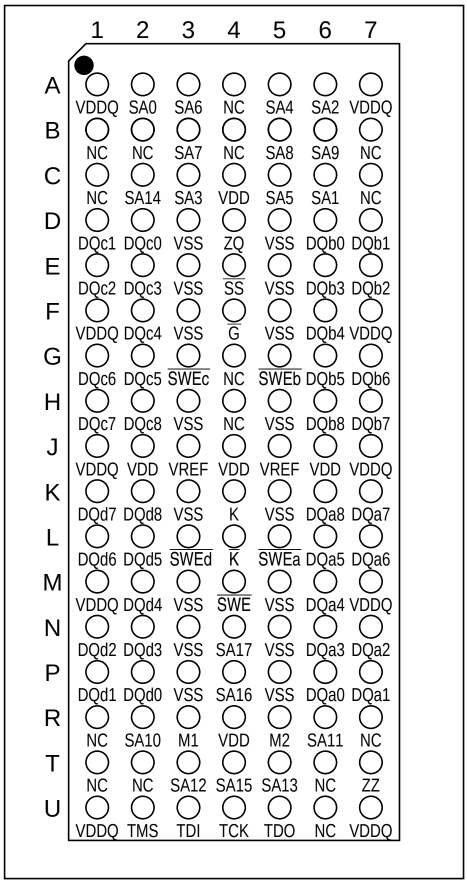
Hitachi semiconductor

Ordering Information

Type No.	Access time	Cycle time	Package
HM62G36256BP-4	2.1 ns	4.0 ns	119-bump 1. 27 mm
HM62G36256BP-5	2.5 ns	5.0 ns	14 mm × 22 mm BGA (BP-119A)

Pin Arrangement

119-bumps BGA



(Top view)

Pin Description

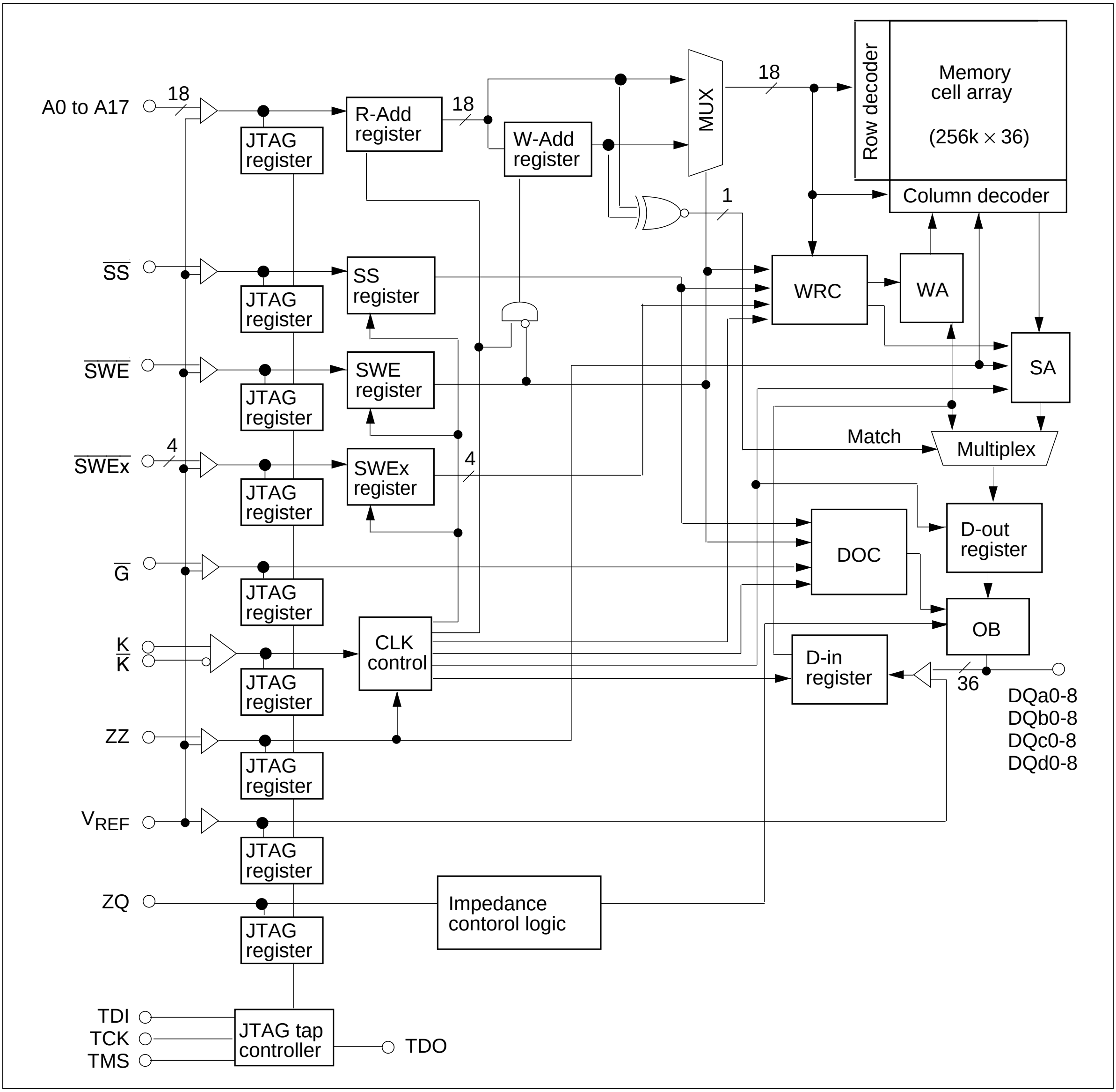
Name	I/O type	Descriptions	Notes
V_{DD}	Supply	Core power supply	
V_{SS}	Supply	Ground	
V_{DDQ}	Supply	Output power supply	
V_{REF}	Supply	Input reference: provides input reference voltage	
K	Input	Clock input. Active high.	
$\overline{K}$	Input	Clock input. Active low.	
$\overline{SS}$	Input	Synchronous chip select	
$\overline{SWE}$	Input	Synchronous write enable	
SAn	Input	Synchronous address input	n = 0, 1, 2...17
$\overline{SWEx}$	Input	Synchronous byte write enables	x = a, b, c, d
$\overline{G}$	Input	Asynchronous output enable	
ZZ	Input	Power down mode select	
ZQ	Input	Output impedance control	1
DQxn	I/O	Synchronous data input/output	x = a, b, c, d n = 0, 1, 2...8
M1, M2	Input	Output protocol mode select	
TMS	Input	Boundary scan test mode select	
TCK	Input	Boundary scan test clock	
TDI	Input	Boundary scan test data input	
TDO	Output	Boundary scan test data output	
NC	—	No connection	

M1	M2	Protocol	Notes
V_{SS}	V_{DD}	Synchronous register to register operation	2

Notes: 1. ZQ is to be connected to V_{SS} via a resistance RQ where 150 Ω ≤ RQ ≤ 300 Ω, if ZQ = V_{DDQ} or open, output buffer impedance will be maximum. A case of minimum impedance, it needs to connect over 120 Ω between ZQ and V_{SS}.

2. There is 1 protocol with mode pin. Mode control pins (M1, M2) are to be tied either V_{DD} or V_{SS} respectively. The state of the Mode control inputs must be set before power-up and must not change during device operation. Mode control inputs are not standard inputs and may not meet V_{IH} or V_{IL} specification. This SRAM is tested only in the synchronous register to register operation.

Block Diagram



Operation Table

ZZ	$\overline{\text{SS}}$	$\overline{\text{G}}$	$\overline{\text{SWE}}$	$\overline{\text{SWEa}}$	$\overline{\text{SWEb}}$	$\overline{\text{SWEc}}$	$\overline{\text{SWEd}}$	K	$\overline{\text{K}}$	Operation	DQ (n)	DQ (n + 1)
H	×	×	×	×	×	×	×	×	×	sleep mode	High-Z	High-Z
L	H	×	×	×	×	×	×	L-H	H-L	Dead (not selected)	×	High-Z
L	×	H	×	×	×	×	×	×	×	Dead (Dummy read)	High-Z	High-Z
L	L	L	H	×	×	×	×	L-H	H-L	Read	×	Dout (a,b,c,d)0-8
L	L	×	L	L	L	L	L	L-H	H-L	Write a, b, c, d byte	High-Z	Din (a,b,c,d)0-8
L	L	×	L	H	L	L	L	L-H	H-L	Write b, c, d byte	High-Z	Din (b,c,d)0-8
L	L	×	L	L	H	L	L	L-H	H-L	Write a, c, d byte	High-Z	Din (a,c,d)0-8
L	L	×	L	L	L	H	L	L-H	H-L	Write a, b, d byte	High-Z	Din (a,b,d)0-8
L	L	×	L	L	L	L	H	L-H	H-L	Write a, b, c byte	High-Z	Din (a,b,c)0-8
L	L	×	L	H	H	L	L	L-H	H-L	Write c, d byte	High-Z	Din (c,d)0-8
L	L	×	L	L	H	H	L	L-H	H-L	Write a, d byte	High-Z	Din (a,d)0-8
L	L	×	L	L	L	H	H	L-H	H-L	Write a, b byte	High-Z	Din (a,b)0-8
L	L	×	L	H	L	L	H	L-H	H-L	Write b, c byte	High-Z	Din (b,c)0-8
L	L	×	L	H	H	H	L	L-H	H-L	Write d byte	High-Z	Din (d)0-8
L	L	×	L	H	H	L	H	L-H	H-L	Write c byte	High-Z	Din (c)0-8
L	L	×	L	H	L	H	H	L-H	H-L	Write b byte	High-Z	Din (b)0-8
L	L	×	L	L	H	H	H	L-H	H-L	Write a byte	High-Z	Din (a)0-8

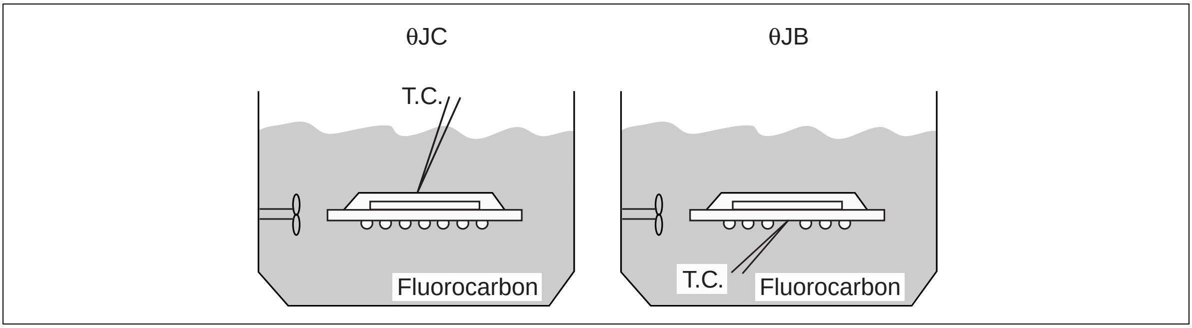
Notes: 1. × means don't care for synchronous inputs, and H or L for asynchronous inputs.
2. $\overline{\text{SWE}}$, $\overline{\text{SS}}$, $\overline{\text{SWEa}}$ to $\overline{\text{SWEd}}$, SA are sampled at the rising edge of K clock.
3. Although differential clock operation is implied, this SRAM will operate properly with one clock phase (either K or $\overline{\text{K}}$) tied to V_{REF}. Under such single-ended clock operation, all parameters specified within this document will be met.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Input voltage on any pin	V_{IN}	–0.5 to V_{DDQ} + 0.5	V	1, 4
Core supply voltage	V_{DD}	–0.5 to 3.9	V	1
Output supply voltage	V_{DDQ}	–0.5 to 2.2	V	1, 4
Operating temperature	T_{OPR}	0 to 70	°C	
Storage temperature	T_{STG}	–55 to 125	°C	
Junction temperature	Tj	110	°C	
Output short–circuit current	I_{OUT}	25	mA	
Latch up current	I_{LI}	200	mA	
Package junction to case thermal resistance	θJC	5	°C/W	5, 7
Package junction to ball thermal resistance	θJB	8	°C/W	6, 7

Notes: 1. All voltage is referred to V_{SS}.

2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The supply voltage application sequence need to be powered up in the following manner: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 3.9 V, whatever the instantaneous value of V_{DDQ}.
5. θJC is measured at the center of mold surface in fluorocarbon (See Figure “Definition of Measurement”).
6. θJB is measured on the center ball pad after removing the ball in fluorocarbon (See Figure “Definition of Measurement”).
7. These thermal resistance values have error of ± 5°C/W.



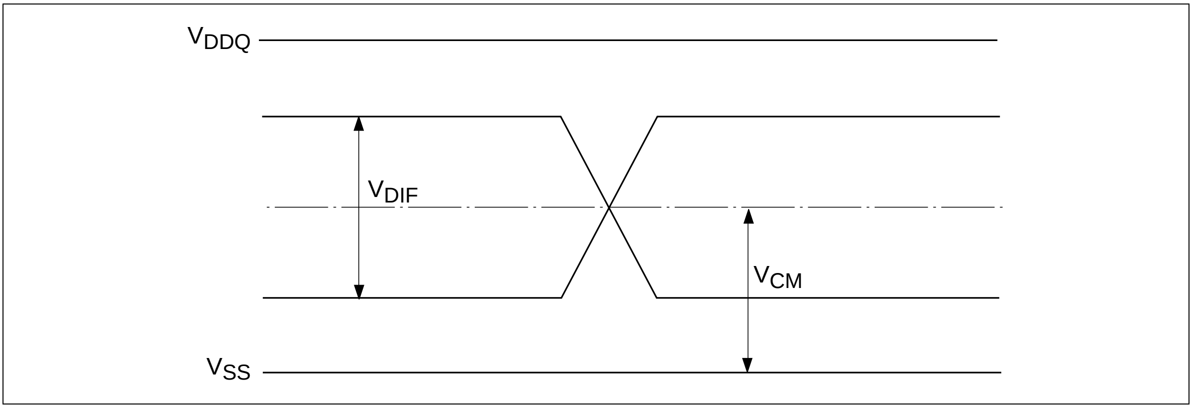
Definition of Measurement

Note: The following the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

DC Operating Conditions (Ta = 0 to 70°C [Tj max = 110°C])

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage (Core)	V_{DD}	3.135	3.30	3.63	V	
Supply voltage (I/O)	V_{DDQ}	1.4	1.5	1.6	V	
Supply voltage	V_{SS}	0	0	0	V	
Input reference voltage (I/O)	V_{REF}	0.65	0.75	0.90	V	1
Input high voltage	V_{IH}	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	4
Input low voltage	V_{IL}	–0.5	—	V_{REF} – 0.1	V	4
Clock differential voltage	V_{DIF}	0.1	—	V_{DDQ} + 0.3	V	2, 3
Clock common mode voltage	V_{CM}	0.55	—	0.90	V	3

Notes: 1. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.
2. Minimum differential input voltage required for differential input clock operation.
3. See following figure.
4. V_{REF} = 0.75 V (typ).



Differential Voltage/Common Mode Voltage

DC Characteristics (Ta = 0 to 70°C, [Tj max = 110°C], V_{DD} = 3.3 V +10%, –5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input leakage current	I_{LI}	—	—	2	µA	1
Output leakage current	I_{LO}	—	—	5	µA	2
Standby current	I_{SBZZ}	—	—	100	mA	3
V_{DD} operating current, excluding output drivers 4 ns cycle	I_{DD4}	—	—	700	mA	4
V_{DD} operating current, excluding output drivers 5 ns cycle	I_{DD5}	—	—	650	mA	4
Quiescent active power supply current	I_{DD2}	—	—	200	mA	5
Output low voltage	V_{OL}	V_{SS}	—	V_{SS} + 0.4	V	6
Output high voltage	V_{OH}	V_{DDQ} – 0.4	—	V_{DDQ}	V	6
ZQ pin connect resistance	RQ	150	250	300	Ω	
Output low current	I_{OL}	(V_{DDQ}/2)/[(RQ/5)–15%]	—	(V_{DDQ}/2)/[(RQ/5)+15%]	mA	7, 9
Output high current	I_{OH}	(V_{DDQ}/2)/[(RQ/5–4)+15%]	—	(V_{DDQ}/2)/[(RQ/5–4)–15%]	mA	8, 9

Notes:
1. 0 ≤ Vin ≤ V_{DDQ} for all input pins (except V_{REF}, ZQ, M1, M2 pin).
2. 0 ≤ Vout ≤ V_{DDQ}, DQ in High-Z.
3. All inputs (except clock) are held at either V_{IH} or V_{IL}, ZZ is held at V_{IH}, Iout = 0 mA, Spec is guaranteed at 75°C junction temperature.
4. Iout = 0 mA, read 50%/write 50%, V_{DD} = V_{DD} max, V_{IN} = V_{IH} or V_{IL}, Frequency = minimum cycle.
5. Iout = 0 mA, read 50%/write 50%, V_{DD} = V_{DD} max, V_{IN} = V_{IH} or V_{IL}, Frequency = 3 MHz.
6. Minimum impedance push pull output buffer mode, I_{OH} = –6 mA, I_{OL} = 6 mA.
7. Measured at V_{OL} = 1/2 V_{DDQ}.
8. Measured at V_{OH} = 1/2 V_{DDQ}.
9. Output buffer impedance can be programmed by terminating the ZQ pin to V_{SS} through a precision resister (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 150 Ω and 300 Ω. If the status of ZQ pin is open, output impedance is maximum. Maximum impedance occurs with ZQ connected to V_{DDQ}. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K clock to guarantee the proper update. At power-up, the output impedance defaults to minimum impedance. It will take 2048 cycles for the impedance to be completely updated if the programmed impedance is much higher than minimum impedance.

Capacitance (Ta = 25°C, f = 1 MHz)

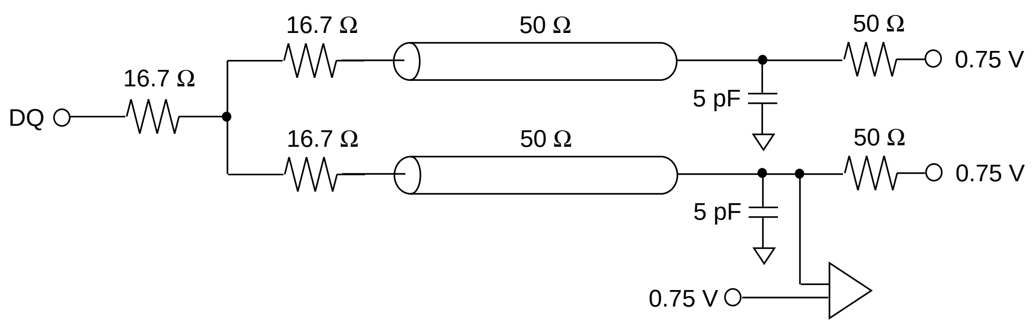
Parameter	Symbol	Min	Max	Unit	Note
Input capacitance (SAn, $\overline{SS}$, $\overline{SWE}$, $\overline{SWEx}$)	C_{IN}	—	4	pF	1
Input capacitance (K, $\overline{K}$, $\overline{G}$)	C_{CLK}	—	7	pF	1
Input/Output capacitance (DQxn)	C_{IO}	—	5	pF	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, [Tj max = 110°C], V_{DD} = 3.3 V +10%, –5%)

Test Conditions

- Input pulse levels (K, $\overline{K}$): V_{DIF} = 0.75 V, V_{CM} = 0.75 V
- Input timing reference level (K, $\overline{K}$): Differential cross point
- Input pulse levels (except K, $\overline{K}$): V_{IL} = 0.25 V, V_{IH} = 1.25 V
- Input and output timing reference levels (except K, $\overline{K}$): V_{REF} = 0.75 V
- Input rise and fall time: 0.5 ns (10% to 90%)
- Measurement condition: the minimum impedance push pull output buffer mode, I_{OH} = –6 mA, I_{OL} = 6 mA
- Output driver supply voltage: V_{DDQ} = 1.5 V
- Output load: See figure



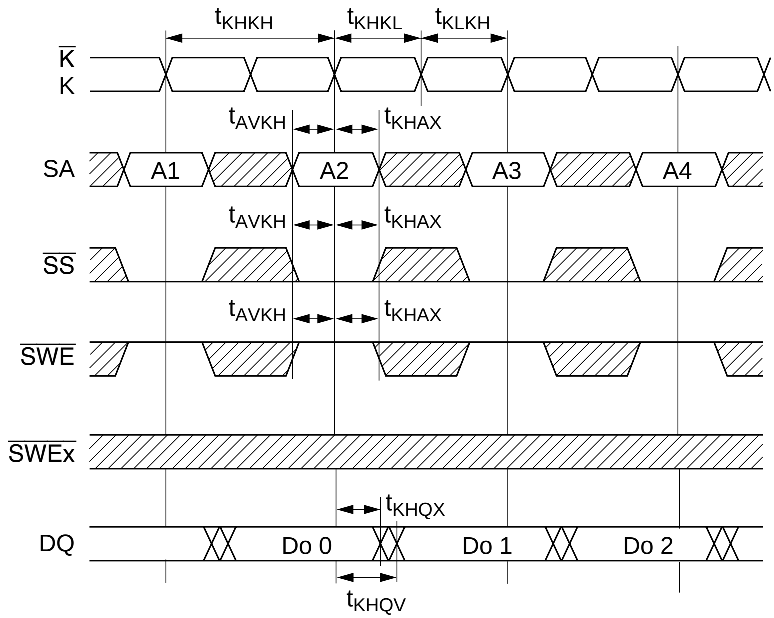
Single Differential Clock Register-Register Mode (M1 = V_{SS}, M2 = V_{DD})

		HM62G36256					
		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CK clock cycle time	t_{KHKH}	4.0	—	5.0	—	ns	
CK clock high width	t_{KHKL}	1.5	—	1.5	—	ns	
CK clock low width	t_{KLKH}	1.5	—	1.5	—	ns	
Address setup time	t_{AVKH}	0.5	—	0.5	—	ns	
Data setup time	t_{DVKH}	0.5	—	0.5	—	ns	
Address hold time	t_{KHAX}	0.75	—	1.0	—	ns	1
Data hold time	t_{KHDX}	0.75	—	1.0	—	ns	1
Clock high to output valid	t_{KHQV}	—	2.1	—	2.5	ns	2
Clock high to output hold	t_{KHQX}	0.5	—	0.5	—	ns	2
Clock high to output valid ($\overline{SS}$ control)	t_{KHQX2}	—	2.1	—	2.5	ns	2, 5
Clock high to output High-Z	t_{KHQZ}	—	2.5	—	3.0	ns	2, 3
Output enable low to output Low-Z	t_{GLQX}	0.5	—	0.5	—	ns	2, 5
Output enable low to output valid	t_{GLQV}	—	2.5	—	2.5	ns	2, 3
Output enable low to output High-Z	t_{GHQZ}	—	2.5	—	2.5	ns	2, 3
Sleep mode recovery time	t_{ZZR}	10.0	—	10.0	—	ns	6
Sleep mode enable time	t_{ZZE}	—	10.0	—	10.0	ns	2, 3, 6

Notes:
1. Guaranteed by design.
2. Refer to the Test Conditions.
3. Transitions are measured at start point of output high impedance from output low impedance.
4. Output driver impedance updates during High-Z.
5. Transitions are measured ±50 mV from steady state voltage.
6. When ZZ is switching, clock input K must be at same logic levels for reliable operation.

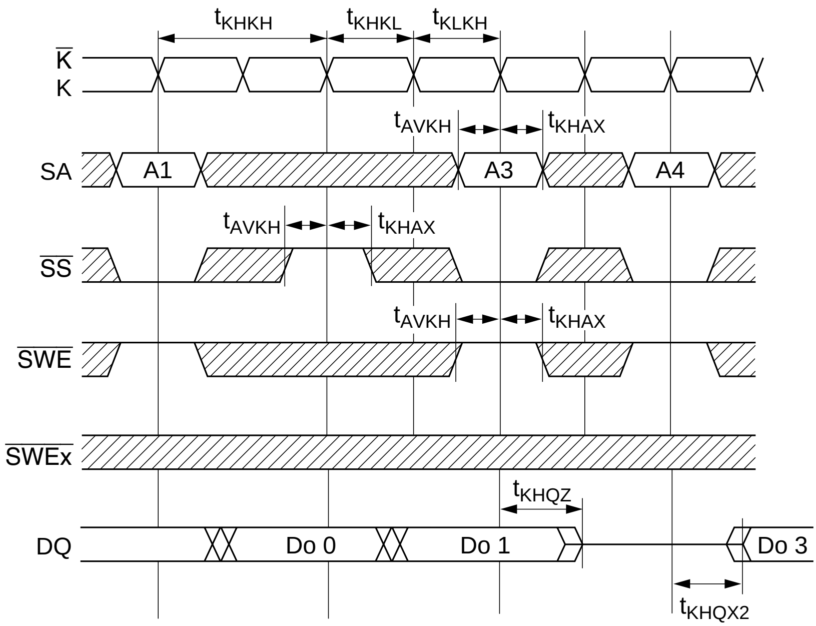
Timing Waveforms

Read Cycle-1



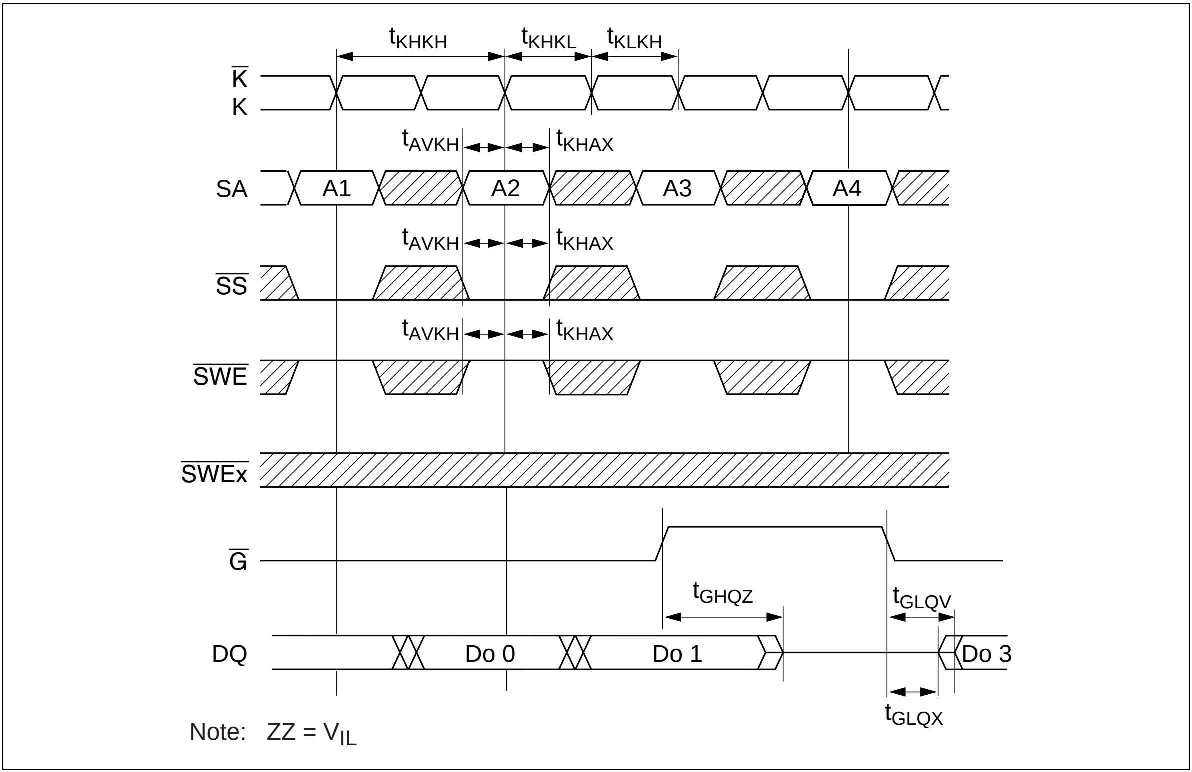
Note: $\overline{G}$, ZZ = V_{IL}

Read Cycle-2 ($\overline{SS}$ Controlled)

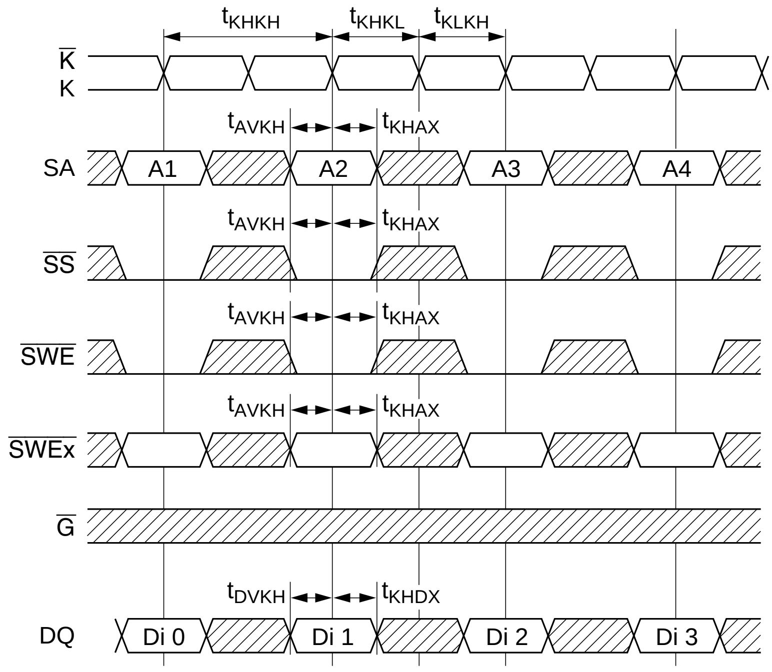


Note: $\overline{G}$, ZZ = V_{IL}

Read Cycle-3 ($\overline{G}$ Controlled)

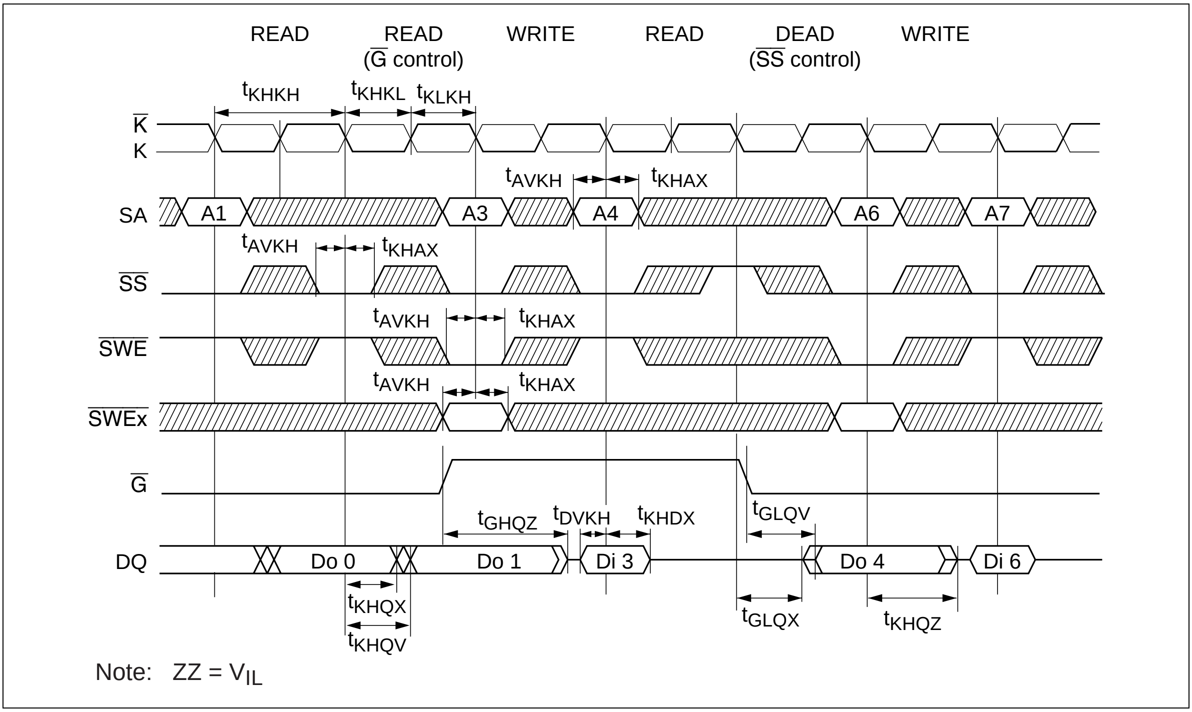


Write Cycle

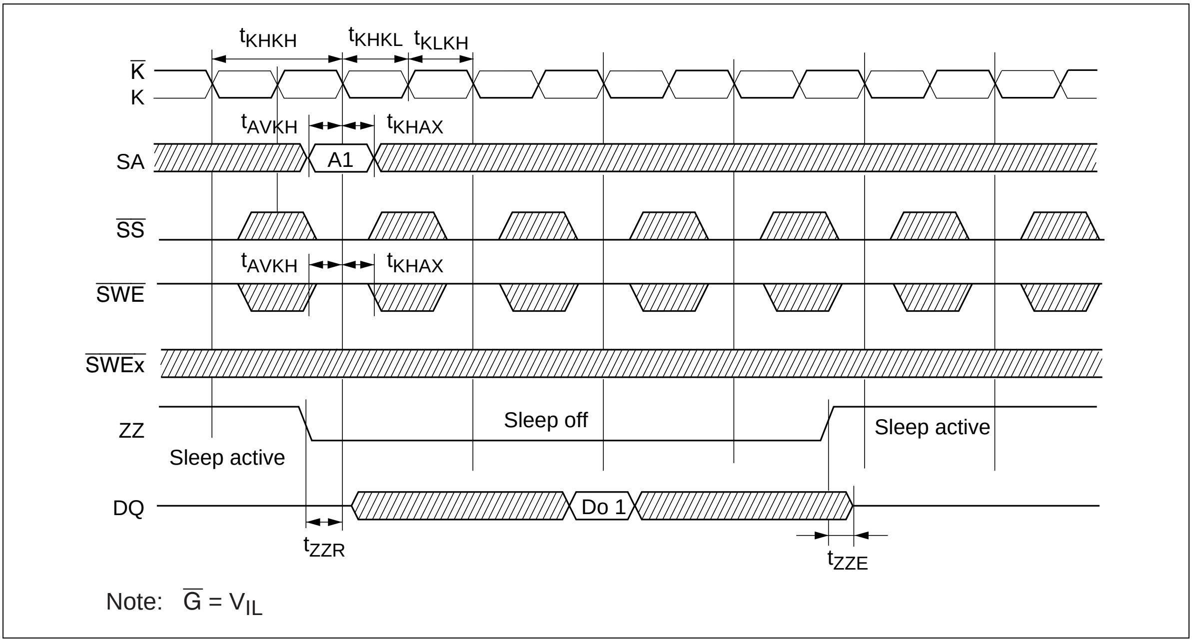


Note: ZZ = V_{IL}

Read-Write Cycle



ZZ Control



Boundary Scan Test Access Port Operations

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance The HM62Gxx series contains a TAP controller. Instruction register, Boundary scans register, Bypass register and ID register.

Test Access Port Pins

Symbol I/O	Name
TCK	Test clock
TMS	Test mode select
TDI	Test data in
TDO	Test data out

Note: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1.
To disable the TAP, TCK must be connected to V_{SS}. TDO should be left unconnected.
To test Boundary scan, ZZ pin need to be kept below V_{REF} – 0.4 V.

TAP DC Operating Conditions (Ta = 0 to 70°C, [Tj max = 110°C])

Parameter	Symbol	Min	Max	Unit	Notes
Boundary scan input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
Boundary scan input low voltage	V_{IL}	–0.5	0.8	V	
Boundary scan input leakage current	I_{LI}	–2	2	µA	1
Boundary scan output low voltage	V_{OL}	—	0.4	V	2
Boundary scan output high voltage	V_{OH}	2.4	—	V	3

Notes: 1. $0 \le Vin \le V_{DD}$ for all logic input pin.
2. I_{OL} = 8 mA.
3. I_{OH} = –8 mA.

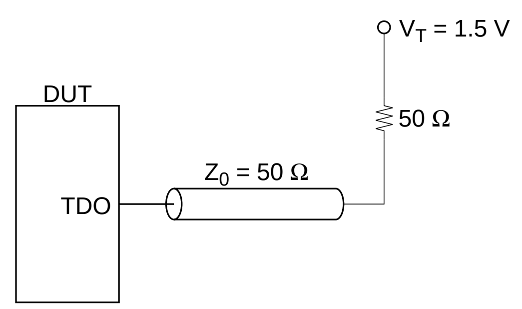
TAP AC Characteristics (Ta = 0 to 70°C, [Tj max = 110°C])

Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	t_{THTH}	67	—	ns	
Test clock high pulse width	t_{THTL}	30	—	ns	
Test clock low pulse width	t_{TLTH}	30	—	ns	
Test mode select setup	t_{MVTH}	10	—	ns	
Test mode select hold	t_{THMX}	10	—	ns	
Capture setup	t_{CS}	10	—	ns	1
Capture hold	t_{CH}	10	—	ns	1
TDI valid to TCK high	t_{DVTH}	10	—	ns	
TCK high to TDI don't care	t_{THDX}	10	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	ns	
TCK low to TDO valid	t_{TLQV}	—	20	ns	

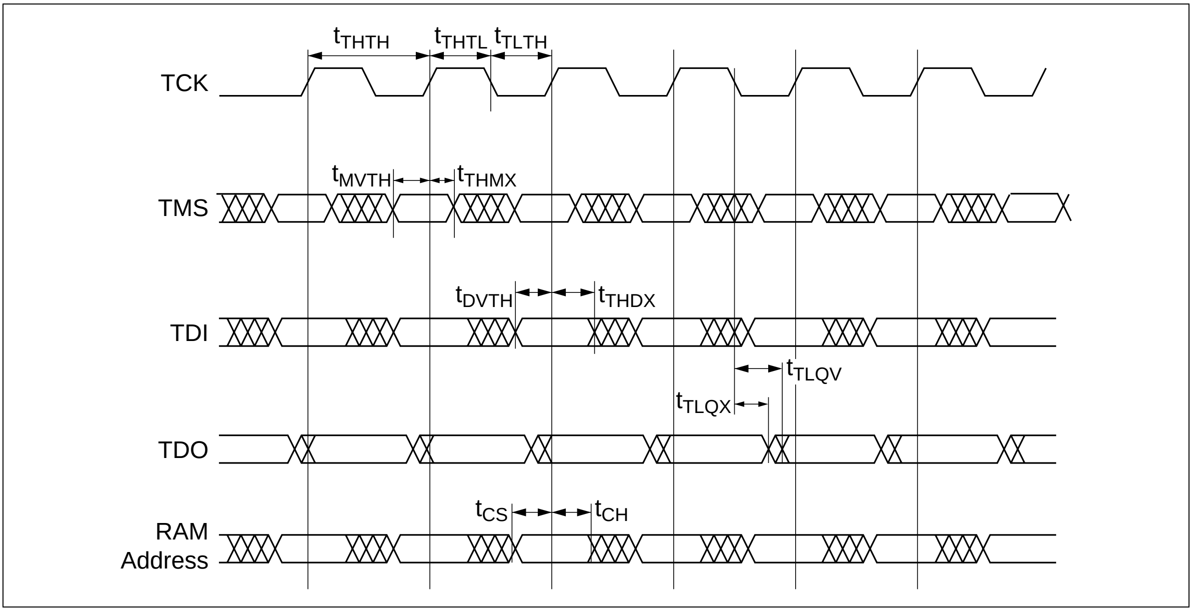
Note: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Test Conditions

- Input pulse levels: 0 to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 2 ns (10% to 90%) (typ)
- Output Load: See figure



TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol	Note
Instruction register	3 bits	IR [0;2]	
Bypass register	1 bit	BP	
ID register	32 bits	ID [0;31]	
Boundary scan register	70 bits	BS [1;70]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order

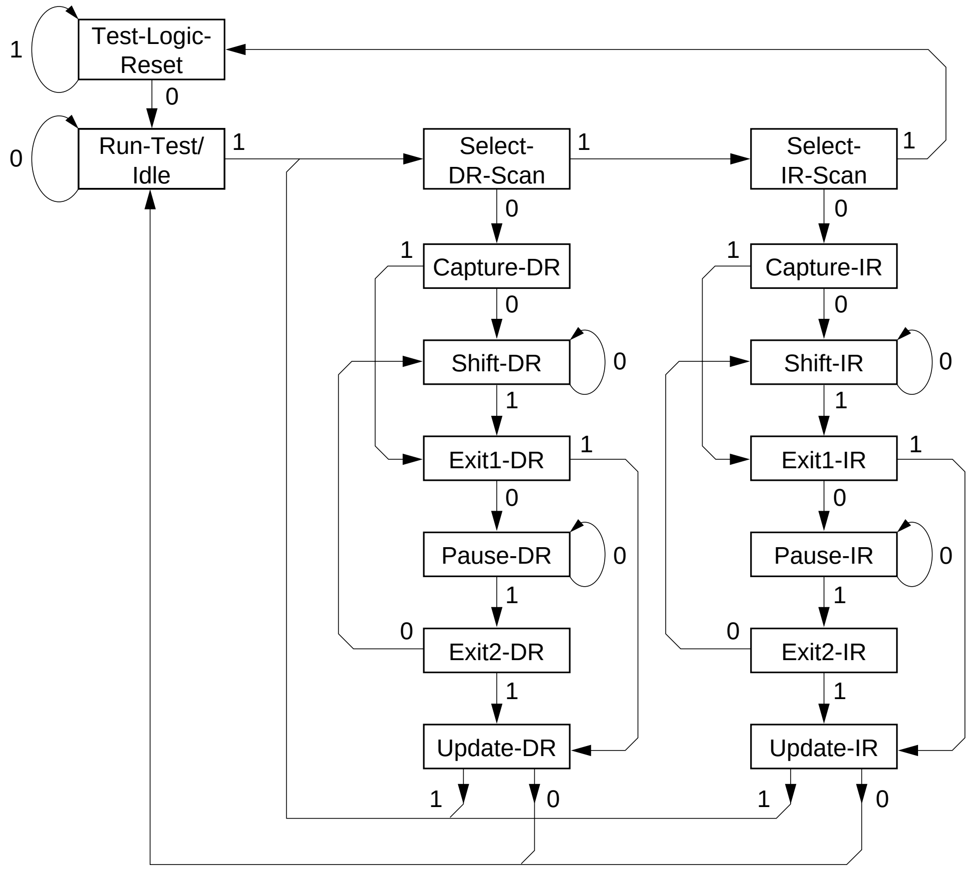
Bit No.	Bump ID	Signal name	Bit No.	Bump ID	Signal name
1	5R	M2	36	3B	SA7
2	4P	SA16	37	2B	NC
3	4T	SA15	38	3A	SA6
4	6R	SA11	39	3C	SA3
5	5T	SA13	40	2C	SA14
6	7T	ZZ	41	2A	SA0
7	6P	DQa0	42	2D	DQc0
8	7P	DQa1	43	1D	DQc1
9	6N	DQa3	44	2E	DQc3
10	7N	DQa2	45	1E	DQc2
11	6M	DQa4	46	2F	DQc4
12	6L	DQa5	47	2G	DQc5
13	7L	DQa6	48	1G	DQc6
14	6K	DQa8	49	2H	DQc8
15	7K	DQa7	50	1H	DQc7
16	5L	$\overline{\text{SWEa}}$	51	3G	$\overline{\text{SWEc}}$
17	4L	$\overline{\text{K}}$	52	4D	ZQ
18	4K	K	53	4E	$\overline{\text{SS}}$
19	4F	$\overline{\text{G}}$	54	4G	NC
20	5G	$\overline{\text{SWEb}}$	55	4H	NC
21	7H	DQb7	56	4M	$\overline{\text{SWE}}$
22	6H	DQb8	57	3L	$\overline{\text{SWEd}}$
23	7G	DQb6	58	1K	DQd7
24	6G	DQb5	59	2K	DQd8
25	6F	DQb4	60	1L	DQd6
26	7E	DQb2	61	2L	DQd5
27	6E	DQb3	62	2M	DQd4
28	7D	DQb1	63	1N	DQd2
29	6D	DQb0	64	2N	DQd3
30	6A	SA2	65	1P	DQd1
31	6C	SA1	66	2P	DQd0
32	5C	SA5	67	3T	SA12
33	5A	SA4	68	2R	SA10
34	6B	SA9	69	4N	SA17
35	5B	SA8	70	3R	M1

Notes: 1. Bit number1 is the first scan bit to exit the chip.
2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “Place Holder”. Placeholder registers are internally connected to V_{SS}.
3. In Boundary scan mode, differential input K and $\overline{K}$ are referred to each other and must be at opposite logic levels for reliable operation.
4. ZZ must remain at V_{IL} during boundary scan.
5. In boundary scan mode, ZQ must be driven to V_{DDQ} or V_{SS} supply rail to ensure consistent results.
6. M1 and M2 must be driven to V_{DD} or V_{SS} supply rail to ensure consistent results.

ID register

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	×	×	×	×	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				Depth					Width					Use in the future						Vendor ID No.											Fix

TAP Controller State Diagram

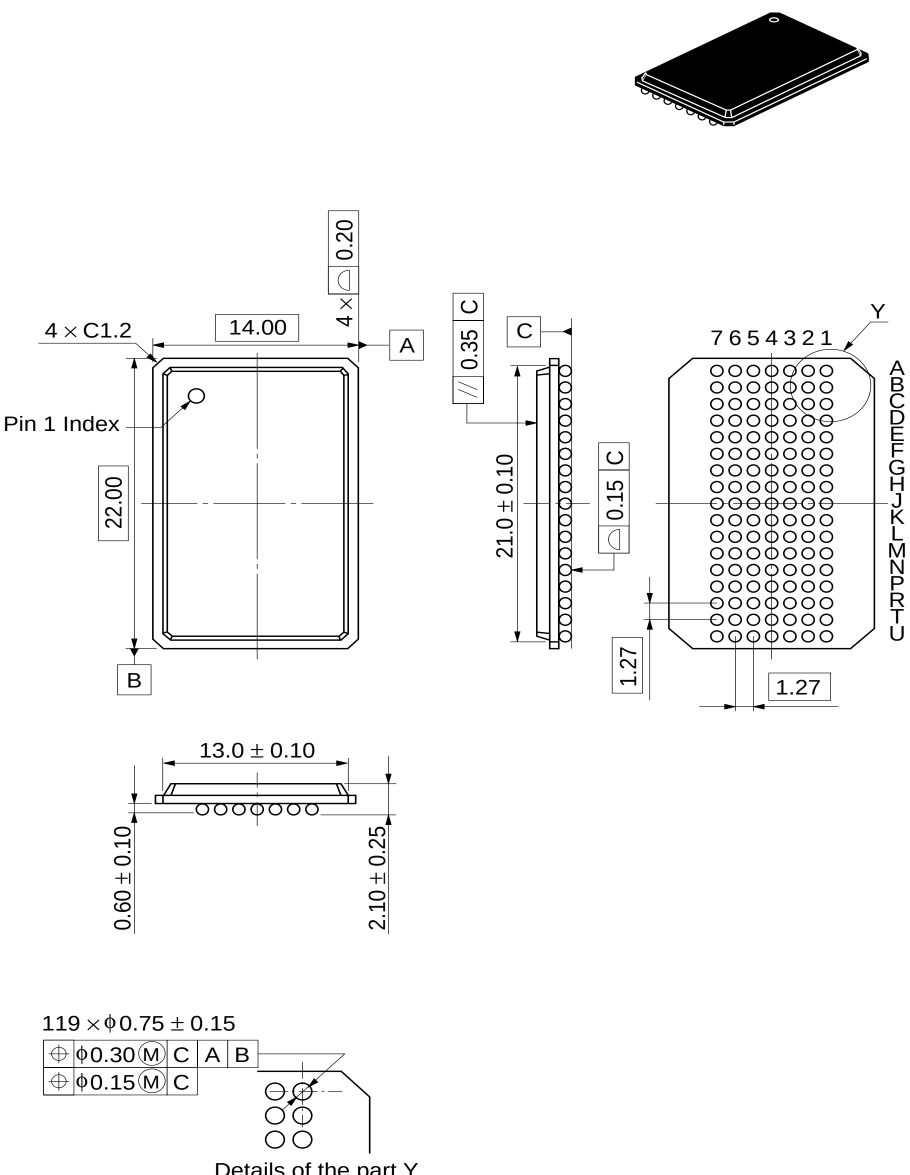


Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

HM62G36256BP Series (BP-119A)

Unit: mm



Hitachi Code	BP-119A
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.2 g

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