SCBS027A - FEBRUARY 1989 - REVISED JANUARY 1994

12 1Y4

11 2A1

2Y1 🛮 9

GND [] 10

DW OR N PACKAGE State-of-the-Art BiCMOS Design (TOP VIEW) Significantly Reduces I_{CC7} 3-State Outputs Drive Bus Lines or 1OE **Buffer-Memory Address Registers** 1A1 🛮 2 P-N-P Inputs Reduce DC Loading 2Y4 🛮 3 18 1Y1 High-Impedance State During Power Up 1A2 🛮 17 2A4 and Power Down 2Y3 🛮 5 16 1Y2 Package Options Include Plastic 1A3 **[**] 6 15 2A3 Small-Outline (DW) Packages and Standard 14 🛮 1Y3 2Y2 | 7 Plastic 300-mil DIPs (N) 1A4 🛮 8 13 2A2

description

This octal buffer and line driver is designed specifically to improve both the performance and

density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the SN64BCT240 and SN64BCT241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs.

The SN64BCT244 is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

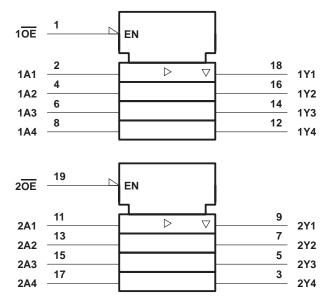
The SN64BCT244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

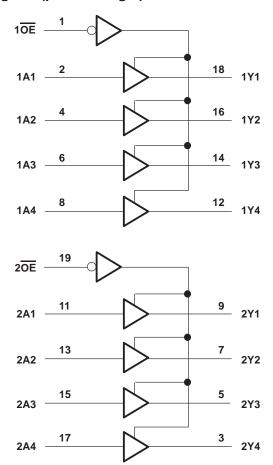


logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the disabled or power-off state, V _O	
Voltage range applied to any output in the high state, VO	
Current into any output in the low state, IO	
Operating free-air temperature range	
Storage temperature range	-65° C to 150° C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
ΙK	Input clamp current			-18	mA
IOH	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V
Vou	V _{CC} = 4.5 V	$I_{OH} = -3 \text{ mA}$		2.4	3.3		V
Voн		$I_{OH} = -15 \text{ mA}$		2	3.1		V
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 64 \text{ mA}$			0.42	0.55	V
lį	V _{CC} = 5.5 V,	V _I = 7 V				0.1	mA
lін	V _{CC} = 5.5 V,	V _I = 2.7 V				20	μΑ
Ι _{ΙL}	$V_{CC} = 5.5 V,$	V _I = 0.5 V				-1	mA
107	$V_{CC} = 0$ to 2.3 V (power up)	$V_0 = 2.7 \text{ V or } 0.5 \text{ V},$	OE at 0.8 V			± 50	μА
loz	V _{CC} = 1.8 V to 0 (power down)					± 50	μΛ
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V				50	μΑ
lozL	$V_{CC} = 5.5 V,$	V _O = 0.5 V				-50	μΑ
los†	$V_{CC} = 5.5 V,$	V _O = 0		-100		-225	mA
Іссн	V _{CC} = 5.5 V,	Output open			23	40	mA
ICCL	V _{CC} = 5.5 V,	Output open			53	80	mA
Iccz	$V_{CC} = 5.5 V,$	Output open			4	10	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	C = 5 V, = 50 pF = 500 Ω = 500 Ω = 25°C	,	V _{CC} = 4.5 C _L = 50 pl R1 = 500 Q R2 = 500 Q T _A = MIN 1	2, 2,	UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	А	Υ	1.2	2.5	4.4	0.9	5.3	ns
^t PHL		ı	1.7	3.2	5	1.4	6	115
^t PZH	ŌĒ	Y	2	5.7	7.8	2	9	ns
^t PZL		1	2	5.9	8.1	2	9.4	115
^t PHZ	ŌĒ	Y	2	5.4	6.7	2	8	ns
tPLZ		1	2	6.1	7.6	2	9.8	1115

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



[†] All typical values are at V_{CC} = 5 V. ‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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