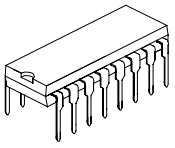
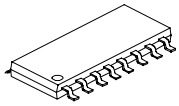
PLL FOR DTS



DIP-16-300-2.54



SOP-16-300-1.27

DESCRIPTION

The SC9256 is phase-locked loop (PLL) LSIs for digital tuning systems (DTS) with built in 2 modulus prescalers.

All functions ate controlled through 3 serial bus lines. These LSIs are used to configure high-performance digital tuning system.

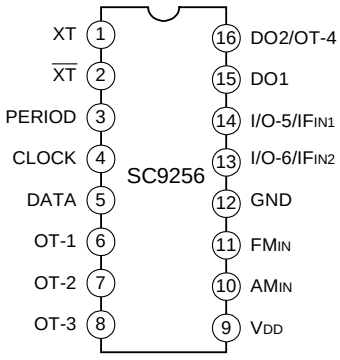
FEATURES

* Optimal for configuring digital tuning systems in high-fi tuners and car stereos.
* built-in prescalers. Operate at input frequency ranging from 30~150 MHz during FM_{IN} input (with 2 modulus prescaler) and at 0.5~40MHz during AM_{IN} input (with 2 modulus prescaler or direct dividing).
* 16 bit programmable counter, dual parallel output phase comparator, crystal oscillator and reference counter.
* 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz crystal oscillators can be used.
* 15 possible reference frequencies. (When using 4.5MHz crystal)
* Built-in 20 bit general-purpose counter for such uses as measuring intermediate frequencies (IF_{IN1} and IF_{IN2})
* High-precision (±0.55~±7.15μs) PLL phase error detection.
* Numerous general-purpose I/O pins for such uses as peripheral circuit control.
* 3 N-channel open-drain output ports (OFF withstanding voltage:12V) for such uses as control signal output.
* Standby mode function (turns off FM, AM and IF amps) to save current consumption.
* All functions controlled through 3 serial bus lines.
* CMOS structure with operating power supply range of V_{DD}=5.0±0.5V.

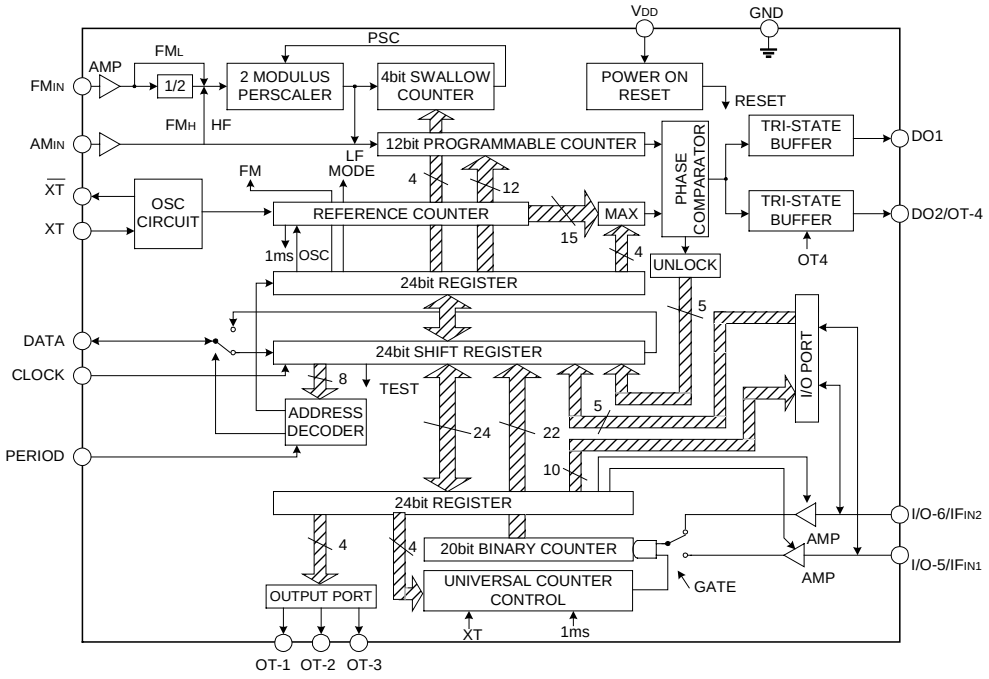
ORDERING INFORMATION

Device	Package
SC9256	DIP-16-300-2.54
SC9256S	SOP-16-300-1.27

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3~6.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
N-ch Open-Drain Off withstanding Voltage	V_{OFF}	13	V
Power Dissipation	P_D	300(200)	mW
Operating Temperature	T_{OPR}	-40~85	°C
Storage Temperature	T_{STG}	-65~150	°C

( ): Flat package

ELECTRICAL CHARACTERISTICS (unless otherwise specified, Ta= -40~85°C, V_{DD}=4.5~5.58V.)

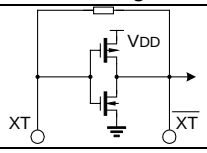
Characteristic	Symbol	Test Condition/Pin	Min	Typ.	Max	Unit
Operating Power Supply Voltage	V_{DD1}	PLL operation (normal operating)	4.5	5.0	5.5	V
Operating Power Supply Current	I_{DD1}	V_{DD}=5.0V, XT=10.8MHz, FMIN=150MHz	--	7	15	mA
Stand-by mode						
Crystal Oscillation Frequency Supply Voltage	V_{DD2}	PLL OFF (Operating crystal oscillation)	4.0	5.0	5.5	V
Operating Power Supply Current	I_{DD2}	V_{DD}=5.0V, XT =10.8MHz PLL OFF	--	0.8	1.5	mA
Operating Power Supply Current	I_{DD3}	V_{DD}=5.0V, XT stop, PLL OFF	--	120	240	μA
Operating frequency range						
Crystal Oscillation Frequency	f_{XT}	Connect crystal resonator to XT- $\overline{XT}$ terminal	3.6	~	10.8	MHz
FM_{IN} (FM_H, FM_L)	f_{FM}	FM_H, FM_L mode, V_{IN}=0.2Vp-p	30	~	130	MHz
FM_{IN} (FM_L)	f_{FML}	FM_L mode, V_{IN}=0.3Vp-p	30	~	150	MHz
AM_{IN} (HF)	f_{HF}	HF mode, V_{IN}=0.2Vp-p	1	~	40	MHz
AM_{IN} (LF)	f_{LF}	LF mode, V_{IN}=0.2Vp-p	0.5	~	20	MHz
IF_{IN1}, IF_{IN2}	f_{IF}	V_{IN}=0.2Vp-p	0.1	~	15	MHz
SC_{IN}	f_{SC}	V_{IH}=0.7V_{DD}, V_{IL}=0.3V_{DD}, square wave input.	--	~	100	kHz
Operating input amplitude range						
FM_{IN} (FM_H, FM_L)	V_{FM}	FM_H, FM_L mode, f_{IN}=30~130MHz	0.2	~	V_{DD}-0.5	Vp-p
FM_{IN} (FM_L)	V_{FML}	FM_L mode, f_{IN}=30~150MHz	0.3	~	V_{DD}-0.5	Vp-p
AM_{IN} (HF)	V_{HF}	HF mode, f_{IN}=1~40MHz	0.2	~	V_{DD}-0.5	Vp-p
AM_{IN} (LF)	V_{LF}	LF mode, f_{IN}=0.5~20MHz	0.2	~	V_{DD}-0.5	Vp-p
IF_{IN1}, IF_{IN2}	V_{IF}	F_{IN}=0.1~15MHz	0.2	~	V_{DD}-0.5	Vp-p
OT1~OT4 N-ch open drain						
Output Current "L" level	I_{OL1}	V_{OL}=1.0V	5.0	10.0	--	mA
OFF-leak Current	I_{OEF}	V_{OFF}=12V	--	---	2.0	μA

(To be continued)

(Continued)

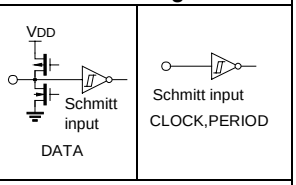
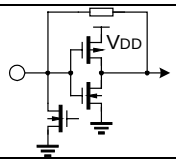
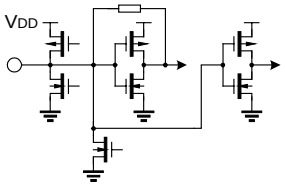
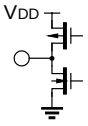
Characteristic		Symbol	Test Condition/Pin	Min	Typ.	Max	Unit
I/O-5~I/O-9, SCIN							
Input Voltage	"H" level	V_{IH1}		0.7V_{DD}	~	V_{DD}	V
	"L" level	V_{IL1}		0	~	0.3V_{DD}	
Input Current	"H" level	I_{IH}	V_{IH}=5V	--	--	2.0	μA
	"L" level	I_{IL}	V_{IL}=0V	--	--	-2.0	
Output Current	"H" level	I_{OH4}	V_{OH}=4.0V (expect SCIN)	-2.0	-4.0	--	mA
	"L" level	I_{OL4}	V_{OL}=1.0V (expect SCIN)	2.0	4.0	--	
PERIOD, CLOCK, DATA							
Input Voltage	"H" level	V_{IH2}		0.8V_{DD}	~	V_{DD}	V
	"L" level	V_{IL2}		0	~	0.2V_{DD}	
Input Current	"H" level	I_{IH}	V_{IH}=5V	--	--	2.0	μA
	"L" level	I_{IL}	V_{IL}=0V	--	--	-2.0	
Output Current	"H" level	I_{OH5}	V_{OH}=4.0V (DATA)	-1.0	-3.0	--	mA
	"L" level	I_{OL5}	V_{OL}=1.0V (DATA)	1.0	3.0	--	
DO1, DO2							
Input Current	"H" level	I_{OH3}	V_{OH}=4.0V	-2.0	-4.0	--	mA
	"L" level	I_{OL3}	V_{OL}=1.0V	2.0	4.0	--	
Tri-State Lead Current		I_{TL}	V_{TLH}=5V, V_{TLL}=0V	--	--	±1.0	μA
$\overline{XT}$							
Output Current	"H" level	I_{OH2}	V_{OH}=4.0V	-0.1	-0.3	--	mA
	"L" level	I_{OL2}	V_{OL}=1.0V	0.1	0.3	--	
Input feedback resistance							
Input Feedback Resistance	"H" level	Rf1	FMIN, AMIN, IFIN (Ta=25°C)	350	700	1400	kΩ
	"L" level	Rf2	XT- $\overline{XT}$ (Ta=25°C)	500	1000	4000	

PIN DESCRIPTION

Pin No.	Symbol	Pin name	Description	Circuit diagram
1	XT	Crystal oscillator pins	Connects 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz crystal oscillator to supply reference frequency and internal clock	
2	$\overline{XT}$			

(To be continued)

(Continued)

Pin No.	Symbol	Pin name	Description	Circuit diagram
3	PERIOD	Period signal input	Serial I/O ports. These pins transfer data to and from the controller to set divisions and dividing modes, and to control the general-purpose counter and general-purpose I/O ports.	
4	CLOCK	Clock signal input		
5	DATA	Serial data input/output		
6	OT-1	General-purpose output ports	N channel open drain port pins, for such uses as control signal output. These pins are set to the OFF state when power is turned on.	 N-channel open drain
7	OT-2			
8	OT-3			
10	AMIN	Programmable counter input	These pins input FM and AM band local oscillator signals by capacitor coupling. FMIN and AMIN operate at low amplitude.	
11	FMIN			
13	I/O-6/IFIN2	General-purpose I/O ports/General-purpose counter frequency measurement input	General-purpose I/O port input /output pins. Can be switched for use as input pins to measure general purpose counter frequencies. The frequency measurement function has such uses as measuring inter-mediate frequencies (IF). These pins feature built-in amps. Data are input by capacitor coupling. FMIN and AMIN operate at low amplitude. (note) Pins are set for input when power is turned on.	
14	I/O-5 /IFIN1			
15	DO1	Phase comparator output (General-purpose output ports)	These pins are for phase comparator tri-state output. DO1 and DO2 are output in parallel.	
16	DO2/OT-4			
12	GND	Power supply pins	Applies 5.0V±10%	
9	VDD			

FUNCTION DESCRIPTION

Serial I/O ports

As the block diagram shows, the functions are controlled by setting data in the 48 bits contained in each of the 2 sets of 24 bit registers. Each bit of data in these register is transferred through the serial ports between the controller and the DATA, CLOCK and PERIOD pins. Each serial transfer consists of a total of 32 bits, with 8 address bits and 24 data bits.

Since all functions are controlled in units of registers, the explanation in this manual focuses on the 8 bit address and functions of each register.

These registers consist of 24 bits and are selected by an 8 bit address.

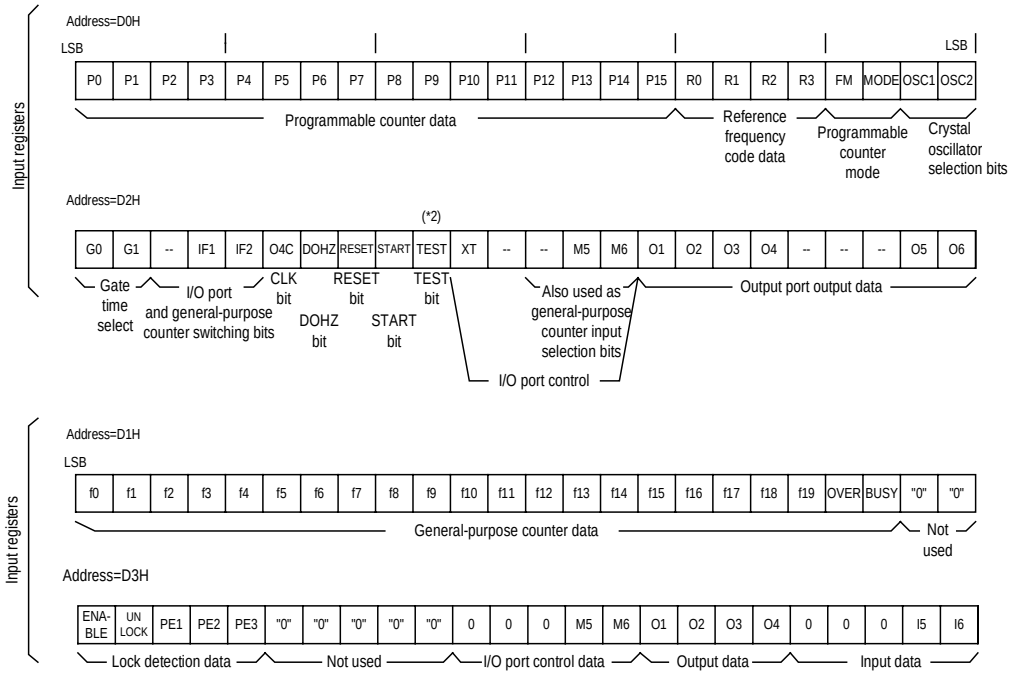
A list of the address assignment for each register is given below under register assignments.

Register	Address	Contents of 24 bits	No. of bit
Input register 1	D0H	PLL divisor setting	16
		Reference frequency setting	4
		PLL input and mode setting	2
		Crystal oscillator selection	2
			total 24
Input register 2	D2H	General=purpose counter control (including lock detection bit control)	4
		I/O port and general-purpose counter switching bits	3
		I/O-5/CLK pin switching bit	1
		DO pin control	1
		Test bit	1
		I/O port control (also used as general-purpose counter input selection bits)	5
		Output data	9
			total 24
Output register 1	D1H	General-purpose counter numeric data	22
		Not used	2
			total 24
Output register 2	D3H	Lock detection data	5
		I/O port control data	5
		Output data	4
		Input data (undefined during output port selection)	5
		Not used	5
			total 24

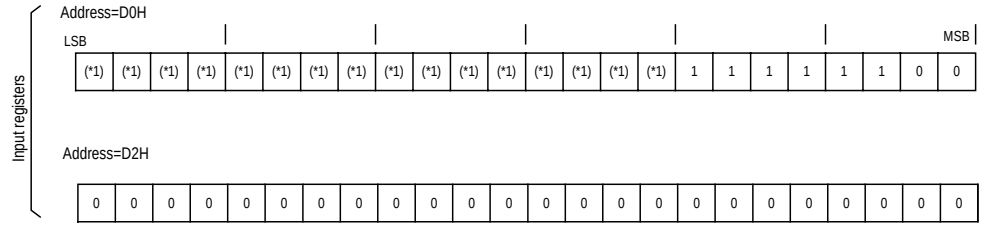
When the PERIOD signal falls, the input data are latched in register 1 or register 2 and the function is performed.

When the CLOCK signal falls for 9 time, the output data are latched in parallel in the output registers. The data are subsequently output serially from the data pin.

REGISTER ASSIGMENTS



When power is turned on, the input registers are set as shown below.



Note: 1. Data are undefined.

2. Set data to “0” for test bit.

Serial transfer format

The serial transfer format consists of 8 address bits and 24 data bits (Fig. 1). Addresses D0H~D3H are used.

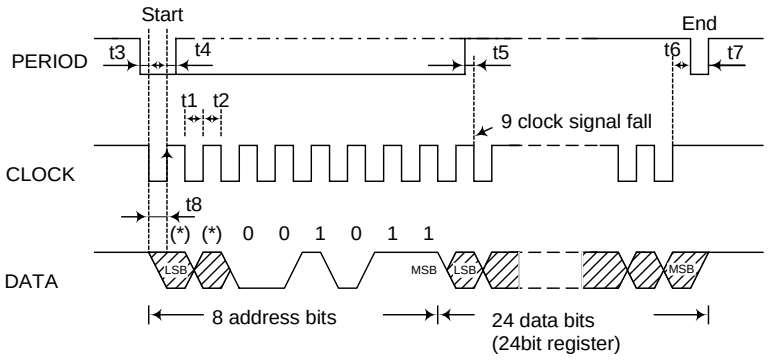


Fig.1

• Serial data transfer

serial data are transferred in sync with the clock signal. In the idle state, the PERIOD, CLOCK and DATA pin lines are all set to “H” level. When the period signal is at “L” level, the falling of the clock signal initiates serial data transfer. Data transfer ceases when the period signal is set to “L” level when the clock signal is at “H” level. Once serial data transfer has begun, however, no more than 8 falls of the clock signal can occur during the time the period signal is at “L” level.

Since the receiving side receives the serial data as valid data when the clock signal rises, it is effective for the sending side to produce output in sync with the clock signal fall.

To receive serial data from the output registers (D1H, D3H), set the serial data output to high impedance after the 8 bit address is output but before the next clock signal falls.

Data reception subsequently continues until the period signal becomes “L” level; data transfer ends just before the period signal rises. Therefore, the data pin must have an open-drain or tristate interface.

Note: 1. when power is turned on, some internal circuit have undefined states. To set internal circuit states, execute a dummy data transfer before performing regular data transfer.

2. times t1~t8 have the following value:

t1≥1.0μs

t2≥1.0μs

t3≥0.3μs

t4≥0.3μs

t5≥0.3μs

t6≥1.0μs

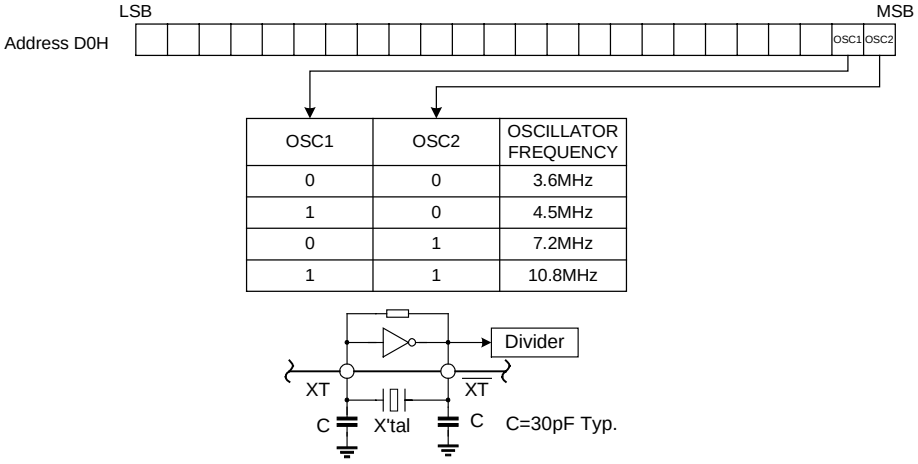
t7≥1.0μs

t8≥0.3μs

3. Asterisks represent numbers taken from addresses, as in D*H.

Crystal oscillator pins (XT, $\overline{XT}$)

As fig.2 shows, the clock necessary for internal operation is produced by connecting a crystal oscillator between capacitors. Use the crystal oscillator selection bit to select an oscillating frequency of 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz which matches that of the crystal oscillator used.



OSC1	OSC2	OSCILLATOR FREQUENCY
0	0	3.6MHz
1	0	4.5MHz
0	1	7.2MHz
1	1	10.8MHz

Fig.2

Note: set to 3.6MHz (OSC1="0" and OSC2="0") when power is turned on. The crystal is not oscillating at this time because the system is in standby mode.

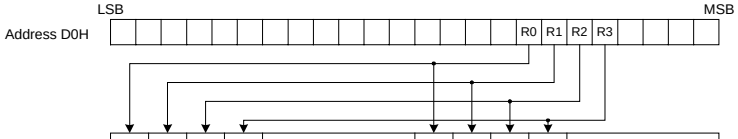
Reference counter (Reference frequency divider)

The reference counter section consists of a crystal oscillator and a counter.

A crystal oscillator frequency of 3.6MHZ, 7.2MHZ or 10.8MHZ can be selected .A maximum of 15 reference frequencies can be generated.

1. Setting reference frequency

The reference frequency is set using bits R0~R3.



R0	R1	R2	R3	REFERENCE FREQUENCY	R0	R1	R2	R3	REFERENCE FREQUENCY
0	0	0	0	0.5 KHz	0	0	0	1	*7.8125 KHz
1	0	0	0	1 KHz	1	0	0	1	9 KHz
0	1	0	0	2.5 KHz	0	1	0	1	10 KHz
1	1	0	0	3 KHz	1	1	0	1	12.5 KHz
0	0	1	0	3.125 KHz	0	0	1	1	25 KHz
1	0	1	0	*3.90654 KHz	1	0	1	1	50 KHz
0	1	1	0	5 KHz	0	1	1	1	100 KHz
1	1	1	0	6.25 KHz	1	1	1	1	Standby mode (*1)

Note: 1. Reference frequencies marked with an asterisk "*"can only be generated with a 4.5MHZ crystal oscillator.

2. (*1)Standby mode

Standby mode occurs when bits R0,R1,R2,and R3 are all set to "1".In standby mode, the programmable counter stops, and FM, AM and IFIN(when selected IFIN) are set to "amp off" state (pins at "L" level). This saves current consumption when the radio is turned off. The DO pins become high impedance during standby mode.

During standby mode, the I/O ports (I/O-5~I/O-6) and output ports (OT1~OT4) can be controlled and the crystal oscillator can be turned on and off.

3.The system is set to standby mode when power is turned on. At this time, the crystal oscillator is not oscillating and the I/O ports are set to input mode.

Programmable counter

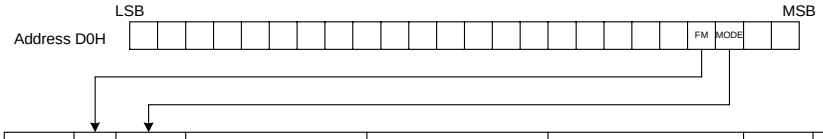
The programmable counter section consists of a 1/2 prescaler, a 2 modulus prescaler and a 4bit +12bit programmable binary counter.

1. Setting programmable counter

16 bits of divisor data and 2 bits, which indicate the dividing mode, are set in the programmable counter.

(*1) Setting dividing mode*

The FM and MODE bits are used to select the input pin and the dividing mode (pulses wallow mode or direct dividing mode). There are 4 possible choices, shown in the table below .Select one based on the frequency band used.

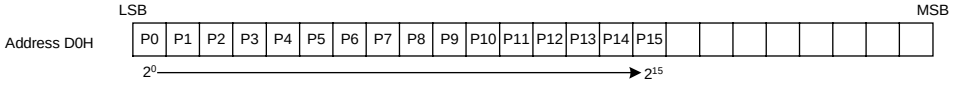


MODE	FM	MODE	DIVIDING MODE	TYPICAL RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT PIN	FREQUENCY
LF	0	0	Direct dividing mode	LW,MW,SWL	0.5 ~ 20MHz	AMIN	n
HF	0	1	Pulse swallow mode	SWH	1 ~ 40MHz		
FML	1	0		FM	30 ~ 130MHz 30 ~ 150MHz	FMIN	
FMH	1	1	1/2 + pulse swallow mode	FM	30 ~ 130MHz		2n

(2) Setting divisor

The divisor for the programmable counter is set as binary data in bits P0~P15.

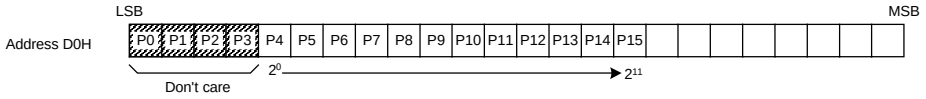
- Pulse swallow mode (16 bits)



Divisor setting range (pulse swallow mode):n=210H~FFFH (528~65535)

(Note) With the 1/2+pulse swallow mode, the actual divisor is twice the programmed value.

• Direct dividing mode (12 bits)



Divisor setting range (direct dividing mode):n=10H~FFFH(16~4095)

With the direct dividing mode, data p0~p3 are don't-care and bit p4 is the LSB.

2. Prescaler and programmable counter circuit configuration

(1) Pulse swallow mode circuit configuration

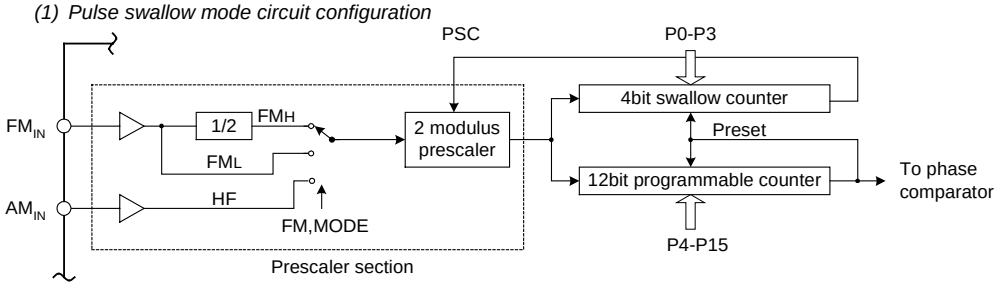


Fig.3

This circuit consists of a 2 modulus prescaler, a 4 bit swallow counter and a 12bit programmable counter. During FMIN(FMIN mode),a 1/2 prescaler is added to the preceding step.

(2) *Direct dividing method circuit configuration*

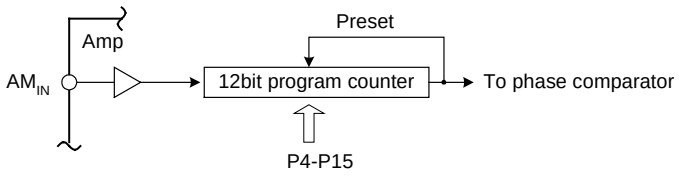


Fig.4

With the direct dividing mode, the prescaler section is bypassed and the 12bit programmable counter is used.

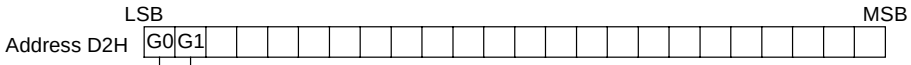
(3) Both FMIN and AMIN have built-in amps. Data are input by capacitor coupling. FMIN and AMIN operate at low amplitude.

General-purpose counter

The general-purpose counter is a 20bit counter. It has such uses as counting AM/FM band intermediate frequencies (IF) and detecting auto-stop signals during auto-search tuning. General-purpose counter pins can also be used as I/O ports.

1. General-purpose counter control bits

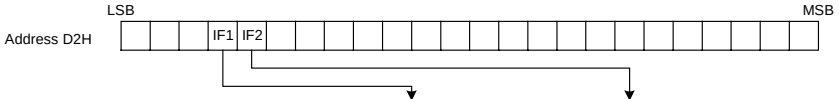
(1) Bits G0 and G1 … Used for selecting the general-purpose counter gate time.



G0	G1	GATE TIME	CYCLE MEASUREMENT PULSE
0	0	1ms	50 KHz
1	0	4ms	150 KHz
0	1	16ms	900 KHz
1	1	64ms	Crystal oscillator frequency

(2) Bits SC,IF1 and IF2 …I/O port and general-purpose counter switching bits.

(*) The functions of the following pins are switched by data.

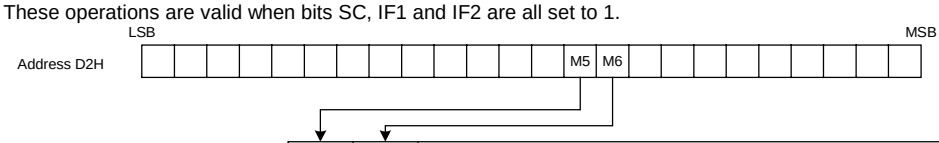


IF1	I/O-5/IF_{IN1}
1	IF_{IN1}
0	I/O-5

IF2	I/O-6/IF_{IN2}
1	IF_{IN2}
0	I/O-6

(3) *Bits M5 sets the state for pin I/O-5/IF$_{IN1}$; M6, for pin I/O-6/IF$_{IN2}$.*

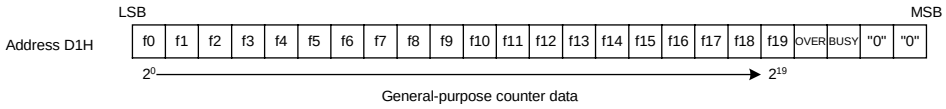
These operations are valid when bits SC, IF1 and IF2 are all set to 1.



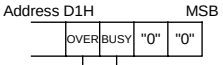
M5	M6	PIN STATES (When bits sc, IF1 and IF2 are all set to "1")	
		IF_{IN1}	IF_{IN2}
0	0	INPUT pulled down	INPUT pulled down
(*)	1		INPUT enabled
1	0	INPUT enabled	INPUT pulled down
0	0	INPUT pulled down	

Note: Bits marked with an asterisk "(*)" are don't care

(4) *Bits f0~f9…The general-purpose counter results can be read in binary from bits f0~f9 of the output register (D1H).*



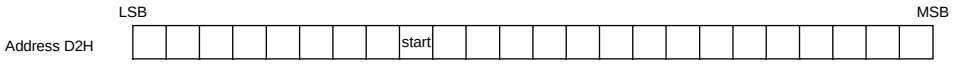
(5) *OVER and BUSY bits…Detect the operating state of the general-purpose counter.*



	BIT DATA = "1"	BIT DATA = "0"
General-purpose counter option monitor bit	General-purpose counter busy	General-purpose counter ended counting
General-purpose counter overflow detection bit	Counted value in general-purpose counter $\geqslant 2^{20}$ (Overflow state)	Counted value in general-purpose counter $\leqslant 2^{20}-1$

Note: When using the general-purpose counter, before referring to the contents of the general-purpose counter result bit (f0~f9), confirm that the busy bit is “0” (counting is ended) and the OVER bit is “0” (general-purpose counter data are normal).

(6) *START bit…When the data are set to “1”, the general-purpose counter is reset then counting begins.*



0	Counting continues uninterrupted.
1	Counting begins after general - purpose counter is reset.

2. General-purpose counter circuit configuration

The general-purpose counter section consists of input amps, a gate time control circuit and a 20 bit binary counter.

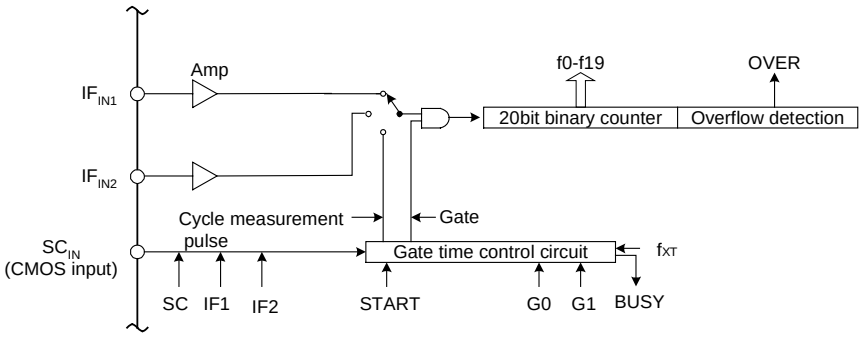
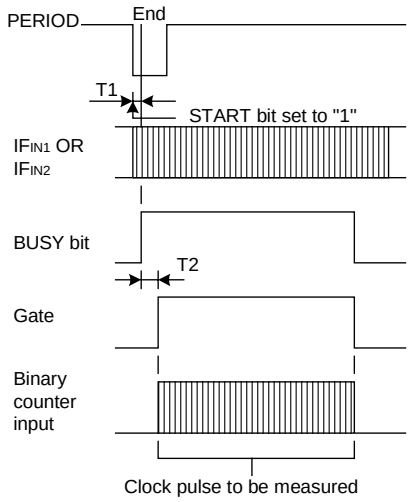


Fig.5

3. General-purpose counter measurement timing



Frequency measurement timing chart

$0<T1\leq 0.25(\mu s)$, $0<T2\leq 1$ (ms)

Note: 1. IF_{IN1} and IF_{IN2} input have built-in amps. Data are input by capacitor coupling. FM_{IN} and AM_{IN} operate at low amplitude.

General-purpose I/O ports

These LSIs feature general-purpose output and I/O ports which are controlled through the serial ports.

Input/output form	port	Input/output configuration
Output port	Dedicated: 4 ports	N channel open-drain output
I/O ports	Dedicated: 1 port, Maximum: 5 ports	CMOS input/output

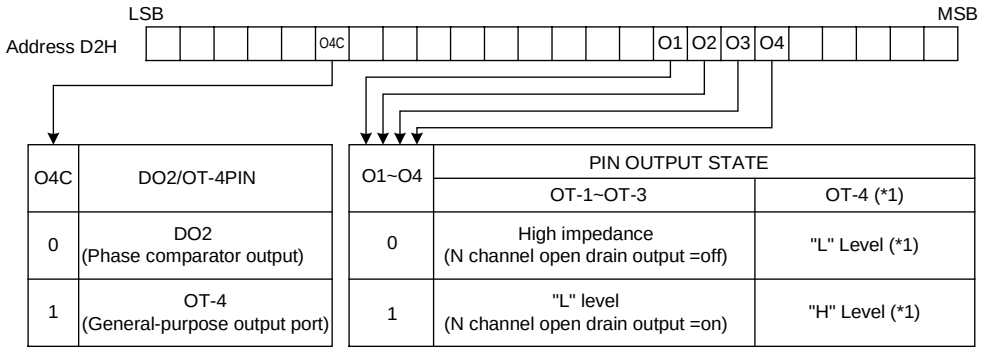
1. General-purpose output ports (OT-1~OT-4)

Pins OT-1~OT-4 are general-purpose dedicated output ports. They have such uses as control signal output. They are configured for N channel open-drain output and have an off withstanding voltage of 12V.

The data set in bits O1~O4 of the input register (D2H) are output in parallel from their correspond dedicated output port pins OT-1~OT-4. SC9256 do not have dedicated output port OT-4, but setting the input register (D2H) CLK (O4C) bit to “1” converts pin DO2 into output port OT-4 (configured for CMOS output).

The data set in bits O1~O4 of the input register (D2H) can also be read from the DATA pins as output register (D3H) serial data O1~O4.

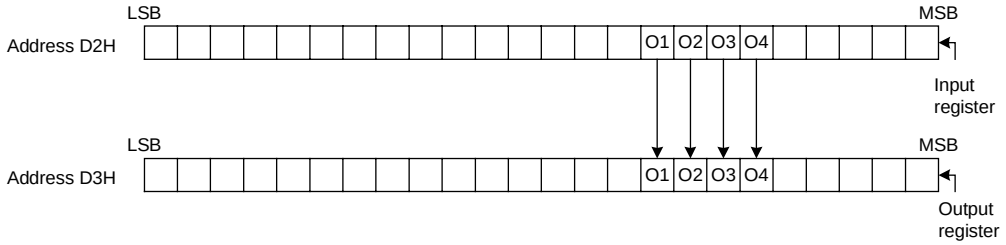
(1) SC9256



O4C	DO2/OT-4PIN
0	DO2 (Phase comparator output)
1	OT-4 (General-purpose output port)

O1~O4	PIN OUTPUT STATE	
	OT-1~OT-3	OT-4 (*1)
0	High impedance (N channel open drain output =off)	"L" Level (*1)
1	"L" level (N channel open drain output =on)	"H" Level (*1)

(2)output register … The data set in bits O1~O4 of the input register can read as serial data O1~O4 from the output register (D3H).



2. General-purpose I/O ports (I/O-5~I/O-6)

Pins I/O-5~ I/O-6 are general-purpose I/O ports used for control signal input and output. They are configured for CMOS input and output.

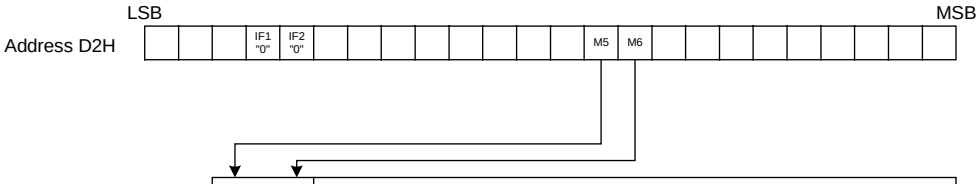
These I/O ports are set for input or output using bits M5~M6 of the input register (D2H).

Setting M5~M6 to “0” sets these ports for input. Data which are input in parallel from I/O-5~I/O-6 are latched in the internal register on the ninth fall of the serial clock signal. These data can then be read as serial data I5~I6 from the DATA pins.

Data which are set in bits O5~O6 of the input register (D2H) are output in parallel from their corresponding general-purpose I/O port pin I/O-5~I/O6.

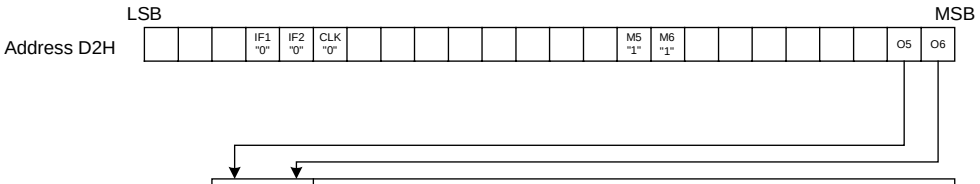
These operations are valid when bits SC, IF1, IF2 and CLK are all set to “0”.

(1) SC9256



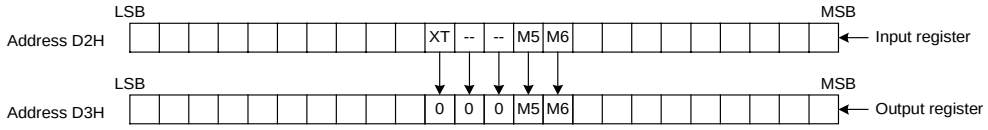
M5, M6	PIN INPUT /OUTPUT STATE (When IF1 and IF2 are "0")
	I/O -5, I/O -6
0	"L" Level
1	"H" Level

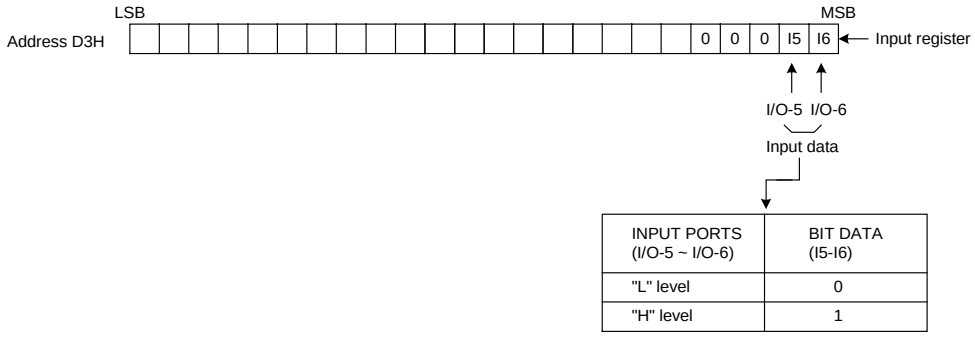
- **Setting data for output ports**



O5, O6	PIN OUTPUT STATE (When IF1 and IF2 are "0")
	I/O -5, I/O -6
0	"L"level
1	"H"level

(2)OUTPUT register…data which are set in bits M5~M6 of the input register (D2H) can be read as serial data M5~M6 from the output register (D3H).





INPUT PORTS (I/O-5 ~ I/O-6)	BIT DATA (I5-I6)
"L" level	0
"H" level	1

Note:

1. When pins I/O-5~I/O-6 are used for output, the data in I5~I6 of the output register(D3H) are undefined..
2. When power is turned on, input register (D2H) I/O port control bits M5~M6 and output data bits O5~O6 are set to “0”. General-purpose I/O ports are set as input ports. Pins which are used both as general-purpose I/O ports and for general-purpose counter input are set for I/O port input. The output state of general-purpose output ports is set to high impedance (N channel open drain output =off).
3. Pin I/O-5 and I/O-6 also serve as general-purpose counter input pins. Therefore, bits IF1 and IF2 of input register 2 must be set to “0” when these pins are used as I/O ports.

Phase comparator

The phase comparator outputs the phase error after comparing the phase difference of the reference frequency signal supplied by the reference counter and the divided output from the programmable counter. The frequencies and phase differences of these two signals are then equalized by passing them through low-pass filters. These signals then control the VCO.

The filter constants can be customized for FM and AM bands since the signals are output in parallel from the phase comparator then pass through the two tristate buffer pins, DO1 and DO2.

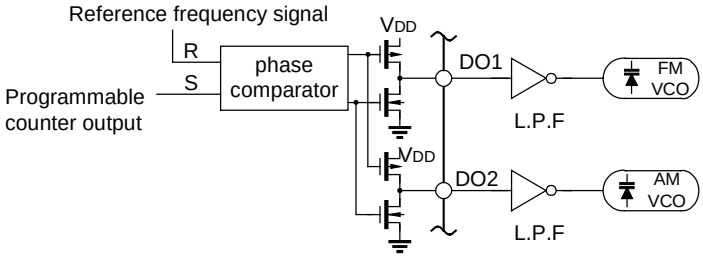
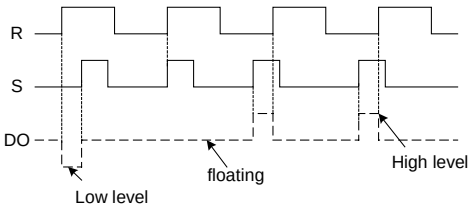
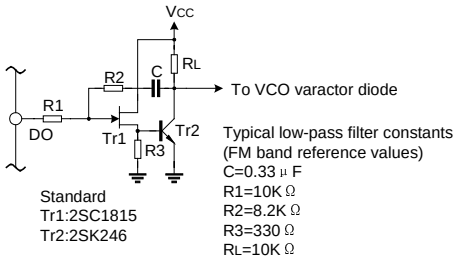


Fig.7



DO Output Timing Chart

Fig.8



Typical Active Low-Pass Filter Circuit

Fig.9

The figures above show the DO output timing chart and a typical active low-pass filter circuit featuring a Darlington connection between the FET and transistor.

The filter circuit shown above is just one example. Actual circuits should be designed based on the band composition and the properties desired from the system.

Pin DO2 can be switched for use as pin OT-4.

Lock detection bits

The lock detection bits detect locked states in the PLL system. These systems have an unlock detection bit (unlock bit) which is used to detect, using the reference frequency cycle, the phase difference between the reference frequency and divided output of programmable counter. These systems also have phase error detection bits (bits PE1~PE3), which are capable of more precise detection (±0.55μs~±7.15μs).

1. Unlock detection bit (UNLOCK)

This bit detects, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. When there is no lock, that is, when the reference frequency and the divided output of the programmable counter are not the same, unlock F/F is set.

Unlock F/F is reset every time the input register (D2H) unlock reset bit (RESET) is set to “1”. After unlock F/F has been reset in this way, locked state can detected by checking the unlock detection bit (UNLOCK) of the output register (D3H). After unlock F/F has been reset, the unlock detection bit must be checked after a time interval exceeding that of the reference frequency cycle has elapsed. This is because the reference frequency cycle inputs the lock detection strobe to unlock F/F. If the time interval is short, the correct locked state cannot be detected. Therefore, the output register (D3H) has a lock enable bit (ENABLE). This bit is reset every time the input register (D2H) reset bit is set to “1”, and set to “1” through the lock detection timing. That is, the locked state is correctly detected when the lock enable bit (ENABLE) is “1”.

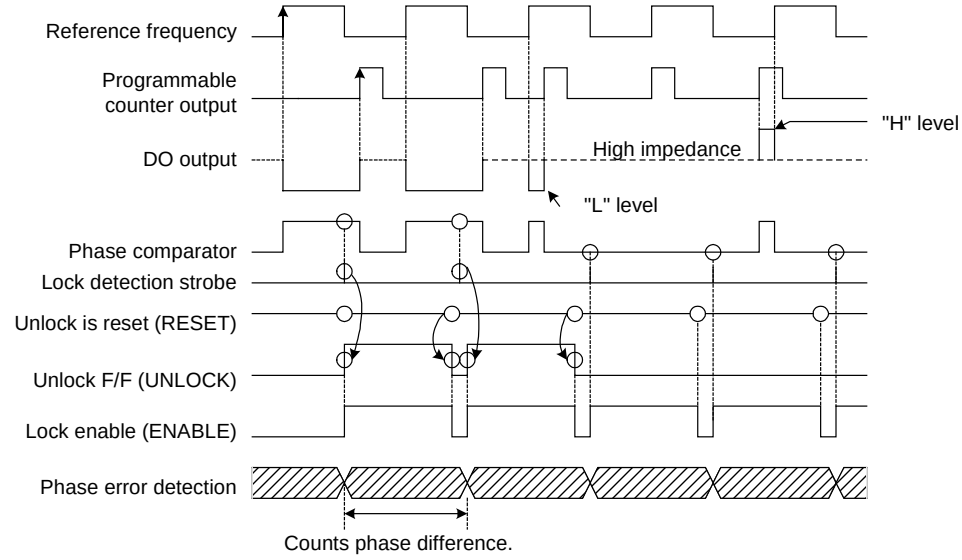
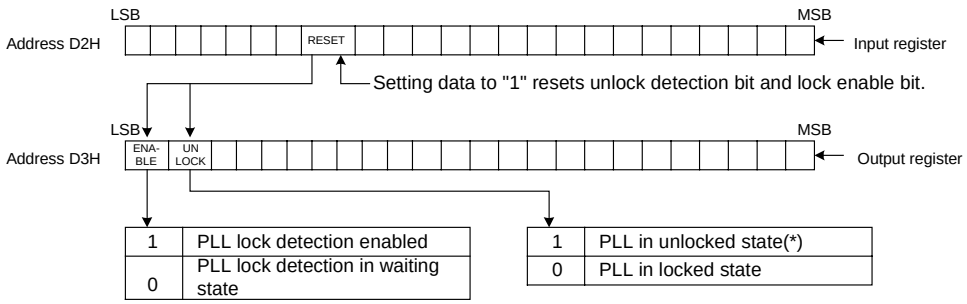


Fig.10



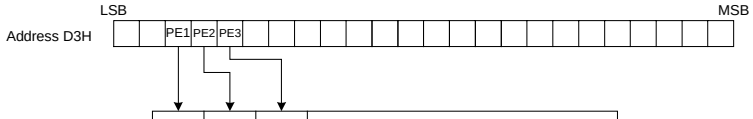
1	PLL lock detection enabled
0	PLL lock detection in waiting state

1	PLL in unlocked state(*)
0	PLL in locked state

Note: The asterisk (*) indicates an error state of over 180° phase difference relative to the reference frequency

2. Phase error detection bits (PE1~PE3)

The unlock bit detects, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. The phase error detection bits (bits PE1~PE3) are capable of precise phase error detection of ±0.55μs~±7.15μs using the reference frequency cycle.(If the UNLOCK bit is set to “1” and the phase difference relative to the reference frequency is over 180°, bits PE1~PE3 cannot correctly detect the phase error. Therefore, bits PE1~PE3 are normally used when the UNLOCK bit is set to “0”.) Bits PE1~PE3 detect phase error normally when the phase difference is -180°~180° relative to the reference frequency cycle.



PE1	PE2	PE3	PHASE ERROR (PE)
0	0	0	PE<±0.55μs
0	0	1	±0.55μs ≤PE<±1.65μs
0	1	0	±1.65μs ≤PE<±2.75μs
0	1	1	±2.75μs ≤PE<±3.85μs
1	0	0	±3.85μs ≤PE<±4.95μs
1	0	1	±4.95μs ≤PE<±6.05μs
1	1	0	±6.05μs ≤PE<±7.15μs
1	1	1	±7.15μs ≤PE

The phase error data can be read from the output register (D3H) as serial data PE1~PE3.

Following is a typical lock detection operation. It shows the operation flow from locked state to frequency change with a phase error greater than ±6.05μs.

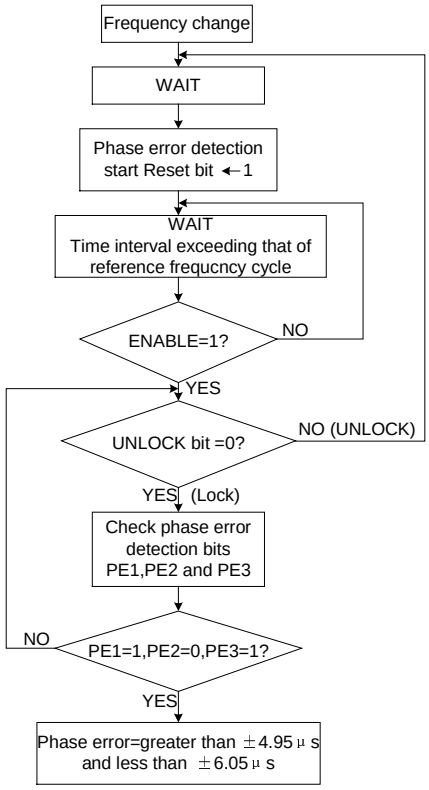


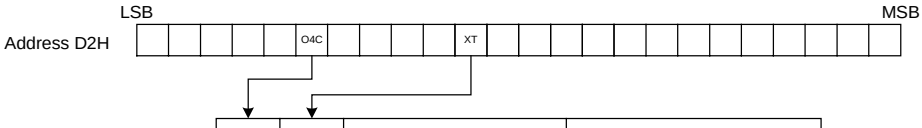
Fig.11

Other Control Bits

1. CLK and C5 bits…Control bits which switch the function for the OT-4/DO2 pin.

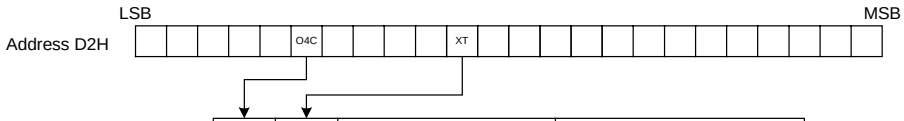
The O4C bit controls switching of the DO2 pin and OT-4 pin.

When bits R0~R3 of the input register (D0H) are set to "1" (standby mode).



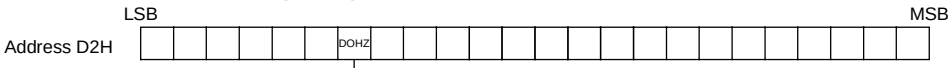
O4C	XT	DO2/OT-4 PIN STATE	CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	DO2 output	Oscillator circuit off
0	1		Oscillator circuit on
1	0	OT-4 output	Oscillator circuit off
1	1		Oscillator circuit on

When one of bit R0~R3 of the input register (D0H) is set to "0" (not standby mode)



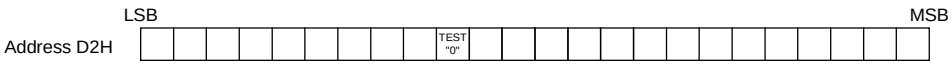
O4C	XT	DO2/OT-4 PIN STATE	CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	DO2 output	Oscillator circuit on
0	1		
1	0	OT-4 output	
1	1		

2. DOHZ bit…controls the DO2 pin output state.



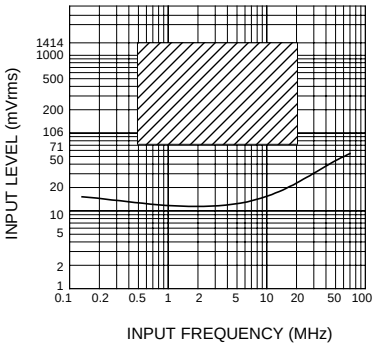
0	phase comparison error output
1	DO2 output fixed at high impedance

3. TEST bit… Data should normally be set to "0".

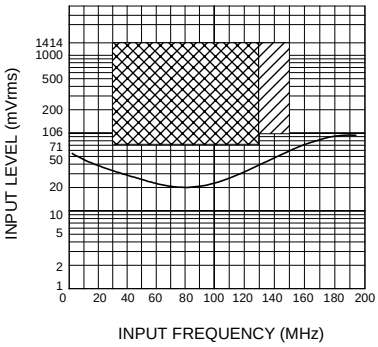


ELECTRICAL CHARACTERISTICS CURVE

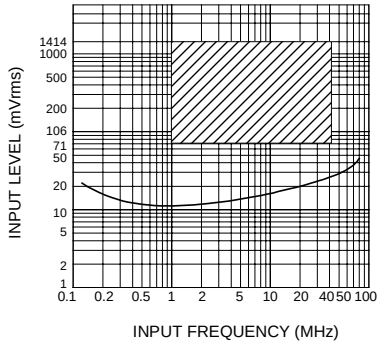
AMIN(LF) Frequency Characteristics



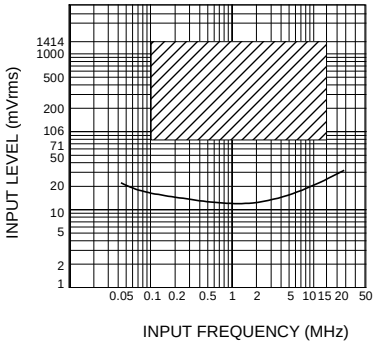
FMIN(LF) Frequency Characteristics



AMIN(HF) Frequency Characteristics



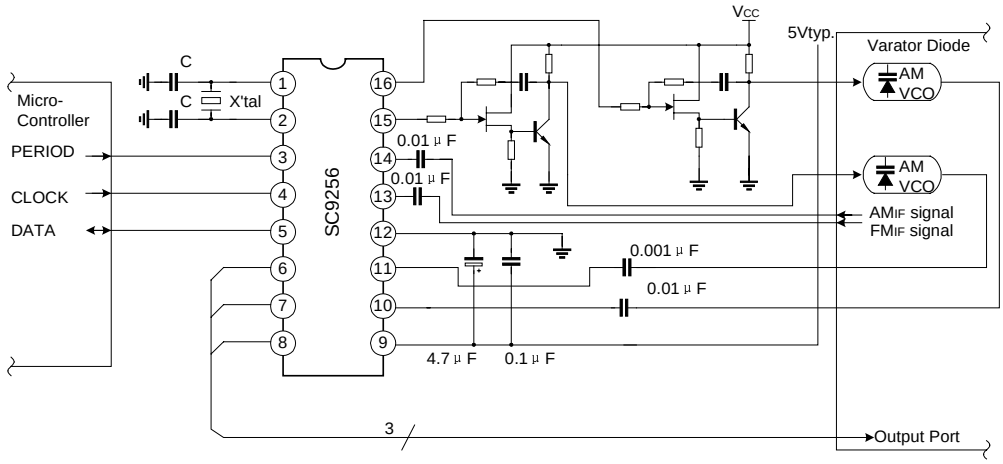
IFIN(LF) Frequency Characteristics



(Note) Operating Guarantee Range
(V_{DD}=4.5~5.5v,Ta = -40 ~ 85℃)
Standard Characteristics(V_{DD} = 5V,Ta =25℃)

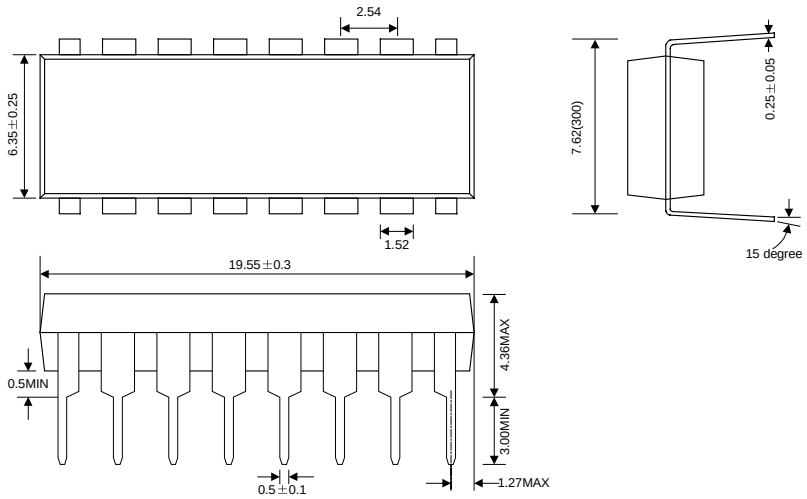
(Note) FM_{IN}:FM_H + FM_{IN}:FM_L Operating Guarantee Range
(V_{DD}=4.5~5.5v,Ta = -40 ~ 85℃)
Standard Characteristics(V_{DD} = 5V,Ta =25℃)

APPLICATION CIRCUIT



PACKAGE OUTLINE

DIP-16-300-2.54 UNIT: mm



SOP-16-300-1.27 UNIT:mm