

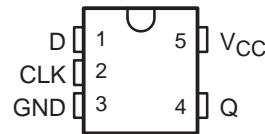
SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

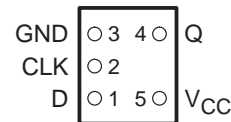
SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	SN74LVC1G79YEAR	--_CR_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC1G79YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LV1G79YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LV1G79YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G79DBVR	C79_
		Reel of 250	SN74LVC1G79DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G79DCKR	CR_
		Reel of 250	SN74LVC1G79DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN74LVC1G79
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

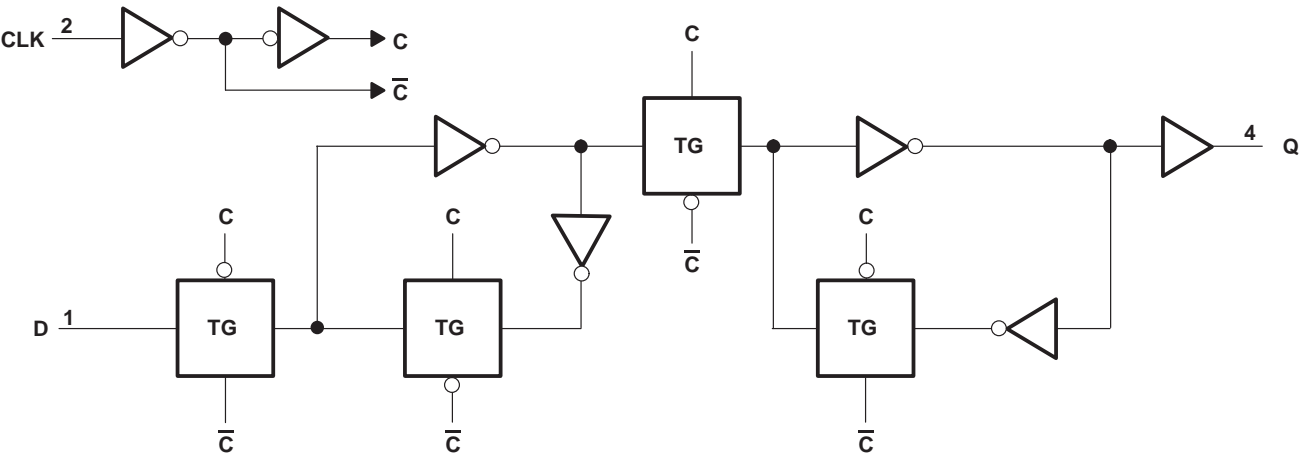
SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE		
INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q_0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	206°C/W
DCV package	252°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4	mA
		V _{CC} = 2.3 V	–8	
		V _{CC} = 3 V	–16	
			–24	
		V _{CC} = 4.5 V	–32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 3 V	16	
			24	
		V _{CC} = 4.5 V	32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20	ns/V
		V _{CC} = 3.3 V ± 0.3 V	10	
		V _{CC} = 5 V ± 0.5 V	5	
T _A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 5.5 V	V _{CC} –0.1			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.9			
		I _{OH} = –16 mA	3 V	2.4			
		I _{OH} = –24 mA		2.3			
		I _{OH} = –32 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 100 µA	1.65 V to 5.5 V	0.1			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.3			
		I _{OL} = 16 mA	3 V	0.4			
		I _{OL} = 24 mA		0.55			
		I _{OL} = 32 mA	4.5 V	0.55			
I _I	CLK or D inputs	V _I = 5.5 V or GND	0 to 5.5 V	±10			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			µA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			µA
C _i		V _I = V _{CC} or GND	3.3 V	4			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.2		1.4		1.3		1.2		ns
		Data low	2.6		1.4		1.3		1.2		
t _h	Hold time, data after CLK↑		0.3		0.4		1		0.5		ns

SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{\max}			160		160		160		160		MHz
t_{pd}	CLK	Q	2.5	9.1	1.2	6	1	4	0.8	3.8	ns

switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{\max}			160		160		160		160		MHz
t_{pd}	CLK	Q	3.9	9.9	2	7	1.7	5	1	4.5	ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 \text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10 \text{ MHz}$	26	26	27	30	pF



SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

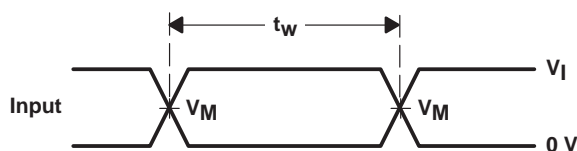
PARAMETER MEASUREMENT INFORMATION



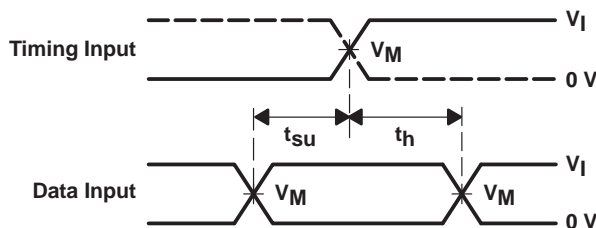
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

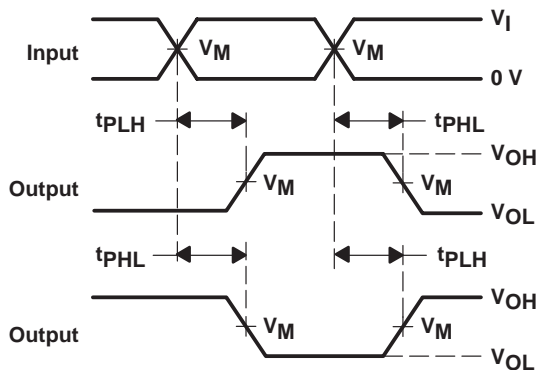
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



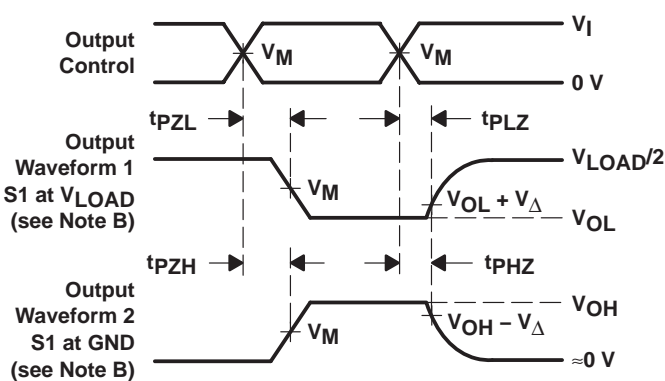
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

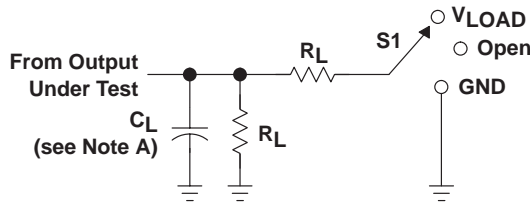
Figure 1. Load Circuit and Voltage Waveforms

SN74LVC1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220N – APRIL 1999 – REVISED SEPTEMBER 2003

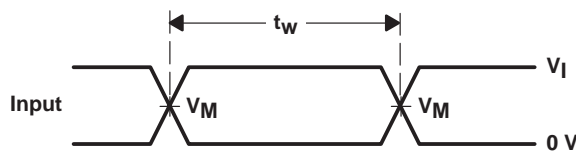
PARAMETER MEASUREMENT INFORMATION



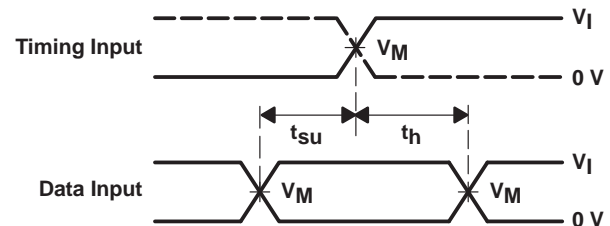
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

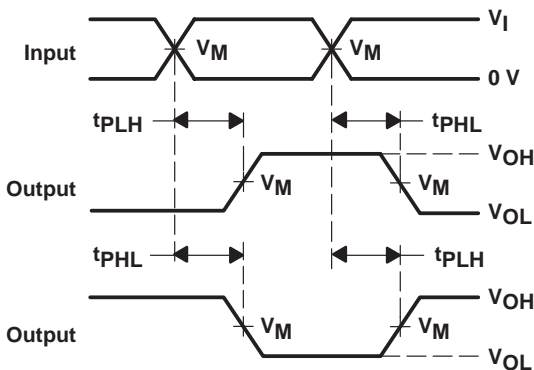
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



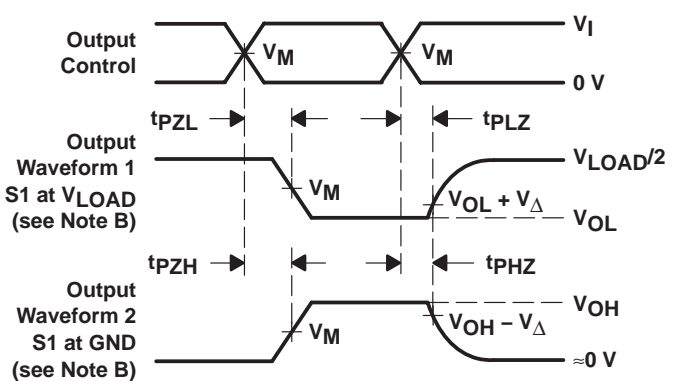
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G79DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G79DBVT	ACTIVE	SOT-23	DBV	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G79DCKR	ACTIVE	SC70	DCK	5	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G79DCKT	ACTIVE	SC70	DCK	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G79YEAR	ACTIVE	WCSP	YEA	5	3000	None	SNPB	Level-1-260C-UNLIM
SN74LVC1G79YEPR	ACTIVE	WCSP	YEP	5	3000	None	SNPB	Level-1-260C-UNLIM
SN74LVC1G79YZAR	ACTIVE	WCSP	YZA	5	3000	None	Call TI	Call TI
SN74LVC1G79YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

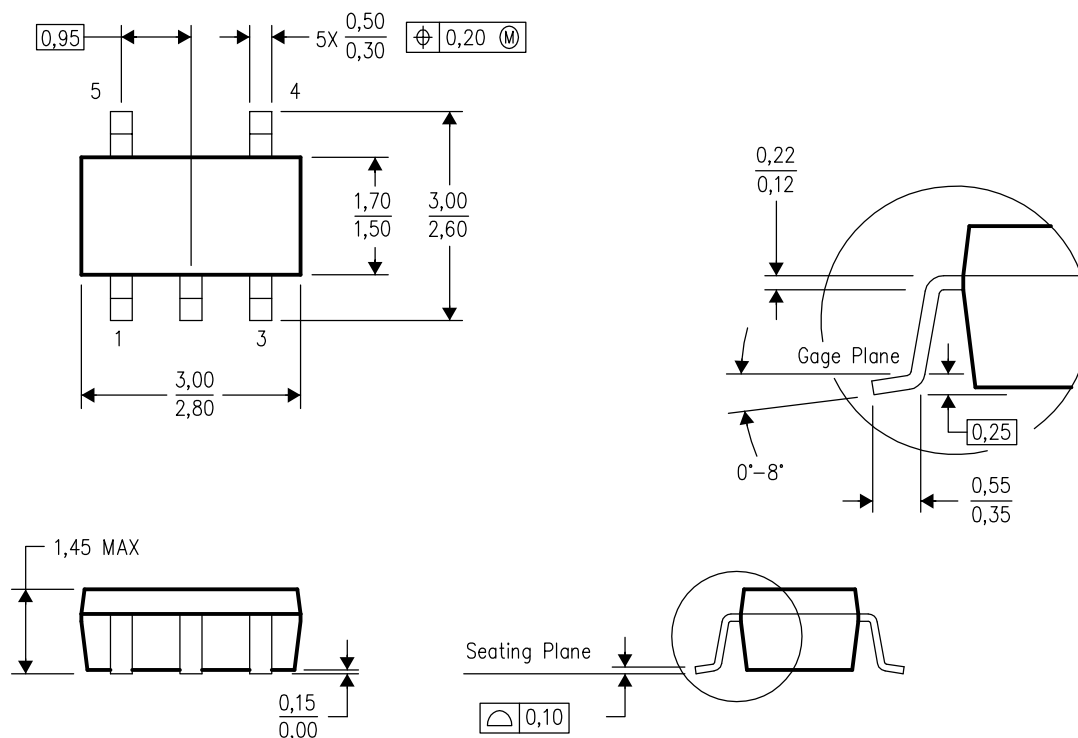
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

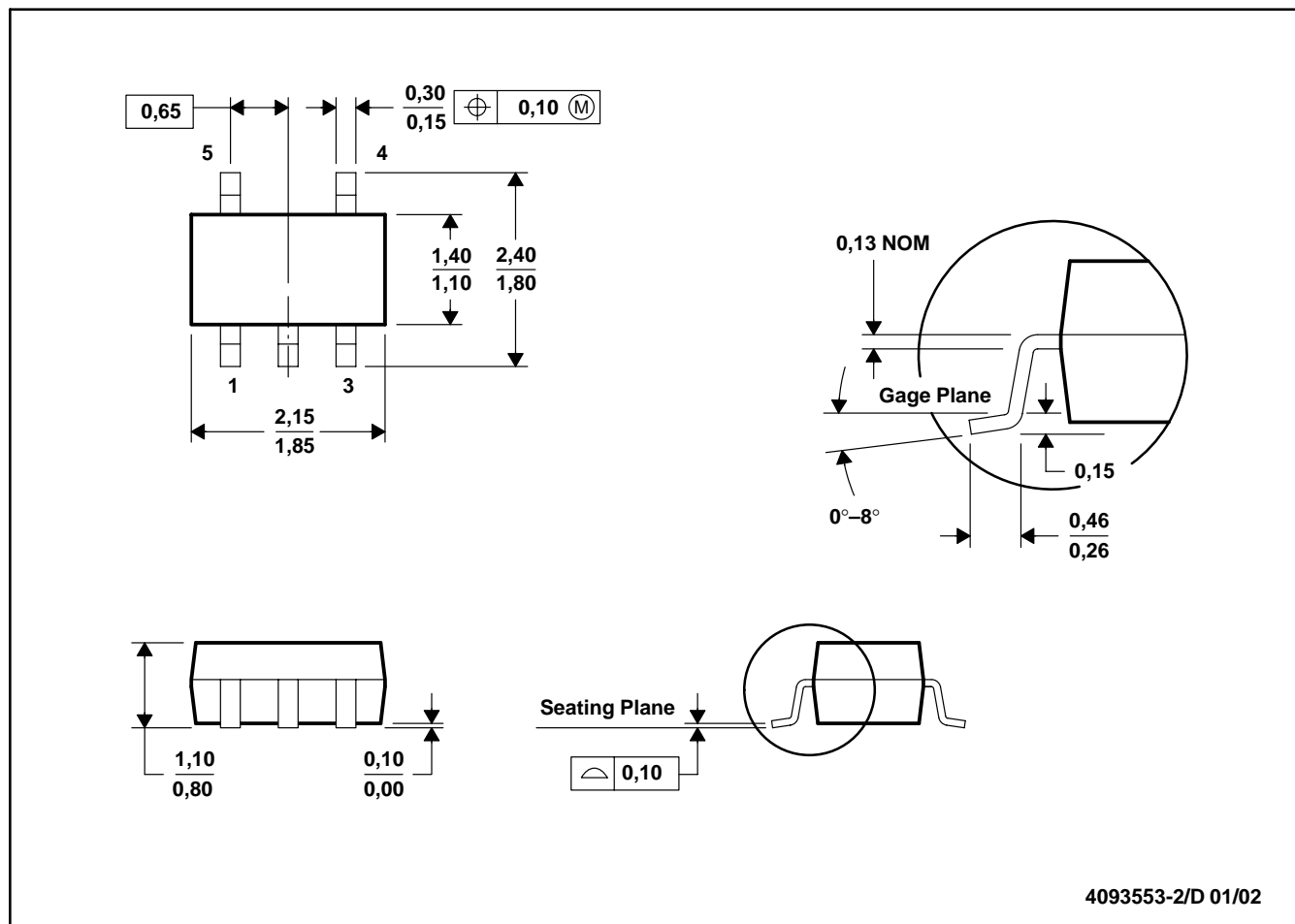


4073253-4/H 10/2003

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178 Variation AA.

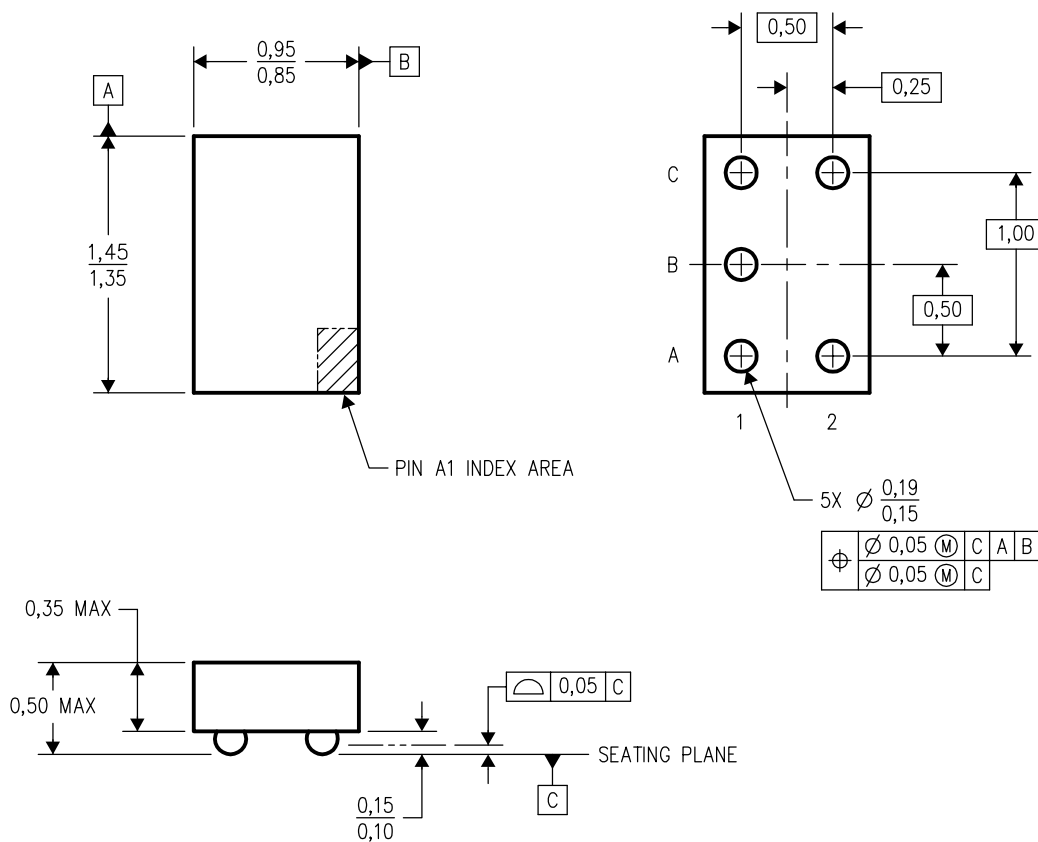
DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



YEA (R-XBGA-N5)

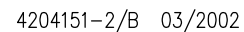
DIE-SIZE BALL GRID ARRAY



4203167-2/C 04/2002

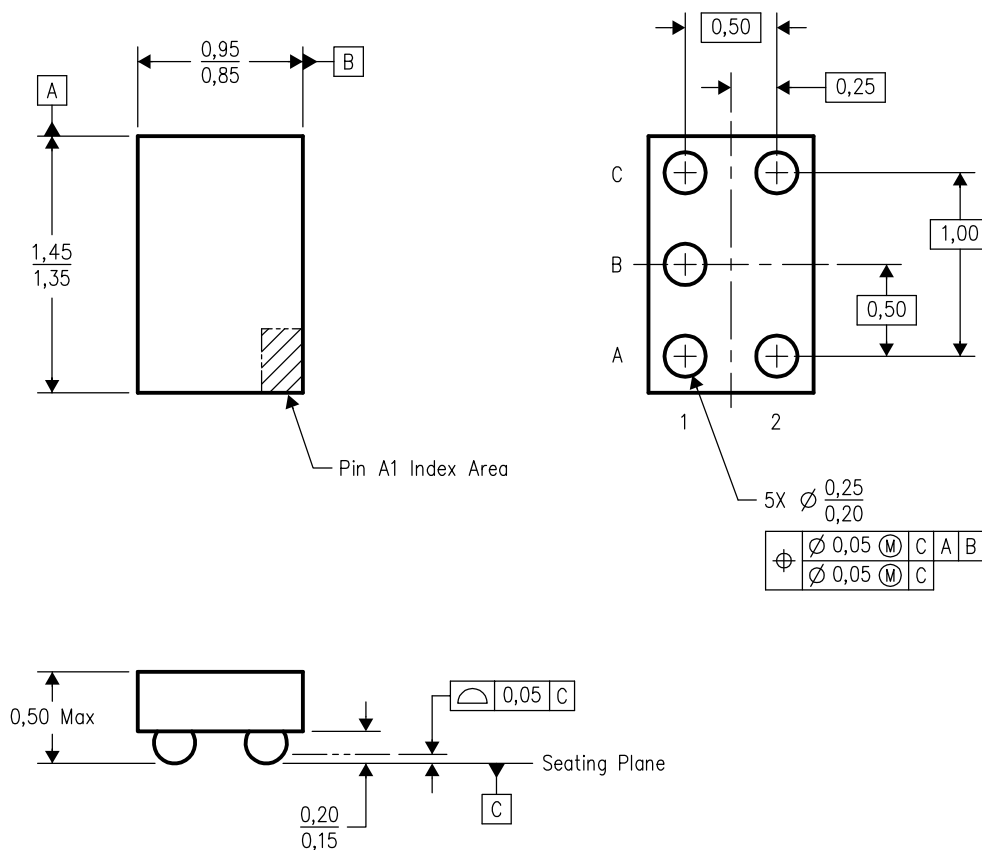
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



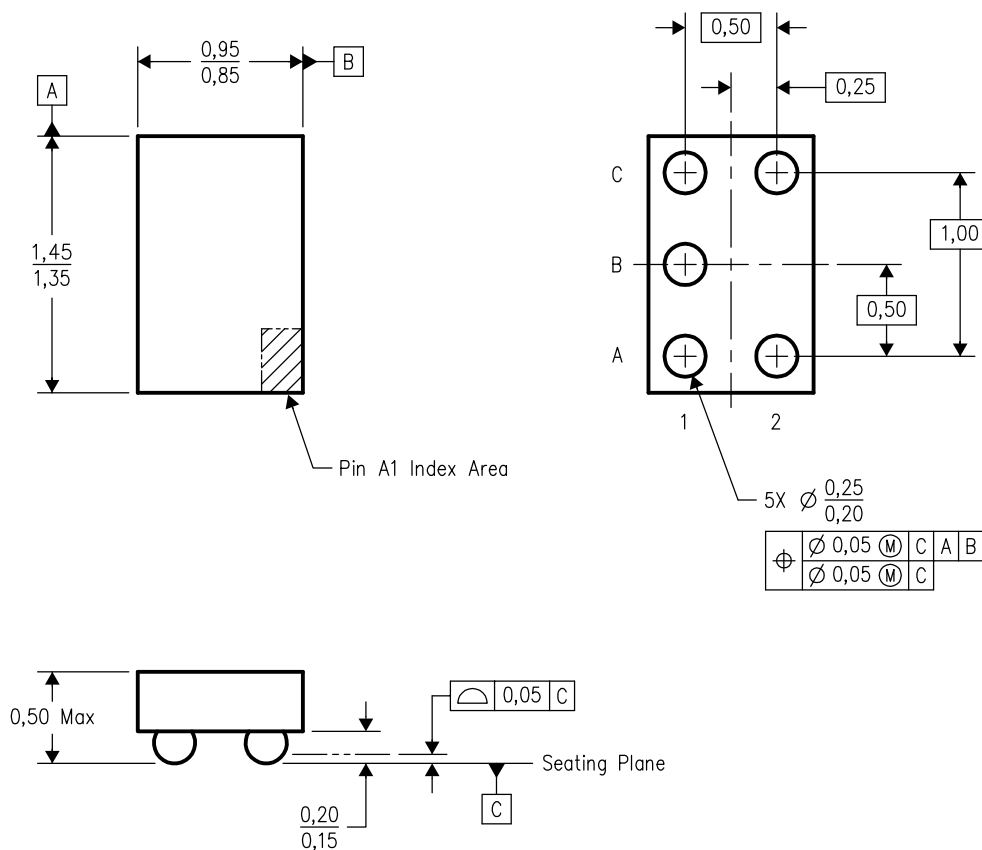
4204741-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated