DMOS Microstepping Driver with Translator And Overcurrent Protection

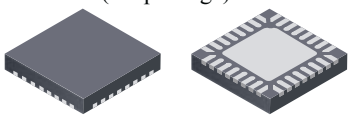
Features and Benefits

- Low $R_{DS(ON)}$ outputs
- Automatic current decay mode detection/selection
- Mixed and Slow current decay modes
- Synchronous rectification for low power dissipation
- Internal UVLO
- Crossover-current protection
- 3.3 and 5 V compatible logic supply
- Thin profile QFN and TSSOP packages
- Thermal shutdown circuitry
- Short-to-ground protection
- Shorted load protection
- Low current Sleep mode, < 10 µA
- No smoke no fire (NSNF) compliance (ET package)

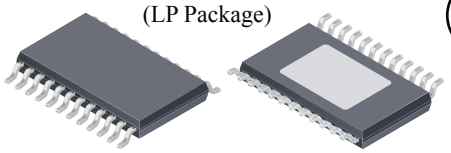
Packages:

32-contact QFN
with exposed thermal pad
5 mm × 5 mm × 0.90 mm
(ET package)

Approximate size



24-pin TSSOP
with exposed thermal pad
(LP Package)



Description

The A4982 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes, with an output drive capacity of up to 35 V and ±2 A. The A4982 includes a fixed off-time current regulator which has the ability to operate in Slow or Mixed decay modes.

The ET package meets customer requirements for no smoke no fire (NSNF) designs by adding no-connect pins between critical output, sense, and supply pins. So, in the case of a pin-to-adjacent-pin short, the device does not cause smoke or fire. Additionally, the device does not cause smoke or fire when any pin is shorted to ground or left open.

The translator is the key to the easy implementation of the A4982. Simply inputting one pulse on the STEP input drives the motor one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The A4982 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

During stepping operation, the chopping control in the A4982 automatically selects the current decay mode, Slow or Mixed. In Mixed decay mode, the device is set initially to a fast decay for a proportion of the fixed off-time, then to a slow decay for the remainder of the off-time. Mixed decay current control

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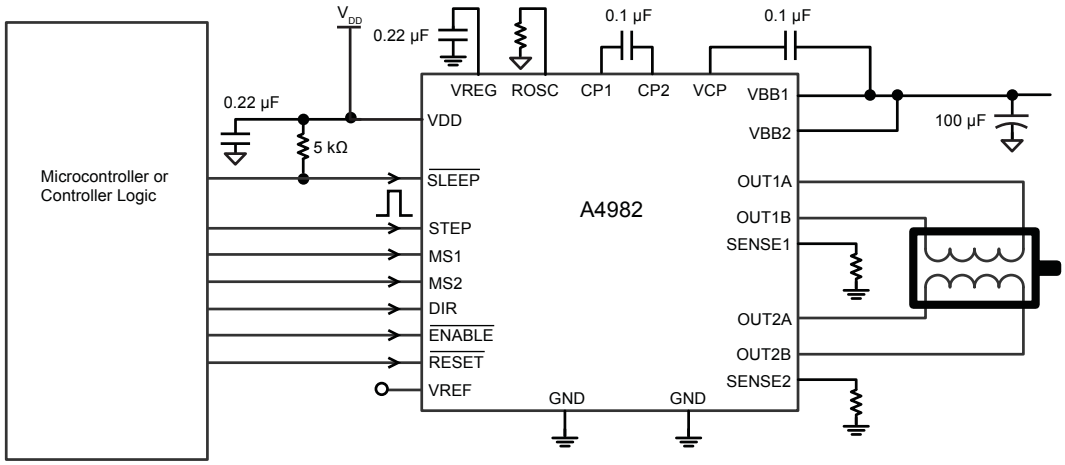
Typical Application Diagram



Description (continued)

results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes: thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-on sequencing is not required.

The A4982 is supplied in two surface mount package, the ET, a 5 mm × 5 mm, 0.90 mm nominal overall package height QFN package, and the LP package, a 24-pin TSSOP. Both packages have exposed pads for enhanced thermal dissipation, and are lead (Pb) free (suffix –T), with 100% matte tin plated leadframes.

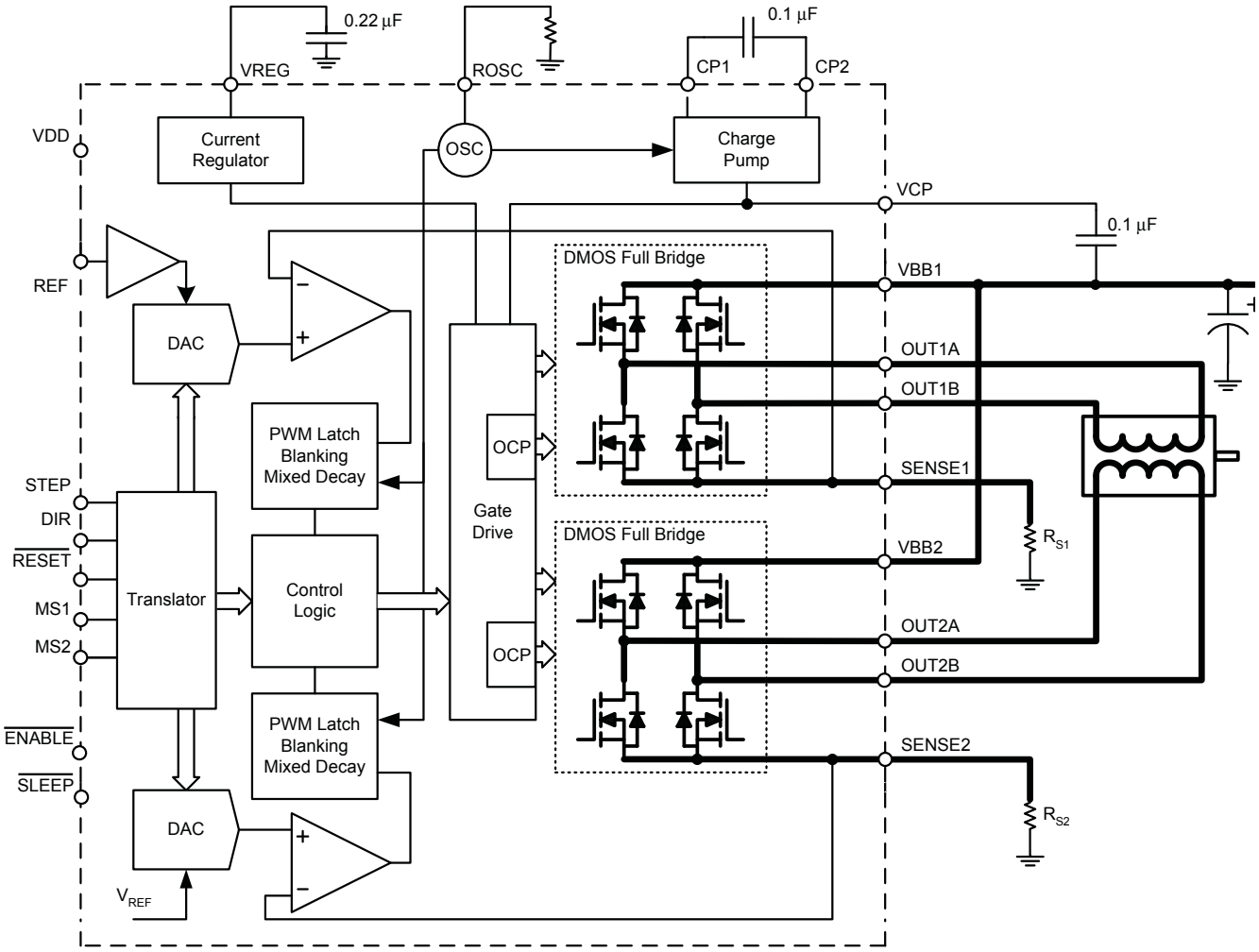
Selection Guide

Part Number	Package	Packing
A4982SETTR-T	32-pin QFN with exposed thermal pad	1500 pieces per 7-in. reel
A4982SLPTR-T	24-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		35	V
Output Current	I_{OUT}		±2	A
Logic Input Voltage	V_{IN}		–0.3 to 5.5	V
Logic Supply Voltage	V_{DD}		–0.3 to 5.5	V
Motor Outputs Voltage			–2.0 to 37	V
Sense Voltage	V_{SENSE}		–0.5 to 0.5	V
Reference Voltage	V_{REF}		5.5	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{BB} = 35 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	35	V
		During Sleep Mode	0	–	35	V
Logic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
Output On Resistance	R_{DSON}	Source Driver, I_{OUT} = –1.5 A	–	320	430	mΩ
		Sink Driver, I_{OUT} = 1.5 A	–	320	430	mΩ
Body Diode Forward Voltage	V_F	Source Diode, I_F = –1.5 A	–	–	1.3	V
		Sink Diode, I_F = 1.5 A	–	–	1.3	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	4	mA
		Operating, outputs disabled	–	–	2	mA
		Sleep Mode	–	–	10	μA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	8	mA
		Outputs off	–	–	5	mA
		Sleep Mode	–	–	10	μA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		V_{DD}×0.7	–	–	V
	$V_{IN(0)}$		–	–	V_{DD}×0.3	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}×0.7	–20	<1.0	20	μA
	$I_{IN(0)}$	V_{IN} = V_{DD}×0.3	–20	<1.0	20	μA
Microstep Select	R_{MS1}	MS1 pin	–	100	–	kΩ
	R_{MS2}	MS2 pin	–	33.3	–	kΩ
Logic Input Hysteresis	$V_{HYS(IN)}$	As a % of V_{DD}	5	11	19	%
Blank Time	t_{BLANK}		0.7	1	1.3	μs
Fixed Off-Time	t_{OFF}	OSC = VDD or GND	20	30	40	μs
		R_{OSC} = 25 kΩ	23	30	37	μs
Reference Input Voltage Range	V_{REF}		0	–	4	V
Reference Input Current	I_{REF}		–3	0	3	μA
Current Trip-Level Error[3]	err_I	V_{REF} = 2 V, %$I_{TripMAX}$ = 38.27%	–	–	±15	%
		V_{REF} = 2 V, %$I_{TripMAX}$ = 70.71%	–	–	±5	%
		V_{REF} = 2 V, %$I_{TripMAX}$ = 100.00%	–	–	±5	%
Crossover Dead Time	t_{DT}		100	475	800	ns
Protection						
Overcurrent Protection Threshold[4]	I_{OCPST}		2.1	–	–	A
Thermal Shutdown Temperature	T_{TSD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{TSDHYS}		–	15	–	°C
VDD Undervoltage Lockout	V_{DDUVLO}	V_{DD} rising	2.7	2.8	2.9	V
VDD Undervoltage Hysteresis	$V_{DDUVLOHYS}$		–	90	–	mV

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[3]$V_{ERR} = [(V_{REF}/8) – V_{SENSE}] / (V_{REF}/8)$.

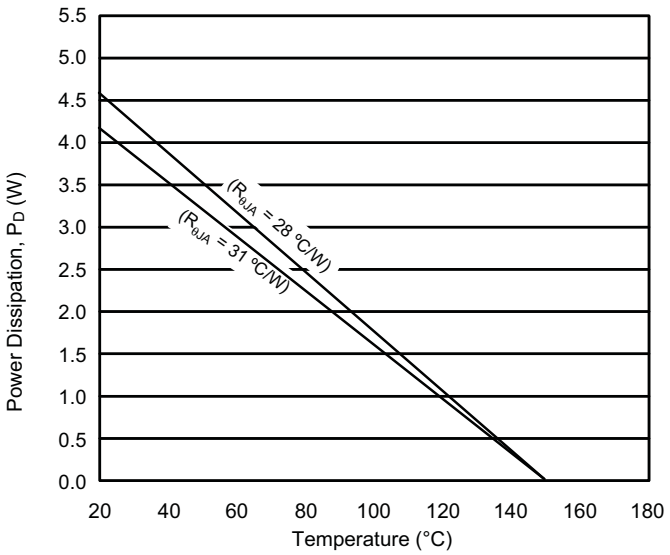
[4]Overcurrent protection (OCP) is tested at T_A = 25°C in a restricted range and guaranteed by characterization.

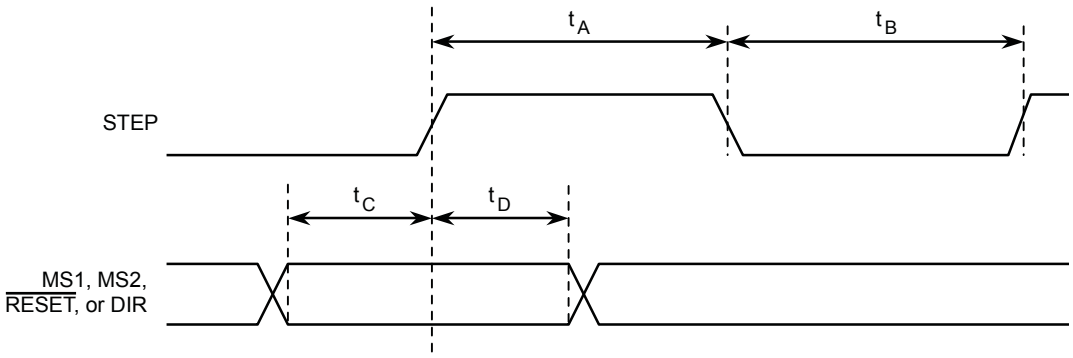
THERMAL CHARACTERISTICS may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	ET package; estimated, on 4-layer PCB, based on JEDEC standard	32	ºC/W
		LP package; on 4-layer PCB, based on JEDEC standard	28	ºC/W

*In still air. Additional thermal information available on Allegro Web site.

Maximum Power Dissipation, $P_{D(max)}$





Time Duration	Symbol	Typ.	Unit
STEP minimum, HIGH pulse width	t_A	1	µs
STEP minimum, LOW pulse width	t_B	1	µs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
H	L	Half Step	1-2 Phase
L	H	Quarter Step	W1-2 Phase
H	H	Sixteenth Step	4W1-2 Phase

Functional Description

Device Operation. The A4982 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step resolution modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PWM (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (R_{S1} and R_{S2}), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state (shown in figures 10 through 13), and the current regulator to Mixed decay mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See table 2 for the current-level sequence.) The microstep resolution is set by the combined effect of the MSx inputs, as shown in table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode for the active full-bridge is set to Mixed. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to Slow. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

Microstep Select (MS1 and MS2). The microstep resolution is set by the voltage on logic inputs MS1 and MS2, as shown in table 1. MS1 has a 100 kΩ pull-down resistance, and MS2 has a 33.3 kΩ pull-down resistance. When changing the step mode the change does not take effect until the next STEP rising edge.

If the step mode is changed without a translator reset, and absolute position must be maintained, it is important to change the step mode at a step position that is common to both step modes in order to avoid missing steps. When the device is powered down, or reset due to TSD or an overcurrent event the translator is set to the home position which is by default common to all step modes.

Low Current Microstepping. Intended for applications where the minimum on-time prevents the output current from regulating to the programmed current level at low current steps. To prevent this, the device can be set to operate in Mixed decay mode on both rising and falling portions of the current waveform. This feature is implemented by shorting the ROSC pin to ground. In this state, the off-time is internally set to 30 µs.

Reset Input ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ input sets the translator to a predefined Home state (shown in figures 10 through 13), and turns off all of the FET outputs. All STEP inputs are ignored until the $\overline{\text{RESET}}$ input is set to high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of inputs MS1 and MS2.

Direction Input (DIR). This determines the direction of rotation of the motor. Changes to this input do not take effect until the next STEP rising edge.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx}. When the voltage across R_{Sx} equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off either the source FET (when in Slow decay mode) or the sink and source FETs (when in Mixed decay mode).

The maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF pin. The transconductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

where R_S is the resistance of the sense resistor (Ω) and V_{REF} is the input voltage on the REF pin (V).

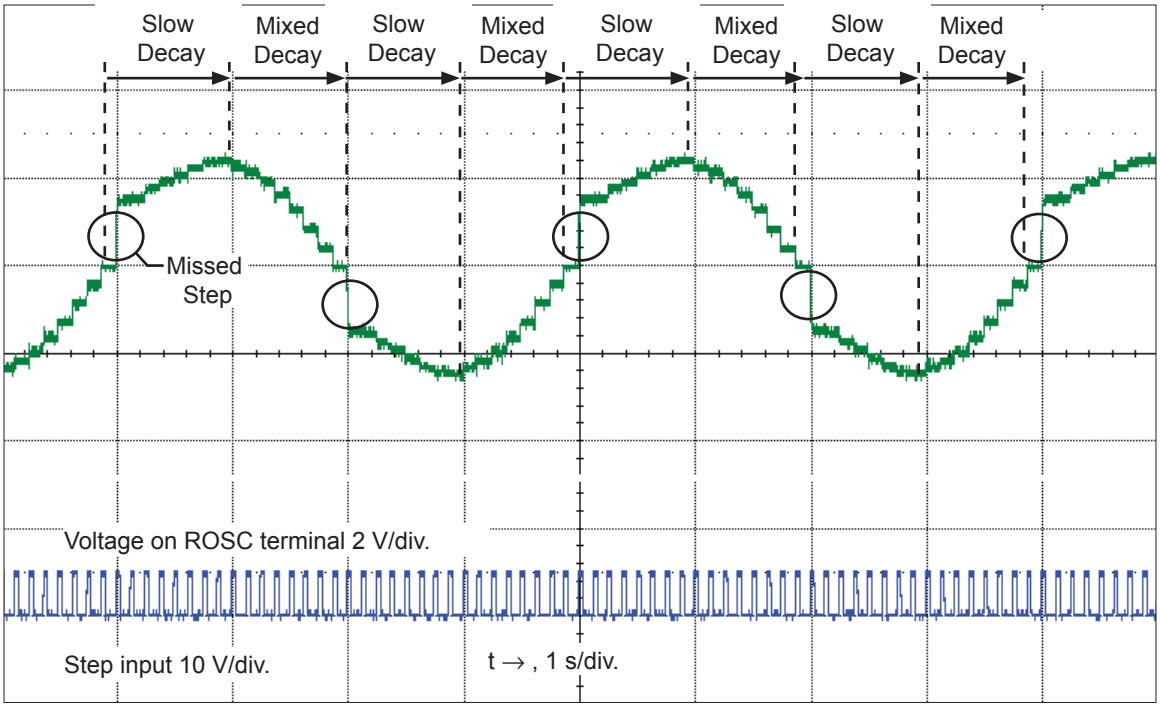


Figure 2. Missed steps in low-speed microstepping

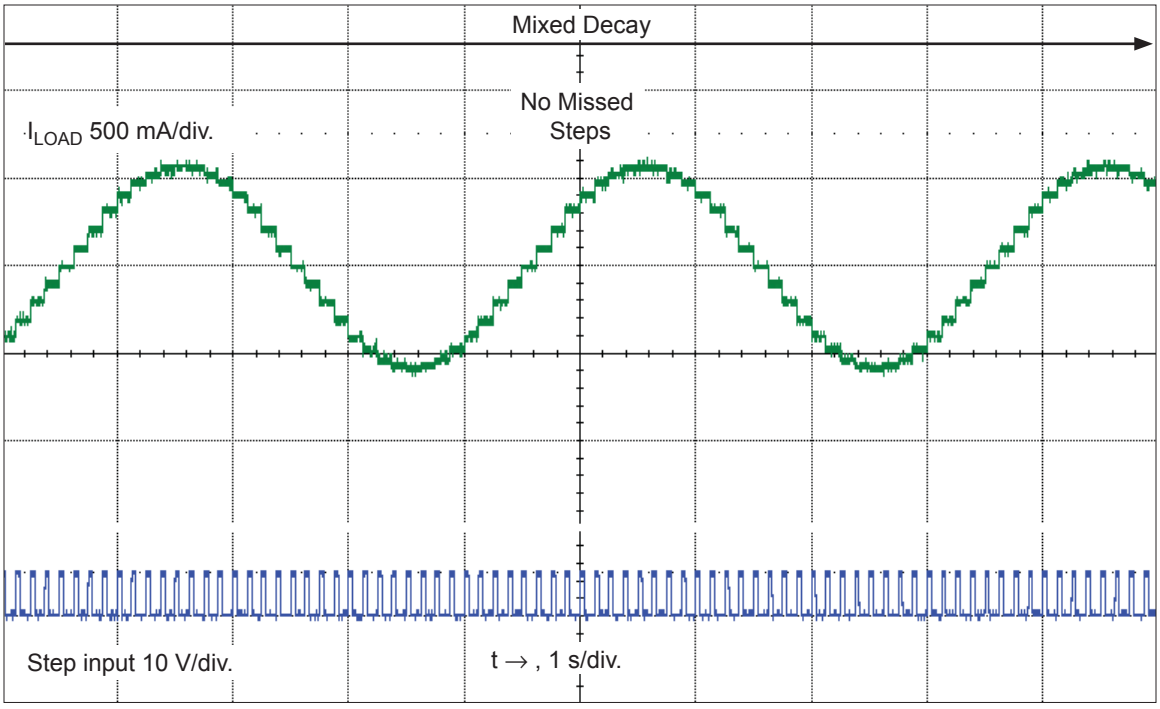


Figure 3. Continuous stepping using automatically-selected mixed stepping (ROSC pin grounded)

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

(See table 2 for $\%I_{TripMAX}$ at each step.)

It is critical that the maximum rating (0.5 V) on the SENSE1 and SENSE2 pins is not exceeded.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The off-time, t_{OFF}, is determined by the ROSC terminal. The ROSC terminal has three settings:

- ROSC tied to VDD — off-time internally set to 30 µs, decay mode is automatic Mixed decay except when in full step where decay mode is set to Slow decay
- ROSC tied directly to ground — off-time internally set to 30 µs, current decay is set to Mixed decay for both increasing and decreasing currents, except in full step where decay mode is set to Slow decay. (See Low Current Microstepping section.)
- ROSC through a resistor to ground — off-time is determined by the following formula , the decay mode is automatic Mixed decay for all step modes.

$$t_{OFF} \approx R_{OSC} / 825$$

Where t_{OFF} is in µs.

Blanking. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (µs), is approximately

$$t_{BLANK} \approx 1 \text{ µs}$$

Shorted-Load and Short-to-Ground Protection. If the motor leads are shorted together, or if one of the leads is shorted to ground, the driver will protect itself by sensing the overcurrent event and disabling the driver that is shorted, protecting the device from damage. In the case of a short-to-ground, the device will remain disabled (latched) until the $\overline{\text{SLEEP}}$ input goes high or VDD power is removed. A short-to-ground overcurrent event is shown in figure 4.

When the two outputs are shorted together, the current path is through the sense resistor. After the blanking time (≈1 µs) expires, the sense resistor voltage is exceeding its trip value, due to the overcurrent condition that exists. This causes the driver to go into a fixed off-time cycle. After the fixed off-time expires the driver turns on again and the process repeats. In this condition the driver is completely protected against overcurrent events, but the short is repetitive with a period equal to the fixed off-time of the driver. This condition is shown in figure 5.

If the driver is operating in Mixed decay mode, it is normal for the positive current to spike, due to the bridge going in the forward direction and then in the negative direction, as a result of the direction change implemented by the Mixed decay feature. This is shown in figure 6. In both instances the overcurrent circuitry is protecting the driver and prevents damage to the device.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side FET gates. A 0.1 µF ceramic capacitor, should be connected between CP1 and CP2. In addition, a 0.1 µF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side FET gates.

Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

V_{REG} (VREG). This internally-generated voltage is used to operate the sink-side FET outputs. The nominal output voltage of the VREG terminal is 7 V. The VREG pin must be decoupled with a 0.22 µF ceramic capacitor to ground. V_{REG} is internally monitored. In the case of a fault condition, the FET outputs of the A4982 are disabled.

Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

Enable Input ($\overline{\text{ENABLE}}$). This input turns on or off all of the FET outputs. When set to a logic high, the outputs are disabled. When set to a logic low, the internal control enables the outputs as required. The translator inputs STEP, DIR, MS1, and MS2, as well as the internal sequencing logic, all remain active, independent of the $\overline{\text{ENABLE}}$ input state.

Shutdown. In the event of a fault, overtemperature (excess T_J) or an undervoltage (on VCP), the FET outputs of the A4982 are disabled until the fault condition is removed. At power-on, the UVLO (undervoltage lockout) circuit disables the FET outputs and resets the translator to the Home state.

Sleep Mode ($\overline{\text{SLEEP}}$). To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output FETs, current regulator, and charge pump. A logic low on the $\overline{\text{SLEEP}}$ pin puts the A4982 into Sleep mode. A logic high allows normal operation, as well as start-up (at which time the A4982 drives the motor to the Home microstep position). When emerging from Sleep mode, in order to allow the charge pump to stabilize, provide a delay of 1 ms before issuing a Step command.

Mixed Decay Operation. The bridge operates in Mixed decay mode, at power-on and reset, and during normal running according to the ROSC configuration and the step sequence, as shown in figures 3 through 6. During Mixed decay, when the trip point is reached, the A4982 initially goes into a fast decay mode for 31.25% of the off-time, t_{OFF}. After that, it switches to Slow decay mode for the remainder of t_{OFF}. A timing diagram for this feature appears in figure7.

Typically, mixed decay is only necessary when the current in the winding is going from a higher value to a lower value as determined by the state of the translator. For most loads automatically-selected mixed decay is convenient because it minimizes ripple when the current is rising and prevents missed steps when the current is falling. For some applications where microstepping at very low speeds is necessary, the lack of back EMF in the winding causes the current to increase in the load quickly, resulting in missed steps. This is shown in figure 2. By pulling the ROSC pin to ground, mixed decay is set to be active 100% of the time, for both rising and falling currents, and prevents missed steps as shown in figure 3. If this is not an issue, it is recommended that automatically-selected mixed decay be used, because it will produce reduced ripple currents. Refer to the Fixed Off-Time section for details.

Synchronous Rectification. When a PWM-off cycle is triggered by an internal fixed-off-time cycle, load current recirculates according to the decay mode selected by the control logic. This synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low FET $R_{DS(ON)}$. This reduces power dissipation significantly, and can eliminate the need for external Schottky diodes in many applications. Synchronous rectification turns off when the load current approaches zero (0 A), preventing reversal of the load current.

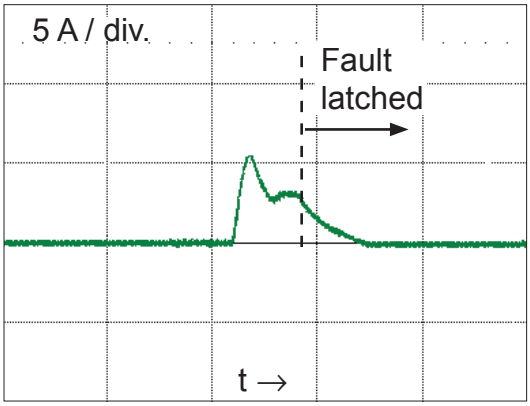


Figure 4. Short-to-ground event

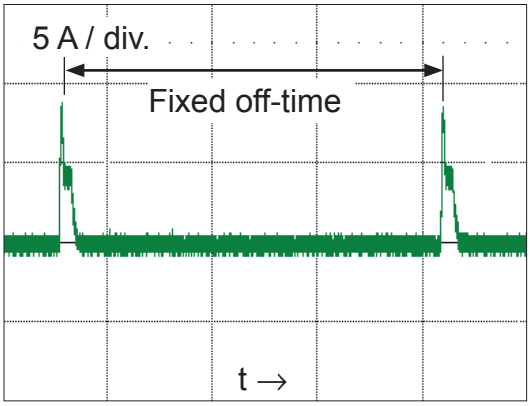


Figure 5. Shorted load (OUTxA → OUTxB) in Slow decay mode

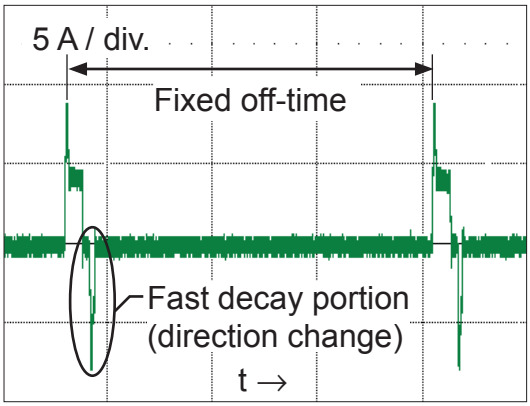
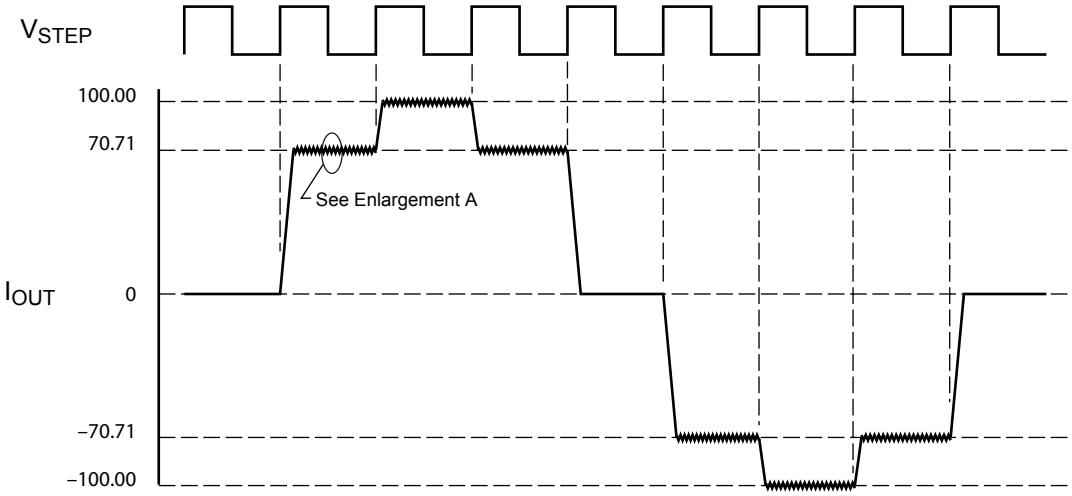
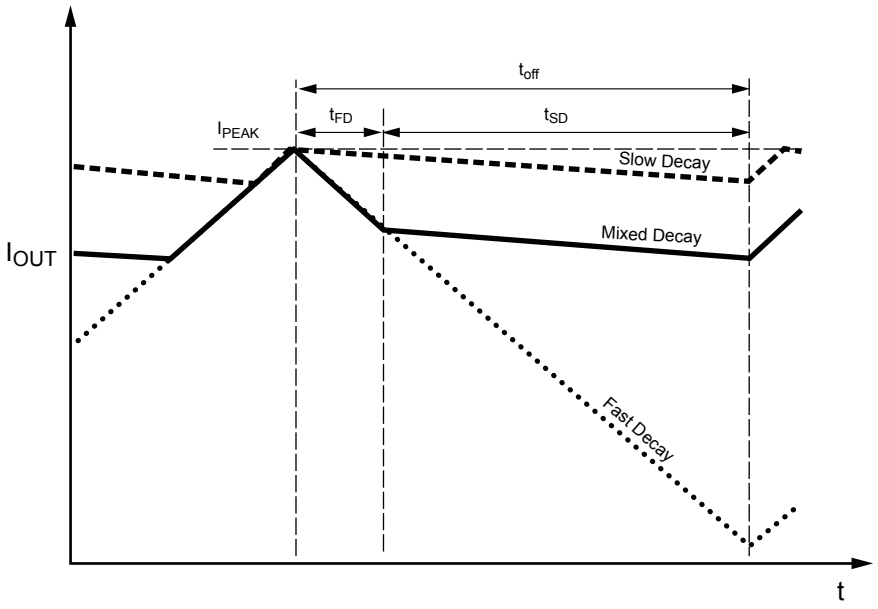


Figure 6. Shorted load (OUTxA → OUTxB) in Mixed decay mode



Enlargement A



Symbol	Characteristic
t_{off}	Device fixed off-time
I_{PEAK}	Maximum output current
t_{SD}	Slow decay interval
t_{FD}	Fast decay interval
I_{OUT}	Device output current

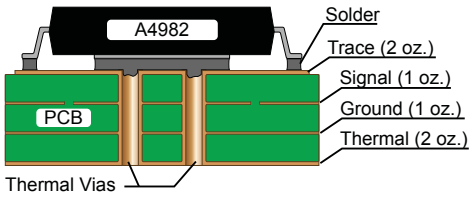
Figure 7. Current Decay Modes Timing Chart

Application Layout

Layout. Typical application circuits and layouts are shown in figures 8 (LP package) and 9 (ET package).The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the A4982 must be soldered directly onto the board. On the underside of the A4982 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the pad and the ground plane directly under the A4982, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CIN1) should be closer to the pins than the bulk capacitor (CIN2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components. The sense resistors, RSx , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.



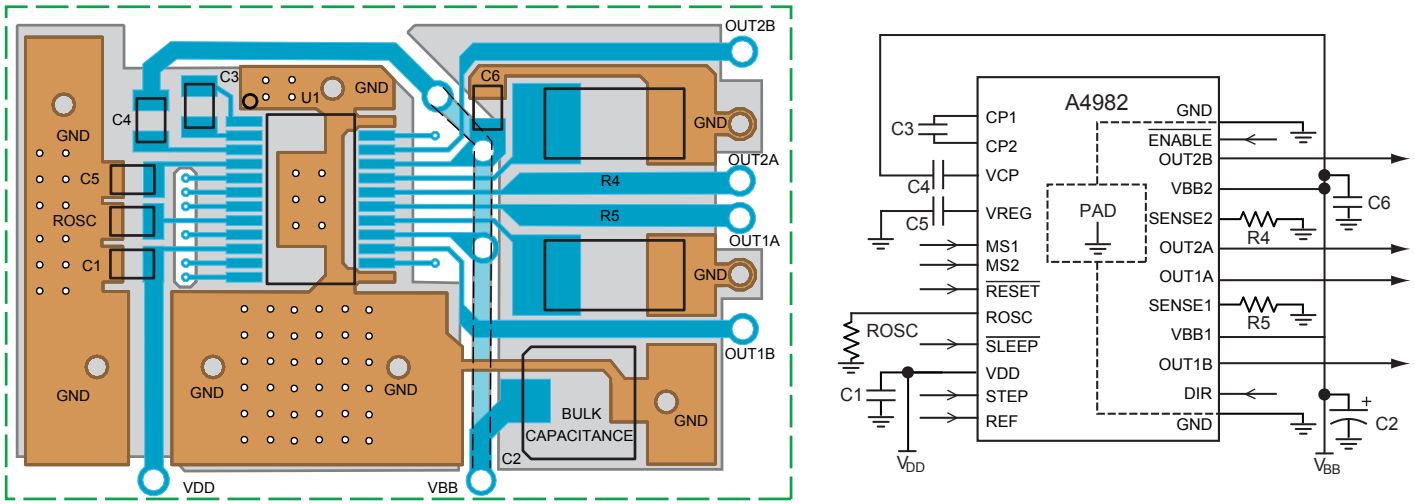


Figure 8. LP package typical application and circuit layout

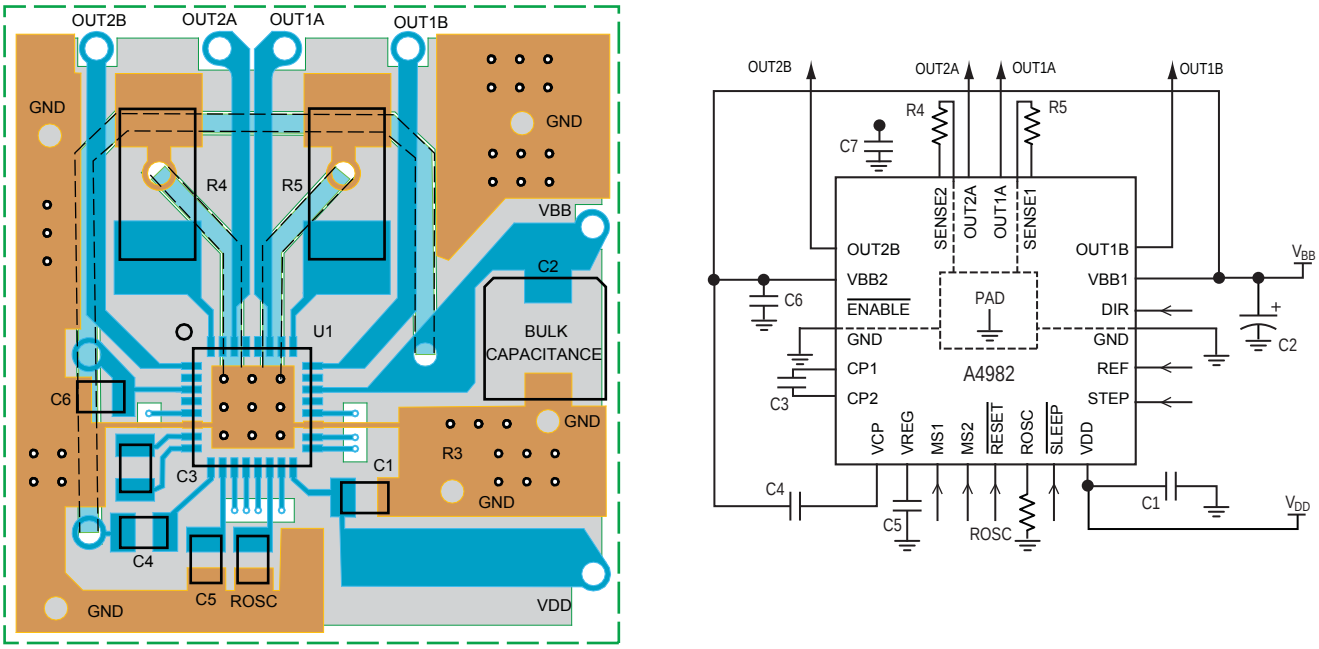
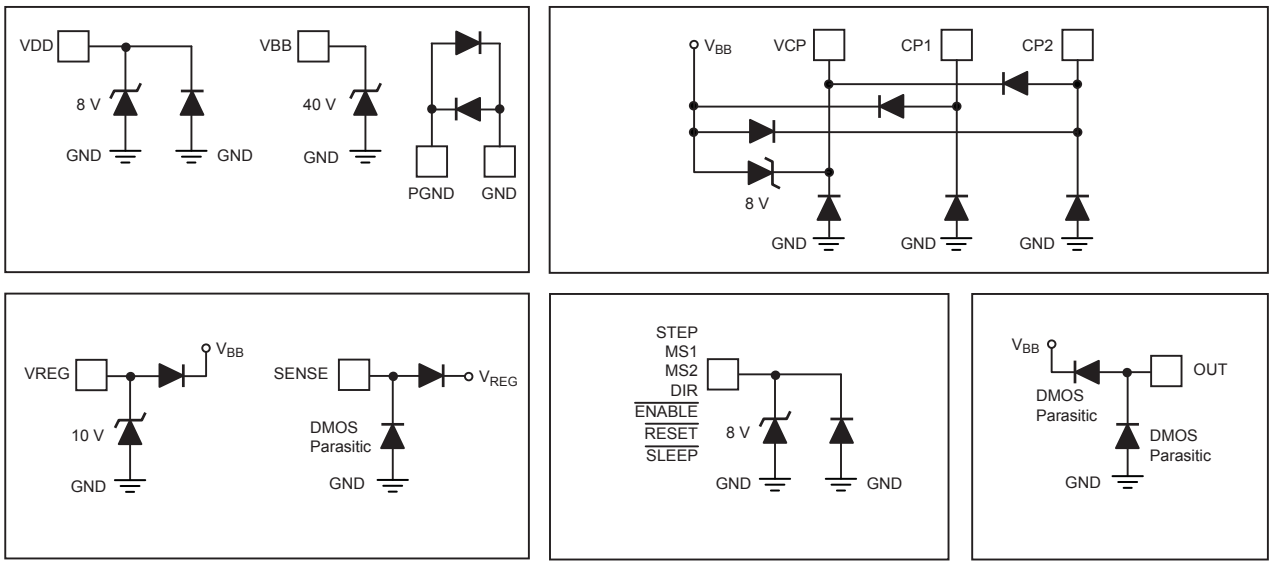


Figure 9. ET package typical application and circuit layout

Pin Circuit Diagrams



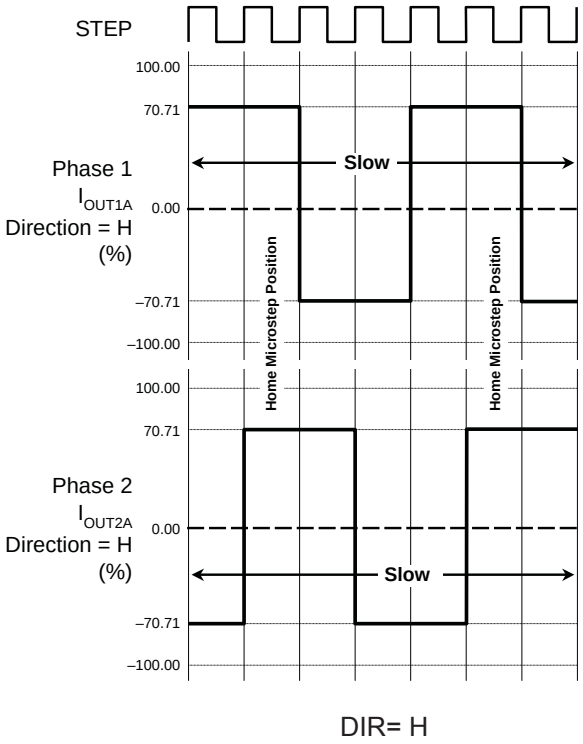


Figure 10. Decay Mode for Full-Step Increments

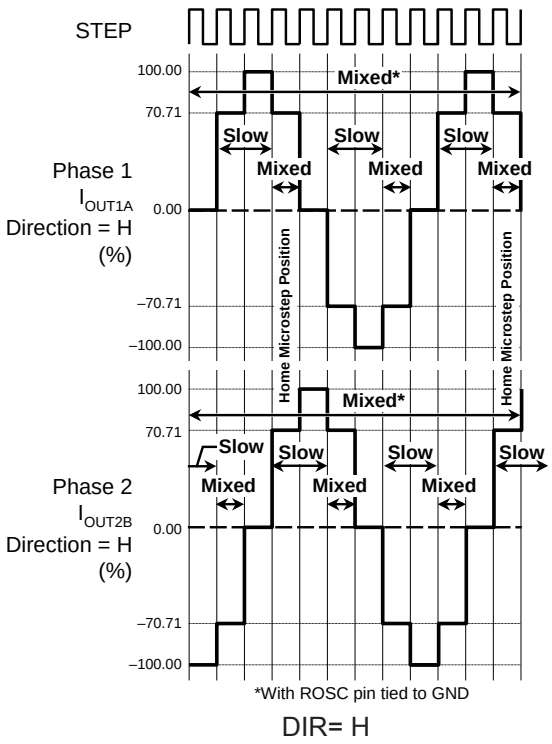


Figure 11. Decay Modes for Half-Step Increments

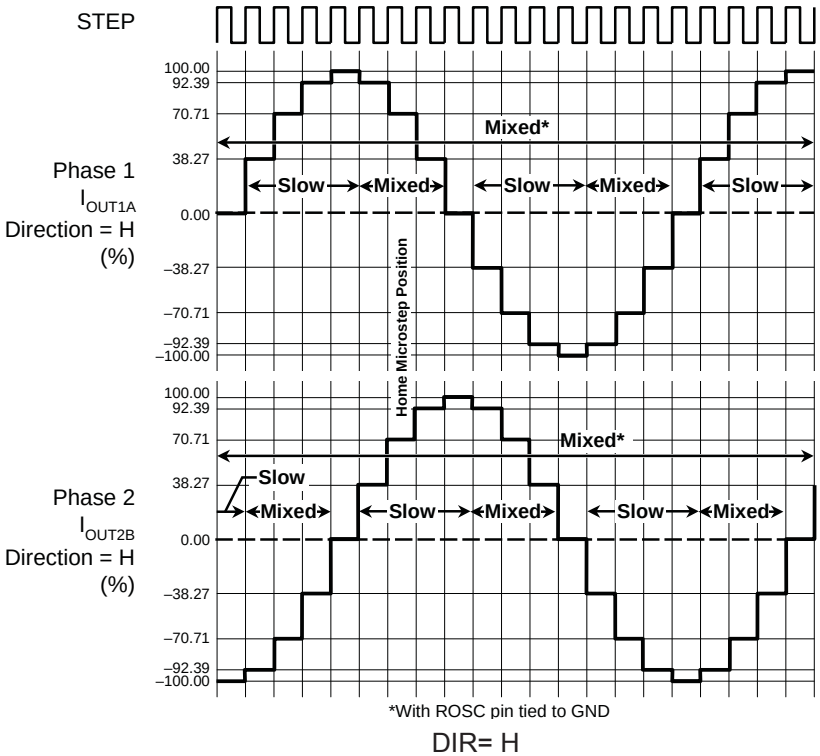


Figure 12. Decay Modes for Quarter-Step Increments

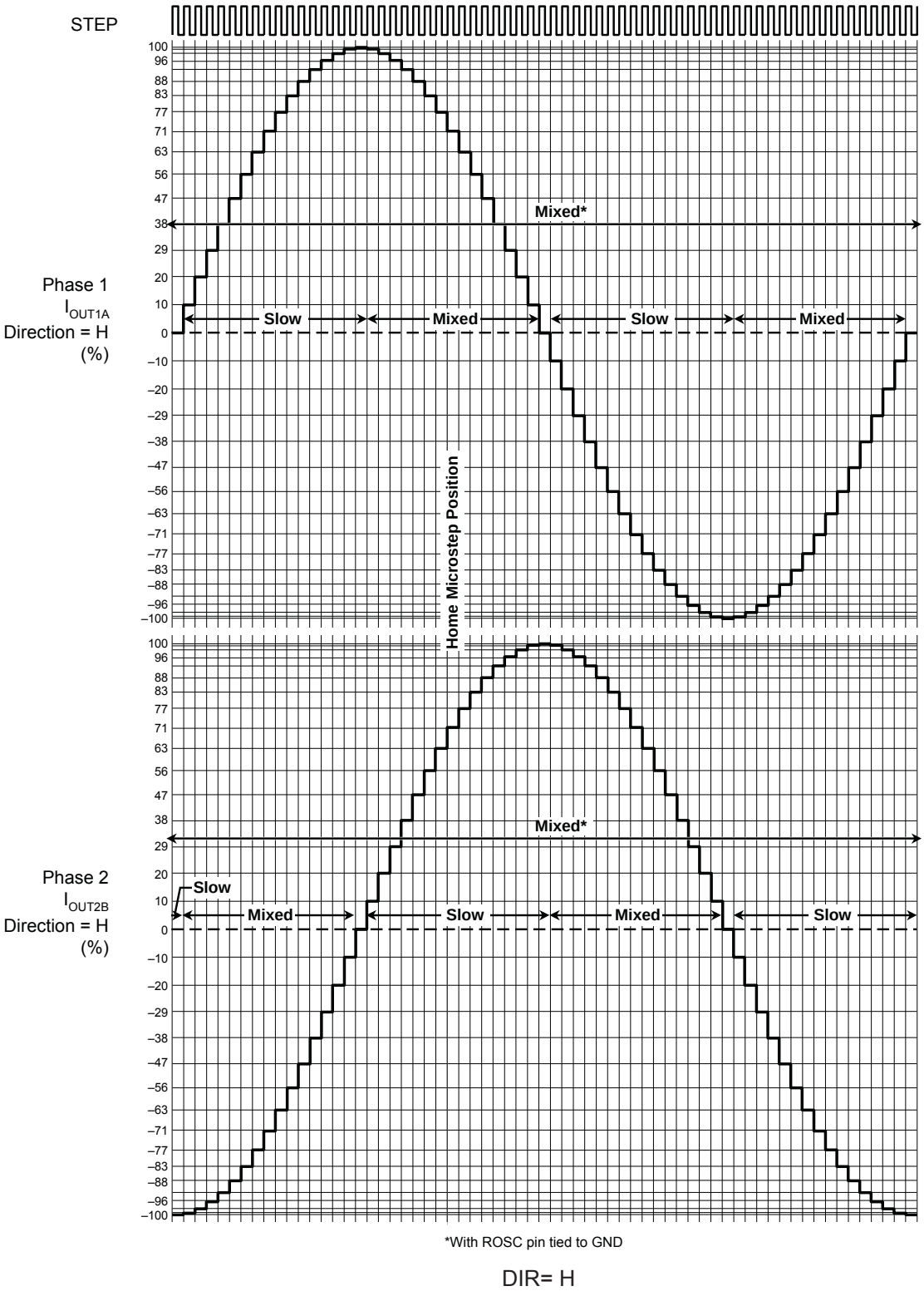


Figure 13. Decay Modes for Sixteenth-Step Increments

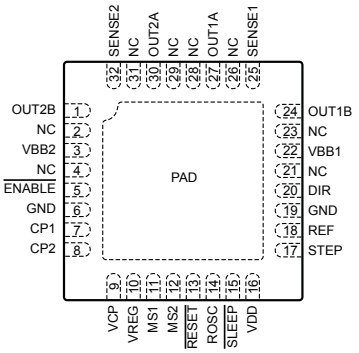
Table 2. Step Sequencing Settings

Home microstep position at Step Angle 45º; DIR = H

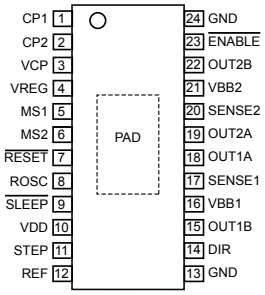
Full Step (#)	Half Step (#)	1/4 Step (#)	1/16 Step (#)	Phase 2 Current (% $I_{TRIP(max)}$)	Phase 1 Current (% $I_{TRIP(max)}$)	Step Angle (°)	Full Step (#)	Half Step (#)	1/4 Step (#)	1/16 Step (#)	Phase 2 Current (% $I_{TRIP(max)}$)	Phase 1 Current (% $I_{TRIP(max)}$)	Step Angle (°)
	1	1	1	0.00	100.00	0.0		5	9	33	0.00	–100.00	180.0
			2	9.38	100.00	5.6				34	–9.38	–100.00	185.6
			3	18.75	98.44	11.3				35	–18.75	–98.44	191.3
			4	29.69	95.31	16.9				36	–29.69	–95.31	196.9
		2	5	37.50	92.19	22.5			10	37	–37.50	–92.19	202.5
			6	46.88	87.50	28.1				38	–46.88	–87.50	208.1
			7	56.25	82.81	33.8				39	–56.25	–82.81	213.8
			8	64.06	76.56	39.4				40	–64.06	–76.56	219.4
1	2	3	9	70.31	70.31	45.0	3	6	11	41	–70.31	–70.31	225.0
			10	76.56	64.06	50.6				42	–76.56	–64.06	230.6
			11	82.81	56.25	56.3				43	–82.81	–56.25	236.3
			12	87.50	46.88	61.9				44	–87.50	–46.88	241.9
		4	13	92.19	37.50	67.5			12	45	–92.19	–37.50	247.5
			14	95.31	29.69	73.1				46	–95.31	–29.69	253.1
			15	98.44	18.75	78.8				47	–98.44	–18.75	258.8
			16	100.00	9.38	84.4				48	–100.00	–9.38	264.4
	3	5	17	100.00	0.00	90.0		7	13	49	–100.00	0.00	270.0
			18	100.00	–9.38	95.6				50	–100.00	9.38	275.6
			19	98.44	–18.75	101.3				51	–98.44	18.75	281.3
			20	95.31	–29.69	106.9				52	–95.31	29.69	286.9
		6	21	92.19	–37.50	112.5			14	53	–92.19	37.50	292.5
			22	87.50	–46.88	118.1				54	–87.50	46.88	298.1
			23	82.81	–56.25	123.8				55	–82.81	56.25	303.8
			24	76.56	–64.06	129.4				56	–76.56	64.06	309.4
2	4	7	25	70.31	–70.31	135.0	4	8	15	57	–70.31	70.31	315.0
			26	64.06	–76.56	140.6				58	–64.06	76.56	320.6
			27	56.25	–82.81	146.3				59	–56.25	82.81	326.3
			28	46.88	–87.50	151.9				60	–46.88	87.50	331.9
		8	29	37.50	–92.19	157.5			16	61	–37.50	92.19	337.5
			30	29.69	–95.31	163.1				62	–29.69	95.31	343.1
			31	18.75	–98.44	168.8				63	–18.75	98.44	348.8
			32	9.38	–100.00	174.4				64	–9.38	100.00	354.4
	5	9	33	0.00	–100.00	180.0		1	1	1	0.00	100.00	360.0

Pin-out Diagrams

ET Package



LP Package

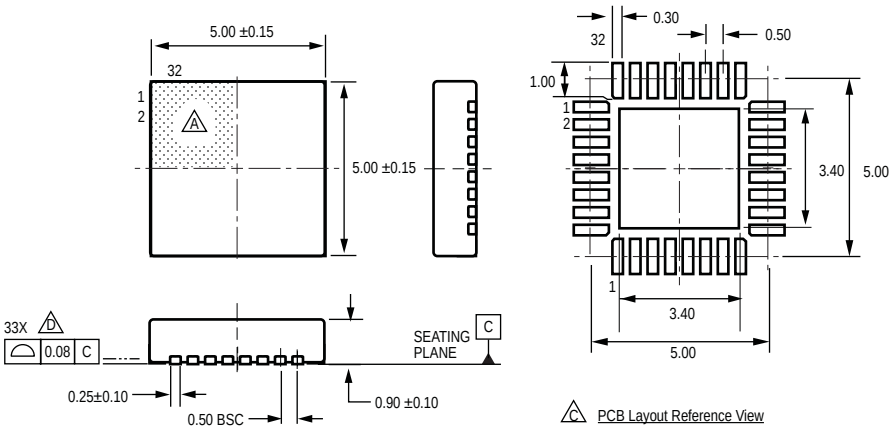


Terminal List Table

Name	Number		Description
	ET[1]	LP	
CP1	7	1	Charge pump capacitor terminal
CP2	8	2	Charge pump capacitor terminal
DIR	20	14	Logic input
$\overline{\text{ENABLE}}$	5	23	Logic input
GND	6, 19	13, 24	Ground[2]
MS1	11	5	Logic input
MS2	12	6	Logic input
NC	2, 4, 21, 23, 26, 28, 29, 31	–	No connection
OUT1A	27	18	DMOS Full Bridge 1 Output A
OUT1B	24	15	DMOS Full Bridge 1 Output B
OUT2A	30	19	DMOS Full Bridge 2 Output A
OUT2B	1	22	DMOS Full Bridge 2 Output B
REF	18	12	G_m reference voltage input
$\overline{\text{RESET}}$	13	7	Logic input
ROSC	14	8	Timing set
SENSE1	25	17	Sense resistor terminal for Bridge 1
SENSE2	32	20	Sense resistor terminal for Bridge 2
$\overline{\text{SLEEP}}$	15	9	Logic input
STEP	17	11	Logic input
VBB1	22	16	Load supply
VBB2	3	21	Load supply
VCP	9	3	Reservoir capacitor terminal
VDD	16	10	Logic supply
VREG	10	4	Regulator decoupling terminal
PAD	–	–	Exposed pad for enhanced thermal dissipation*

*The GND pins must be tied together externally by connecting to the PAD ground plane under the device.

ET Package, 32-Contact QFN with Exposed Thermal Pad



For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-6)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

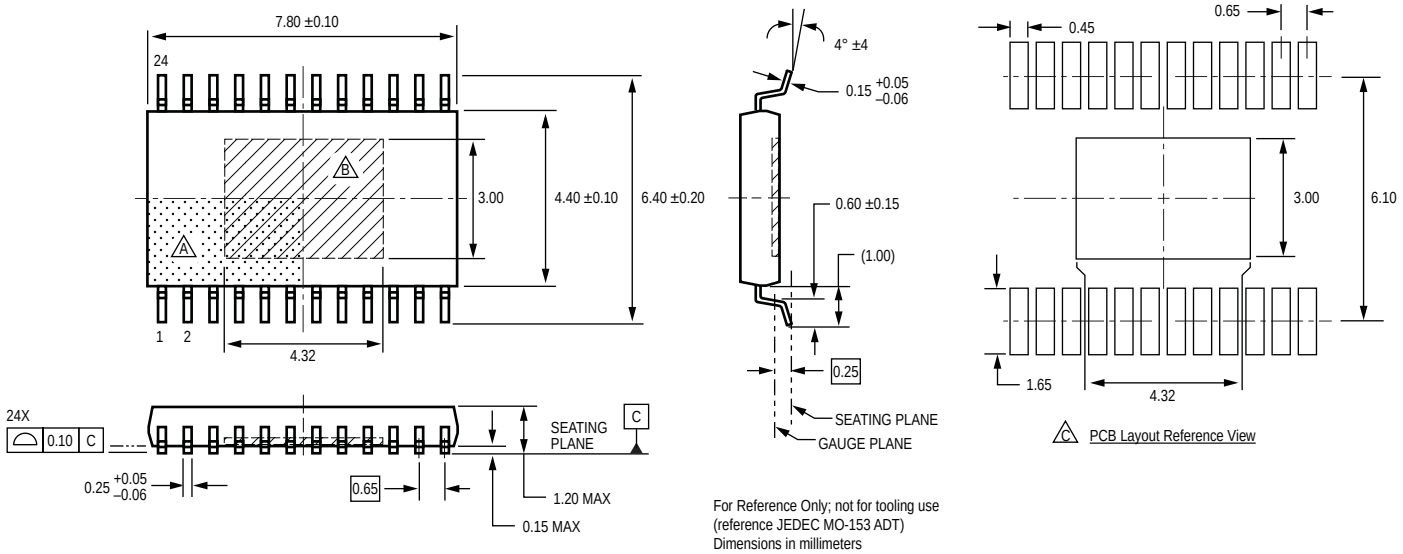
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

LP Package, 24-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use
(reference JEDEC MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 4	March 21, 2012	Update example layout

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