

# SN74CBTS6800

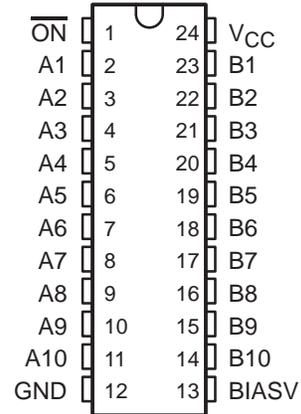
## 10-BIT FET BUS SWITCH

### WITH PRECHARGED OUTPUTS AND SCHOTTKY DIODE CLAMPING

SCDS102A – JUNE 1999 – REVISED JULY 1999

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Schottky Diodes on the I/Os to Clamp Undershoots up to -2 V**
- **Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



#### description

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot.

The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

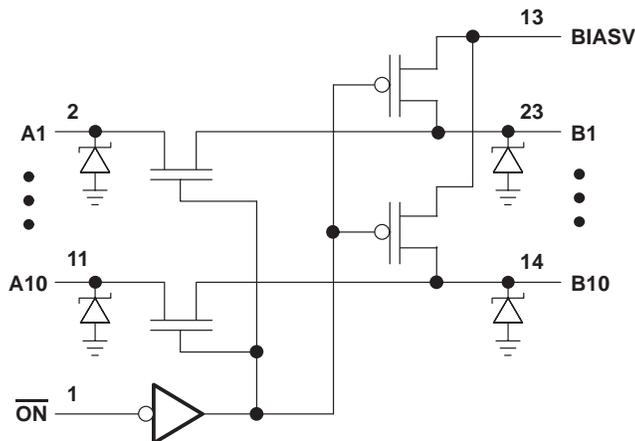
The SN74CBTS6800 is organized as one 10-bit switch with a single enable ( $\overline{\text{ON}}$ ) input. When  $\overline{\text{ON}}$  is low, the switch is on, and port A is connected to port B. When  $\overline{\text{ON}}$  is high, the switch between port A and port B is open. When  $\overline{\text{ON}}$  is high or  $V_{CC}$  is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

The SN74CBTS6800 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

$\overline{\text{ON}}$	B1-B10	FUNCTION
L	A1-A10	Connect
H	BIASV	Precharge

#### logic diagram (positive logic)



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Bias voltage range, $BIASV$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	104°C/W
DBQ package	103°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$BIASV$ Supply voltage	1.3	$V_{CC}$	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$V_{IK}$	A or B inputs	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–0.7	V
	Control inputs					–1.2	
$I_{IL}$		$V_{CC} = 5.5$ V,	$V_I = GND$			–5	$\mu$ A
$I_{IH}$		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V			150	$\mu$ A
$I_O$		$V_{CC} = 4.5$ V,	$BIASV = 2.4$ V, $V_O = 0$	0.25			mA
$I_{CC}$		$V_{CC} = 5.5$ V,	$I_O = 0$ , $V_I = V_{CC}$ or GND			3	$\mu$ A
$\Delta I_{CC}^{\S}$	Control inputs	$V_{CC} = 5.5$ V,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs	$V_I = 3$ V or 0			3.5		pF
$C_{i(OFF)}$		$V_O = 3$ V or 0, $\overline{ON} = V_{CC}$			4.5		pF
$r_{on}^{\parallel}$	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,	$I_I = 15$ mA		11	20	$\Omega$
	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA	3	7		
			$I_I = 30$ mA	3	7		
		$V_I = 2.4$ V,	$I_I = 15$ mA		6	15	

‡ All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

∥ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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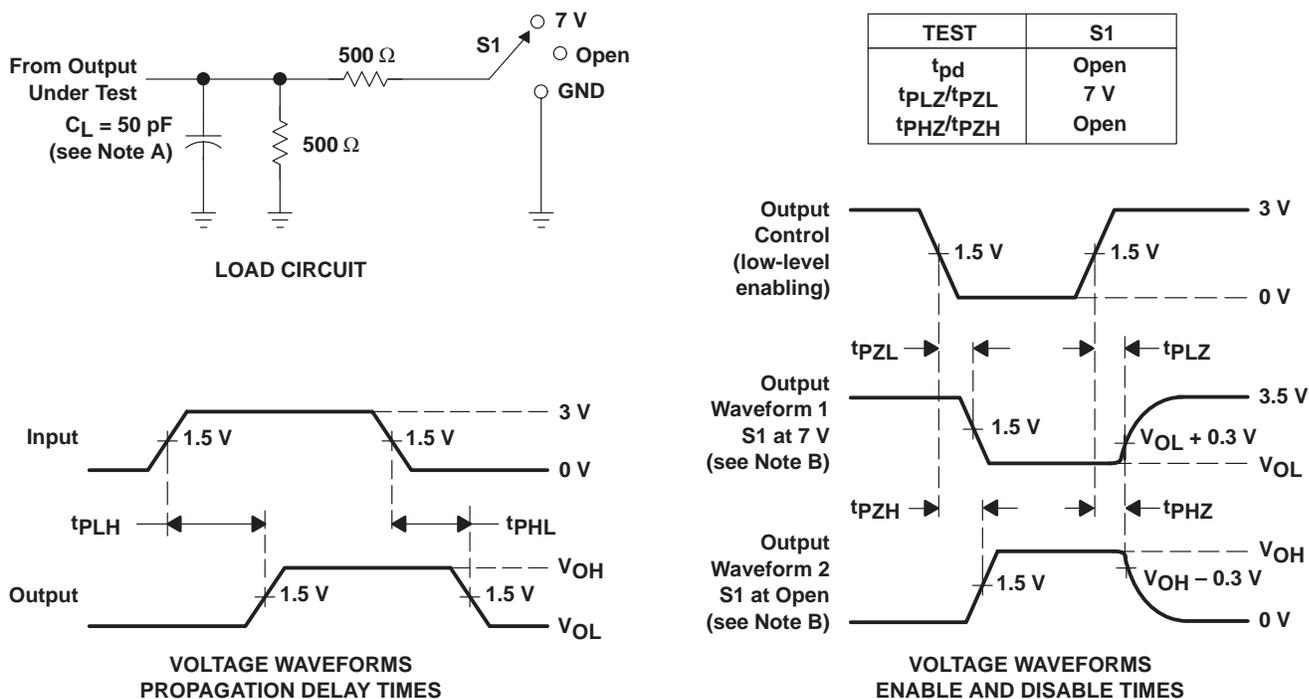
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}^\dagger$		A or B	B or A	0.35		0.25		ns
$t_{PZH}$	BIASV = GND	$\overline{\text{ON}}$	A or B	6		2	5.1	ns
$t_{PZL}$	BIASV = 3 V			6		2	5.6	
$t_{PHZ}$	BIASV = GND	$\overline{\text{ON}}$	A or B	5.5		1	5	ns
$t_{PLZ}$	BIASV = 3 V			5.5		2	5.9	

$^\dagger$  The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50$   $\Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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