

■ Features

- ### ■ Block Diagram



■ Terminal Description

Table 1

Pin No.	Name	Description
78	V _{SS}	Negative power supply
87	V _{DD}	Positive power supply
90 to 95	V ₅ to V ₁	LCD drive power supply. Apply correct voltage to each terminal according to this order : V _{DD} ≥ V ₁ ≥ V ₂ ≥ V ₃ ≥ V ₄ ≥ V ₅
73	A ₀	Display data/display command switching input. Normally connect the last bit of MPU address bus. A ₀ = "0": D ₀ to D ₇ are command inputs and status outputs. A ₀ = "1": D ₀ to D ₇ are display data inputs/outputs.
74	OSC ₁	CR oscillation circuit input. Connect R _f in master operation. NC in slave operation. [Note] • In 80 family, RDX and WRX are each OR'ed with CSX. • In 68 family, E is ANDed with the invert of CSX.
75	OSC ₂	CR oscillation circuit output or display clock input. Master operation: CR oscillation circuit output. Connect R _f . Slave operation: Display clock input. Connect OSC ₂ of the master IC.
76	E	Enable clock signal input (68 family MPU). Active "H".
	RDX	Read signal input (80 family MPU). Active "L". RDX "L" puts the data bus in output status.
77	R/WX	Read/write signal input (68 family MPU). R/WX = "H": Read R/WX = "L": Write
	WRX	Write signal input (80 family MPU). Active "L".
79 to 86	D ₀ to D ₇	3-state input/output. 8-bit bidirectional data bus connection pins.
88	RESX	Interface mode selection and reset. The S-4520BA is reset at the rising and falling edge of RESX signal. Interface mode is selected by RESX level after the S-4520BA is reset. RESX = "H" : 68 family interface RESX = "L" : 80 family interface
89	FR	Alternating signal input/output. M/S = "H": FR signal output M/S = "L": FR signal input
93	M/S	Mode selection. M/S = "H": Master mode M/S = "L": Slave mode
12 to 72	SEG ₆₀ to SEG ₀	Segment drive output.
96 to 100 1 to 11	COM ₀ to COM ₁₅	Common drive output (master mode). Outputs from COM ₀ to COM ₁₅ . Scans from pin No.96→100→1→11.
	COM ₃₁ to COM ₁₆	Common drive output (slave mode). Outputs from COM ₁₆ to COM ₃₁ . Scans from pin No.11→1→100→96.

■ Operating Frequency

Table 2

Operating frequency		Segment driver	Common driver	Note
Internal osc.	External clock			
18 kHz	18 kHz	61	16	External clock is used only in slave mode

Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS}	- 8.0 to + 0.4	V
LCD drive voltage 1	V_5	- 14.5 to + 0.4	V
LCD drive voltage 2	V_1, V_2, V_3, V_4	V_5 to + 0.4	V
Input voltage	V_{IN}	$V_{SS} - 0.4$ to + 0.4	V
Output voltage	V_{OUT}	$V_{SS} - 0.4$ to + 0.4	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	- 30 to + 85	°C
Storage temperature	T_{stg}	- 65 to + 150	°C

Note Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Table 4

(Unless otherwise specified : $V_{DD} = 0$ V, $V_{SS} = -5.0 \pm 0.5$ V, $T_a = -20$ to 75°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating voltage	V_{SS}		- 7.0	-	- 2.4	V	Note 1, 2
Recommended operating voltage	V_{SS}		- 5.5	- 5.0	- 4.5	V	Note 14
LCD drive voltage	V_5		- 13.0	-	- 3.5	V	Note 1, 2
	V_1, V_2		$0.6 \times V_5$	-	V_{DD}	V	
	V_3, V_4		V_5	-	$0.4 \times V_5$	V	
High level input voltage	V_{IHT}		$V_{SS} + 2.0$	-	V_{DD}	V	Note 3, 13
	V_{IHC}		$0.2 \times V_{SS}$	-	V_{DD}	V	Note 4, 13
Low level input voltage	V_{ILT}		V_{SS}	-	$V_{SS} + 0.8$	V	Note 3, 13
	V_{ILC}		V_{SS}	-	$0.8 \times V_{SS}$	V	Note 4, 13
High level output voltage	V_{OHT}	$I_{OH} = -3.0$ mA	$V_{SS} + 2.4$	-	-	V	Note 5
	V_{OHC1}	$I_{OH} = -2.0$ mA	$V_{SS} + 2.4$	-	-	V	FR
	V_{OHC2}	$I_{OH} = -120$ μ A	$0.2 \times V_{SS}$	-	-	V	OSC ₂
Low level output voltage	V_{OLT}	$I_{OL} = 3.0$ mA	-	-	$V_{SS} + 0.4$	V	Note 5
	V_{OLC1}	$I_{OL} = 2.0$ mA	-	-	$V_{SS} + 0.4$	V	FR
	V_{OLC2}	$I_{OL} = 120$ μ A	-	-	$0.8 \times V_{SS}$	V	OSC ₂
Input leakage current	I_{IL}		- 1.0	-	1.0	μ A	Note 6
Output leakage current	I_{OL}		- 3.0	-	3.0	μ A	Note 7
LCD driver ON resistance	R_{ON}	$T_a = 25^\circ\text{C}$	$V_5 = -5.0$ V	-	5.0	k Ω	SEG ₀ to SEG ₆₁ COM ₀ to COM ₁₅ Note 8
			$V_5 = -3.5$ V	-	10.0	k Ω	
Standby current	I_S		-	0.05	1.0	μ A	Note 9
Current consumption	I_{DD1}	During display, $V_5 = -5.0$ V	$R_f = 1$ M Ω	-	9.5	μ A	Note 10
	I_{DD2}	During access, $t_{CYC} = 200$ kHz		-	300	μ A	Note 11
Oscillating frequency	f_{OSC}	$R_f = 1.0$ M Ω , $V_{SS} = -5.0$ V	15	18	21	kHz	
		$R_f = 1.0$ M Ω , $V_{SS} = -3.0$ V	11	16	21	kHz	
Reset time	t_R		-	-	1000	μ s	Note 12

Note 1 Make sure V_{DD} , V_1, V_2, V_3, V_4 , and V_5 have the relationship: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.

Note 2 Drastic fluctuation by power supply voltage, input signal voltage noise, etc. causes malfunction and normal operation can not be guaranteed. In any case, avoid intentionally changing the power supply voltage during operation.

Note 3 TTL input pins: A₀, D₀ to D₇, E(RDX), R/WX(WRX).

Note 4 CMOS input pins: FR, M/S, RESX.

Note 5 D₀ to D₇

Note 6 Input pins: A₀, E(RDX), R/WX(WRX), OSC₁, OSC₂(slave mode), M/S, RESX.

Note 7 Input and output pins at high impedance: FR, D₀ to D₇.

Note 8 This is the resistance when applying 0.1 V between the LCD drive output pins (SEG₀ to SEG₆₀, COM₀ to COM₁₅) and the LCD drive power pins (V_1, V_2, V_3 , and V_4 pins). R_{ON} is measured between the LCD drive power pins and the LCD drive output pins whose electric potential is the same as that of the LCD drive power pins.

DOT MATRIX LCD DRIVER

S-4520BA

Note 9 Current consumption when circuits, for example the oscillation circuit, the MPU interface, etc, are not operating.

Note 10 Current consumption by LCD panel and parasitic capacitance is not included.

Note 11 Current consumption when writing vertically-striped display data at $t_{CYC} = 200$ kHz. After the termination of command, the current consumption value is I_{DD1} .

Note 12 Reset time is from the point where RESX changed to the time when the reset operation is over and normal operation becomes available.

Note 13 This is the inversion level of the input signal. Make the input signal go through the entire power supply voltage range applied for the S-4520BA. If the input signal does not go the full range, current consumption will increase.

Note 14 When using a power supply voltage other than -5.0 ± 0.5 V, the value is different. Check the power supply voltage.

AC Electrical Characteristics

1. Read/write with 80 family MPU

- $V_{SS} = -5$ V

Table 5

($T_a = -20$ to 75°C , $V_{SS} = -5 \text{ V} \pm 10\%$)

Parameter	Sym.	Signal	Conditions	Min.	Max.	Unit
Address hold time	t_{AH8}	A_0		10	—	ns
Address setup time	t_{AW8}			20	—	ns
System cycle time	t_{CYC8}	WRX, RDX		1000	—	ns
Control pulse width	t_{CC}			200	—	ns
Data setup time	t_{DS8}	D_0 to D_7		100	—	ns
Data hold time	t_{DH8}			10	—	ns
RDX access time	t_{ACC8}		CL = 100pF	—	110	ns
Output disable time	t_{OH8}		CL = 100pF	50	130	ns

- $V_{SS} = -3$ V

Table 6

($T_a = -20$ to 75°C , $V_{SS} = -3 \text{ V} \pm 10\%$)

Parameter	Sym.	Signal	Conditions	Min.	Max.	Unit
Address hold time	t_{AH8}	A_0		20	—	ns
Address setup time	t_{AW8}			40	—	ns
System cycle time	t_{CYC8}	WRX, RDX		2000	—	ns
Control pulse width	t_{CC}			400	—	ns
Data setup time	t_{DS8}	D_0 to D_7		200	—	ns
Data hold time	t_{DH8}			20	—	ns
RDX access time	t_{ACC8}		CL = 100pF	—	220	ns
Output disable time	t_{OH8}		CL = 100pF	25	260	ns

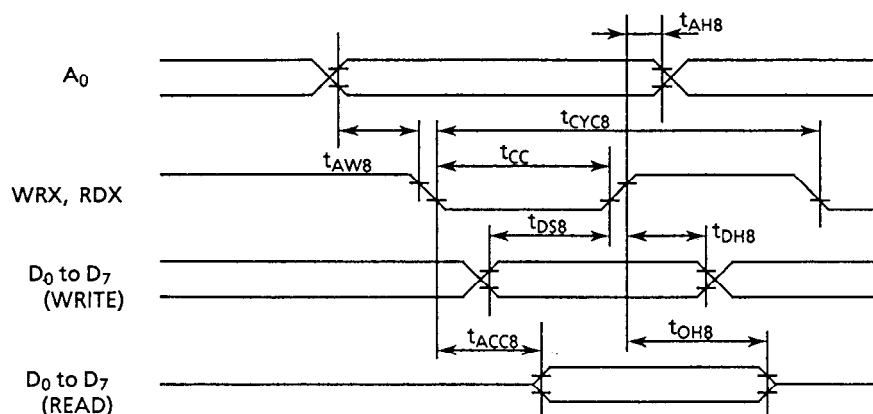


Figure 2 Read/write timing with 80 family MPU

2. Read/write with 68 family MPU

- $V_{SS} = -5\text{ V}$

Table 7

($T_a = -20$ to 75°C , $V_{SS} = -5\text{ V} \pm 10\%$)

Parameter	Sym.	Signal	Conditions	Min.	Max.	Unit
System cycle time	t_{CYC6}	A ₀ RWX		1000	—	ns
Address hold time	t_{AH6}			10	—	ns
Address setup time	t_{AW6}			60	—	ns
Data setup time	t_{DS6}	D ₀ to D ₇		100	—	ns
Data hold time	t_{DH6}			10	—	ns
Access time	t_{ACC6}		CL = 100pF	—	110	ns
Output disable time	t_{OH6}		CL = 100pF	50	130	ns
Enable pulse width	t_{EW}	E	READ	120	—	ns
			WRITE	120	—	ns

- $V_{SS} = -3\text{ V}$

Table 8

($T_a = -20$ to 75°C , $V_{SS} = -3\text{ V} \pm 10\%$)

Parameter	Sym.	Signal	Conditions	Min.	Max.	Unit
System cycle time	t_{CYC6}	A ₀ RWX		2000	—	ns
Address hold time	t_{AH6}			20	—	ns
Address setup time	t_{AW6}			120	—	ns
Data setup time	t_{DS6}	D ₀ to D ₇		220	—	ns
Data hold time	t_{DH6}			20	—	ns
Access time	t_{ACC6}		CL = 100pF	—	220	ns
Output disable time	t_{OH6}		CL = 100pF	25	260	ns
Enable pulse width	t_{EW}	E	READ	240	—	ns
			WRITE	240	—	ns

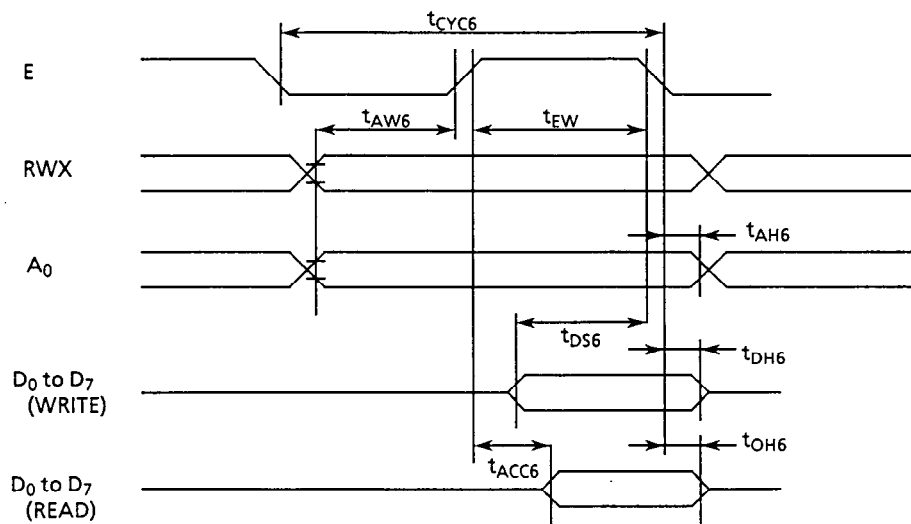


Figure 3 Read/write timing with 68 family MPU

■ Operation

1. Power-on

After power-on, initialization is executed by either the rising or the falling edge of the RESX input. MPU interface mode is selected by the level after RESX signal changes.

When initialization by RESX and the selection of an interface are not executed at power-on, a malfunction may occur. Since chattering in RESX causes poor initialization and erroneous selection of MPU interface, input the signal without chattering. For details, refer to Reset and MPU Interface Selection in this section.

2. Reset

The S-4520BA can be initialized through RESX input or Reset command.

The initialization items through RESX input are listed in Table 9. Initialization through RESX input is executed at the signal change point, either rising or falling. At that time, it is possible to select the MPU Interface. When executing RESX input during operation at power-on, it is necessary to set the signal polarity to fixed MPU.

Initialization through Reset command executes ②, ④, and ⑤ in Table 9. Be aware of the difference in initialization items between reset through RESX input and initialization through Reset command.

Table 9 Initialization at power-on

	Item	Status
①	Display	OFF
②	Display Start Line Set	1st
③	Display all-lit	OFF
④	Column Address Counter	0
⑤	Page Address Register	3
⑥	Duty Select	1/32
⑦	ADC Select	Forward
⑧	Read Modify Write	OFF

3. MPU interface selection

The selection of the S-4520B Series interface is determined by RESX signal logic after RESX signal input.

It is possible to connect directly to either the 68 family or the 80 family MPU.

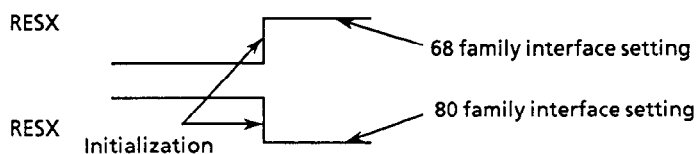


Table 10

Interface	Pin			
	73	76	77	79~86
68 family	A ₀	E	R/WX	D ₀ ~D ₇
80 family	A ₀	RDX	WRX	D ₀ ~D ₇

4. Status

The internal operation status of S-4520BA is monitored for four kinds of status. The status is output in D₄ through D₇. For the monitoring method and function, refer to the Command functions section.

Table 11

Item	Output pin	Status
Busy flag	D ₇	"1": Command operation, Reset operation "0": Command ready
ADC select	D ₆	"1": Forward "0": Reverse
Display ON/OFF	D ₅	"1": Display all-lit "0": Normal display status
Reset	D ₄	"1": Resetting "0": Normal operation status

5. Busy flag

During internal operation, for example command operation, the busy flag is "1", and commands other than Status Read are not received. The Busy flag is output in D₇ through the Status Read command. When accessing the S-4520BA by the signal which specifies the value of read cycle and write cycle timing, the busy flag "0" is not required to be confirmed.

6. Data bus

Table 12

A ₀	68 family R/WX	80 family		Operation
		RDX	WRX	
1	1	0	1	Read from Display Data RAM
1	0	1	0	Write to Display Data RAM
0	1	0	1	Status Read
0	0	1	0	Command Read to internal register

7. Display Data RAM

The S-4520BA has Display Data RAM (8 bits X 4 pages X 80 columns = 2560 bits). As the memory area for display, 8 bits X 4 pages X 61 columns (segments) = 1952 bits is valid. It is possible to use the not-used area for display as normal SRAM. The Display Data RAM is in dual port RAM and enables access from the MPU through Page address and Column address. To the LCD driver side, the one line's common output is read by Line address. The correspondence between Page address, Column address, and Line address is shown in Figure 6.

Display data reading /writing from/to the MPU interface and display data reading to the LCD display are executed independently; one is executed through command, the other is executed synchronizing with the LCD display clock.

At power-on, the display RAM data is not fixed. After power-on, clear the display RAM or write the display data with display OFF and turn the display ON.

8. Reading and writing of display data

The S-4520BA reads and writes the display data through the internal bus holder. The display data is read to the bus holder from the display data RAM, and in the next read cycle on the data bus. Therefore, a dummy read cycle is needed before the first read cycle. When reading the display data after the address set and the data write cycle, a dummy read is needed. Since the reading of the display data is executed using this bus holder, it is possible to read the data at high speed.

Display data is written to the display data RAM through the bus holder within a write cycle. Therefore, writing the display data does not need a dummy cycle.

9. Column address

The column address of the display data RAM is that for writing and reading of the display data. Setting the column address is executed through a command. When accessing the display data RAM from the MPU, the address is incremented by one.

10. Page address

The display RAM is composed of four pages. When accessing the display data RAM from MPU, the page of the display data RAM is set a command.

11. CR oscillation circuit

The S-4520BA is built-in a CR oscillation circuit. Oscillation frequency is approximately 18 kHz at Rf 1 MΩ.

12. LCD drive circuit

The S-4520BA has a 16 common and a 61 segment driver output. An LCD drive waveform which is a two-frame AC drive method (B) type is generated. Refer to Figure 7, LCD drive waveform.

13. Display timing circuit

The display timing is generated by the clock using a CR oscillation circuit or an external clock, and a frame signal FR.

When configuring an LCD panel with more than two S-4520BA, the S-4520BA on the slave side synchronizes to the falling of FR signal. So, on the slave side of the S-4520, the LCD drive waveform is synchronized only by input of the FR signal on the master side. As shown in Figure 8, the display drive output on the slave side, after the common output COM15 on master side, is executed in COM16 through COM31. The FR signals are that of the duty 50 % of synchronized to the COM output timing.

14. Line address

This is the address for reading the LCD RAM data to the LCD data latch. The line address is incremented synchronizing with the common output. The display start line is set with a command.

15. Display data latch

The display data latch is the circuit for latching one line's display data from the display RAM. The display data is output from this latch to the LCD drive circuit. Since the display ON/OFF and the display all-lit ON/OFF control the display data latch, it has no effect on the display RAM data.

16. Master/Slave selection

Master and slave selection is executed through the master/slave terminal logic. The Master IC and the Slave IC have different terminal functions.

Table 13

Product name		M/S	FR	COM output	OSC ₁	OSC ₂
S-4520BA	Master	V _{DD}	Output	COM ₀ to COM ₁₅	Input	Output
	Slave	V _{SS}	Input	COM ₃₁ to COM ₁₆	NC	Input

Note 1 CR oscillation circuit: In slave operation, OSC₁ is at high impedance. OSC₂ is connected to OSC₂ on the master side as a display clock input terminal.

Note 2 Common output: Master operation is output counterclockwise from terminal No.96 to No.11.
Slave operation is output clockwise from terminal No.11 to No.96.

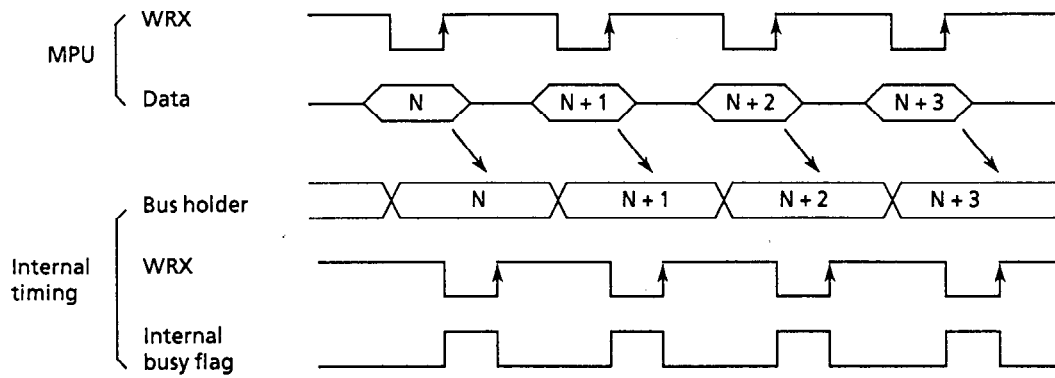


Figure 4 Display data write timing (80 family interface)

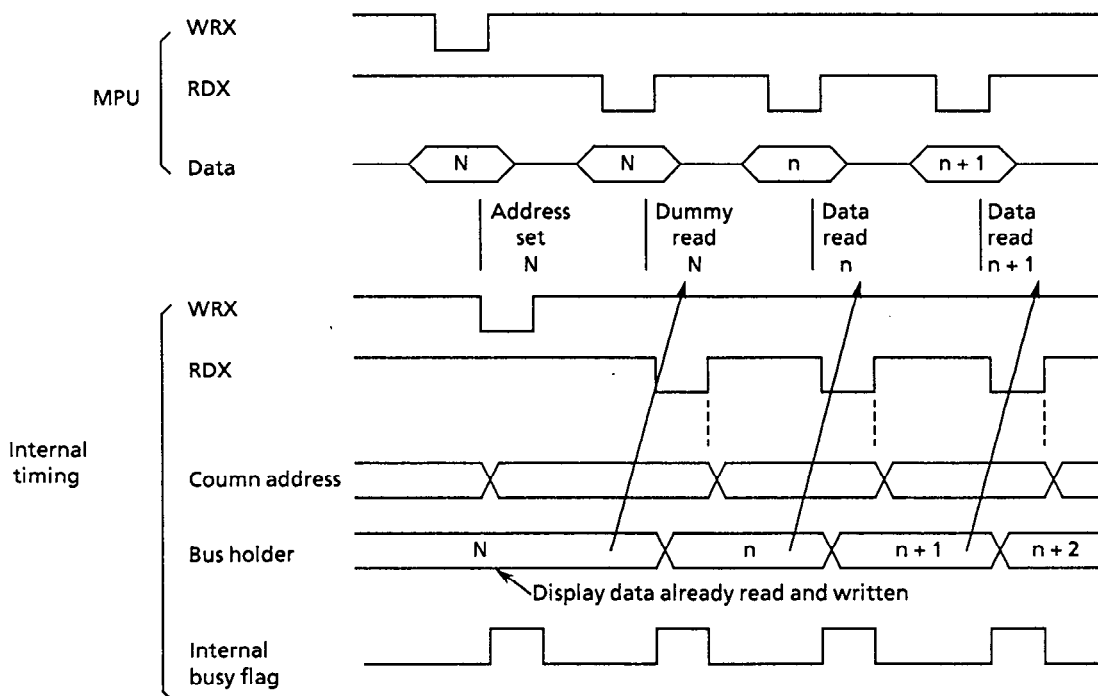
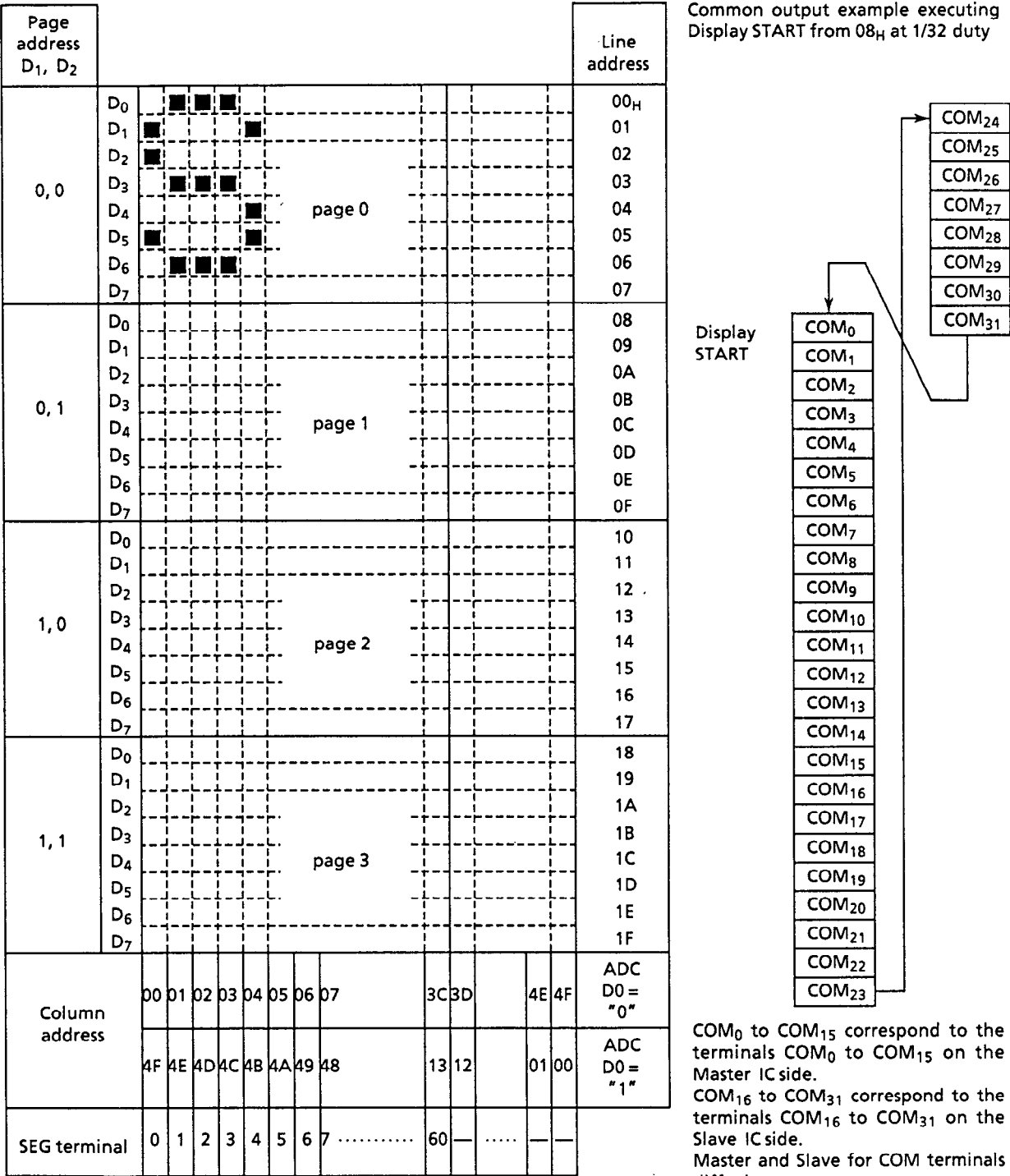


Figure 5 Display data read timing (80 family interface)



Note : For the display data RAM of the S-4520BA, the memory area corresponding to SEG terminal 0 to 60 is valid as display data.
The other area is usable as normal SRAM.

Figure 6 Correspondence between display data and address

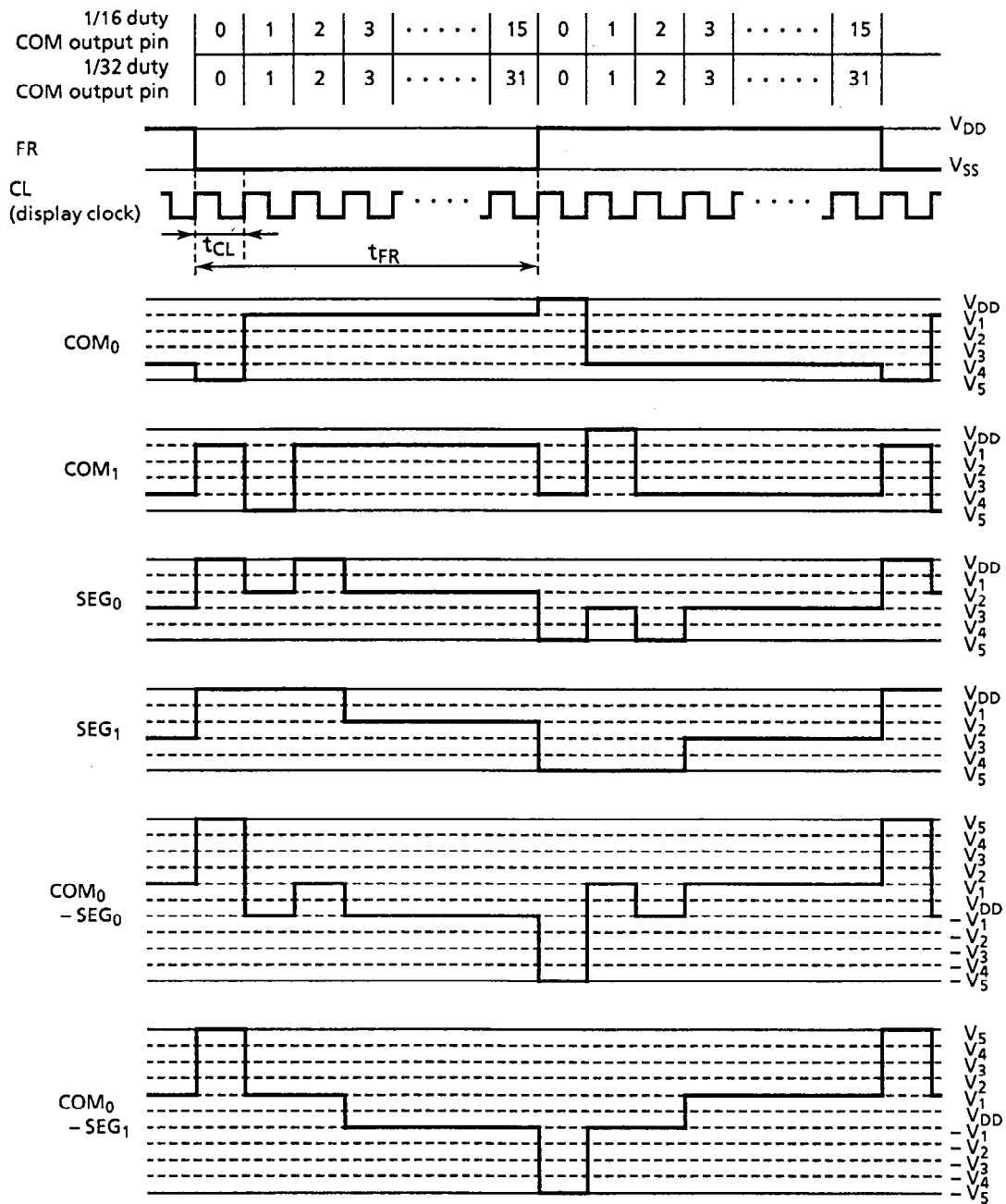
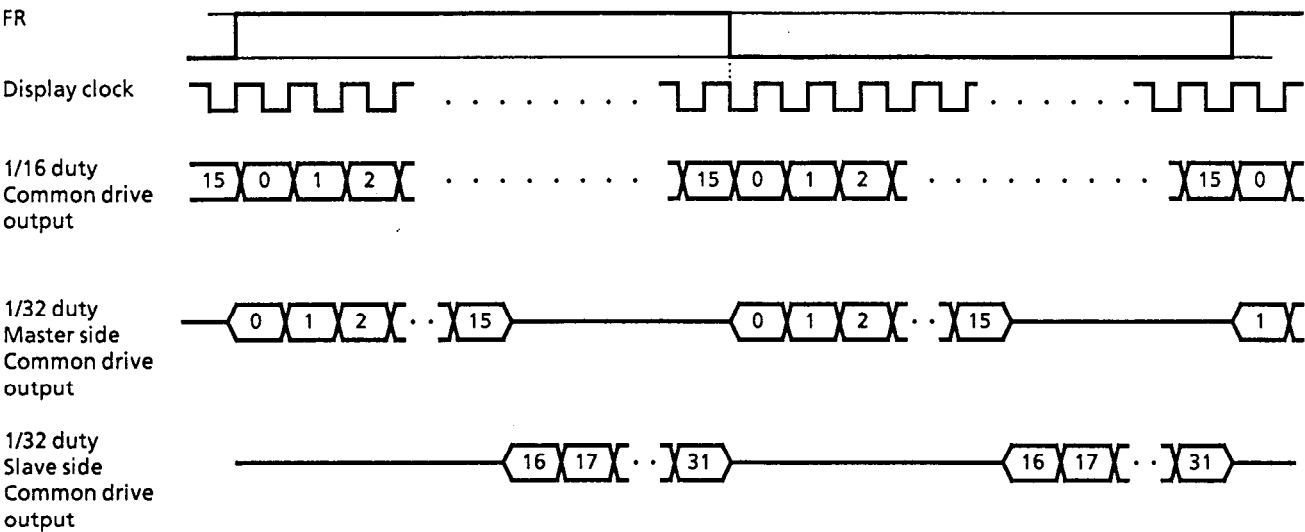


Figure 7 LCD driver waveform example



Note : Common drive output orders on the Master side and the Slave side differ.

	Common drive output order
Master side	Counterclockwise from pad No.96
Slave side	Clockwise from pad No.11

Figure 8 FR and Common drive output waveform

Table 14 Column, frame cycle

Item	Display duty	Cycle
t_{CL} Column cycle	duty 1/16	16/f
	duty 1/32	8/f
t_{FR} Frame cycle	duty 1/16	256/f
	duty 1/32	256/f

f = CR oscillation frequency

■ Command

The S-4520BA can set the command functions with combinations of A₀, R/WX (68 family MPU), RDX and WRX (80 family MPU). The command setting is executed according to the internal timing. If the Display data read timing diagram, the Display data write timing diagram, and the timing characteristic diagram in the operation description are satisfied, it is possible to input through the commands without confirming the busy flag. Therefore, high speed operation and MPU load reduction are attainable. For the command list, refer to Table 17.

1. Display ON/OFF

The logic D₀ controls the display ON/OFF. In display OFF, the screen is compelled to be all-off regardless of the display RAM data. The display RAM data does not change.

In display ON, normal display is on according to the display RAM data. When the display ON command is input, display OFF is canceled.

When setting display all-lit ON in the display OFF status, it changes to Power save mode (see the Power Save command.)

2. Display start line set

The line address of the display data RAM which indicates the display start line is set. The display start line corresponding to COM0, as shown in the figure, indicates the correspondence between the display data RAM and the address. The display area read from the display data RAM corresponds to the number of the lines for the duty set using the Duty select command. The line address is automatically incremented synchronizing with the common output. Changing the display START line using this command enables a smooth scroll on the screen or a page change.

3. Page address set

The page address is set when accessing the display data RAM from the MPU. It is possible to access the display data RAM from the MPU using the page address and the column address. Refer to the figure which shows the correspondence between the display data RAM and the address. Even if the page address is changed, it has no influence, such as changing of the screen during operation.

4. Column address set

The column address is set when accessing the display data RAM from the MPU. When accessing the display data RAM from the MPU, the column address is incremented by one. When accessing the successive column address from the MPU, it is possible to access the display data without setting the column address each time. The automatic increment stops at 80 after accessing the top column address 79. The page address is not incremented.

5. Status read

It is possible to read four kinds of status using this command.

Table 19 Status

Busy	Shows the command ready during the S-4520BA command operation.	
	"1"	Shows that the IC inside is executing a command operation or a reset operation. When the Busy flag is output, the command is not received. If the cycle time of the command is satisfied with the specified value, Busy flag confirmation is not needed.
	"0"	Shows that the command is ready
ADC	Shows forward or reverse correspondence between column address and segment output terminal of the display data RAM The setting is executed using the ADC select command.	
	"1"	Forward The column addresses 0 _H to 3C _H corresponds to the segment output terminals 0 to 60.
	"0"	Reverse The column address 13 _H to 4F _H corresponds to the segment output terminals 60 to 0.
ON/OFF	Shows the display ON/OFF status. Note: it is the reverse to the polarity of Display ON/OFF command.	
	"0"	Shows the display ON status. Display normal operation status
	"1"	Shows the display OFF status. Display all-OFF status.
Reset	Shows that the S-4520BA is executing initialization by RESX input or Reset command.	
	"0"	Normal operation
	"1"	Reset operation

6. Write data

The 8-bit display data is written in the display data RAM. After writing the display data, the column address is automatically incremented. When writing the successive display data after setting the first column address using the column address set command, it is unnecessary to set the column address each time.

7. Read data

The 8-bit display data is read from the display data RAM. After reading the display data, the column address is automatically incremented. When reading the successive display data after setting the first column address using the column address set command, it is unnecessary to set the column address each time. For reading display data just after the column address set, a dummy read is needed.

8. ADC select

Forward or reverse is selectable for the correspondence between the column address and the segment output terminal of the display data RAM. When configuring an LCD panel with more than two ICs, it is possible to reverse the segment output order from the MPU. Since the segment output terminals of an S-4520BA go from 0 to 60, the valid column address for the display data of the reverse select side IC is 13_H to 4F_H. Refer to the correspondence between the display data RAM and the address in Figure 6.

D₀ D : "0" Forward The column addresses 0_H to 3C_H correspond to the segment output terminals 0 to 60.

 D : "1" Reverse The column addresses 13_H to 4F_H correspond to the segment output terminals 60 to 0.

9. Display all-lit ON/OFF

Display all-lit ON makes the display be entirely lit. All common outputs become selectable status. Segment output is compelled to be all-lit output. The display RAM's data, however does not change. Through Display all-lit OFF, the screen returns to normal display operation. When inputting the Display OFF command in the display all-lit ON status, it changes to Power save mode. Refer to the Power save command.

10. Duty select

The duty for the LCD drive output is selected.

11. Read modify write

The read modify write command is valid when partly altering or rewriting the display data RAM, for example the cursor indication, the blinking indication, etc. After inputting the Read modify write command, column address of the display data RAM is incremented only when inputting the display data write command. In Read data command, it is possible to rewrite the display data of the column address which is read, without increment of the column address. Furthermore, when reading and writing of the display data is successively executed, the successive address of the display data RAM is rewritten within the same page. A dummy read is needed when reading the display data.

Read modify write command is valid until the End command is input. When inputting the End command, the column address returns to the address before the Read modify command was input.

During the Read modify write command operation, all commands are usable except the Column address set command.

12. End command

This command cancels Read modify write. The column address of the display data returns to the address before Read modify write was executed.

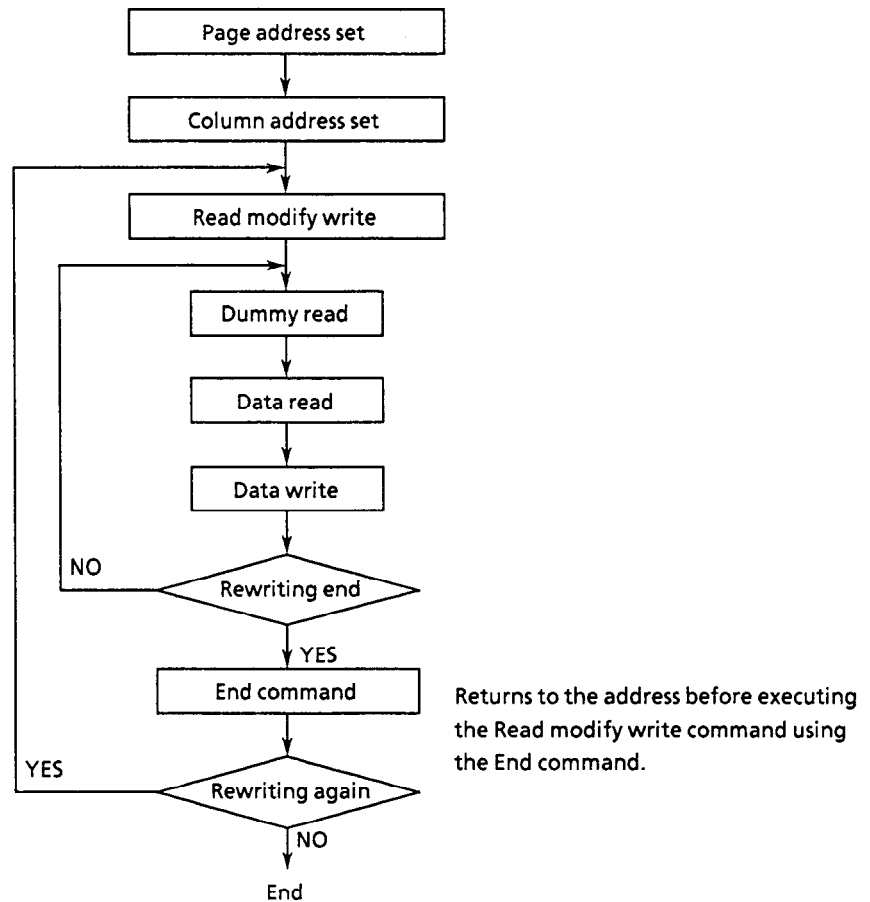


Figure 9 Command sequence for cursor indication

13. Reset command

This command resets the address of the display data RAM as followings.
After resetting, display starts according to the reset value.

- Resets the Display START Line to the 1st line.
- Resets the page address to 3.

Be aware that the functions are limited in comparison with resetting through the reset signal. At power-on, reset through the RESX input. For details, refer to the description of reset operation.

14. Power Save mode

When setting display all-OFF using the Display OFF command and executing the Display all-lit ON command, it changes to the Power save mode. When displaying in all-lit status and executing the Display OFF command, it also changes to the Power save mode. In the Power save mode,

- Current consumption is reduced and a value near that at standstill is attainable.
- The LCD drive circuit is stopped. The Segment and Common outputs are fixed at V_{DD} level.
- Input is prohibited and the OSC_2 terminal floats.
- Content of the display data RAM, the command and the address before the power save mode do not change.

The Power save status is canceled through the Display ON or the Display all-lit commands.

When the LCD driver voltage is generated by division of external resistance, the electric current is passed through this divided resistance regardless of the ICs. When reducing this current, attach a switching transistor which cuts the current flowing to the external resistance.

Table 16 Power save command

Command combination		Status
Dipslay	Display all-lit	
ON	OFF	Normal display operation
ON	ON	All-lit display
OFF	OFF	All-off
OFF	ON	Power save

Table 17 Display commands

Command	Code											Function
	A ₀	RDX	R/WX WRX	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 / 1	Selects normal display or all off on the screen. D ₀ : 1 ON. Normal display operation using the display data RAM. D ₀ : 0 OFF. Display OFF status regardless of the display RAM data. Power Save mode is entered by display OFF and display all-lit ON.
Display START Line	0	1	0	1	1	0	Display START line address (See Table 22)					Sets the line address of the display data RAM to be displayed at the top line of the screen (COM ₀ output). Address setting ranges from 0 to 31.
Page Address Set	0	1	0	1	0	1	1	1	0	Page address (See Table 23)		Sets up the page address of the display data RAM in order to access the display data RAM from the MPU. Address setting ranges from 0 to 3.
Column Address Set	0	1	0	0	Column address (See Table 24)							Sets up the column address of the display data RAM in order to access the display data RAM from the MPU. Address setting ranges from 0 to 79.
Status Read	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Command operation 0: Command ready ADC 1: Column address forward 0: Column address invert Display ON/OFF 1: Display all-off status 0: Normal display status RESET 1: Resetting 0: Normal operation
Write Display Data	1	1	0	Write Data								Writes the data D ₀ through D ₇ on the display data RAM.
Read Display Data	1	0	1	Read Data								Reads the data D ₀ through D ₇ from the display data RAM.
ADC Select	0	1	0	1	0	1	0	0	0	0	0 / 1	Used to invert the column address of the display data RAM, after which the correspondence between the display RAM's addresses and segment output terminals is inverted. D ₀ : 0 Forward SEG0 terminal = column address 0 (00 _H) D ₀ : 1 Invert SEG0 terminal = column address 79 (4F _H)
Display all-lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 / 1	Selects normal display operation or all-lit display operation. D ₀ : 0 Normal display operation D ₀ : 1 All-lit display operation The screen is changed to all-lit status. Power Save mode is entered through display OFF and display all-lit ON.
Duty Select	0	1	0	1	0	1	0	1	0	0	0 / 1	Selects the LCD drive output duty. D ₀ : 0 1/16 duty D ₀ : 1 1/32 duty
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address of display data RAM only when display data is written but not when it is read.
End	0	1	0	1	1	1	0	1	1	1	0	Cancels Read Modify Write mode and increments the column address of the display data RAM when display data is written and read.
Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the address of the display data RAM as follows: • Resets the Display START Line to the 1st line. • Resets the page address to 3.

Table 18 Display START line address

D ₄	D ₃	D ₂	D ₁	D ₀	Line address
A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	0
0	0	0	0	1	1
.
.
1	1	1	1	1	31

Table 19 Page address

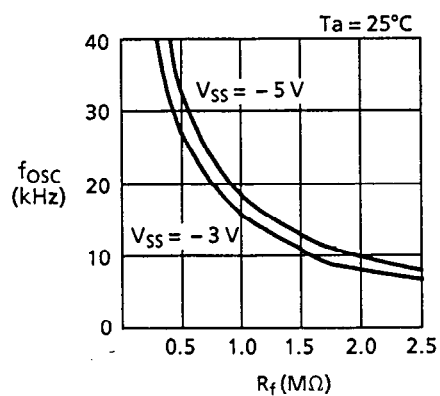
D ₁	D ₀	Page address
A ₁	A ₀	
0	0	0
0	1	1
1	0	2
1	1	3

Table 20 Column address

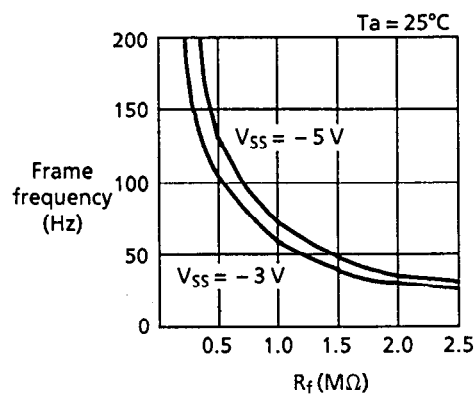
D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Column address
A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
.
.
1	0	0	1	1	1	1	79

Frequency Characteristics

1. Oscillation frequency

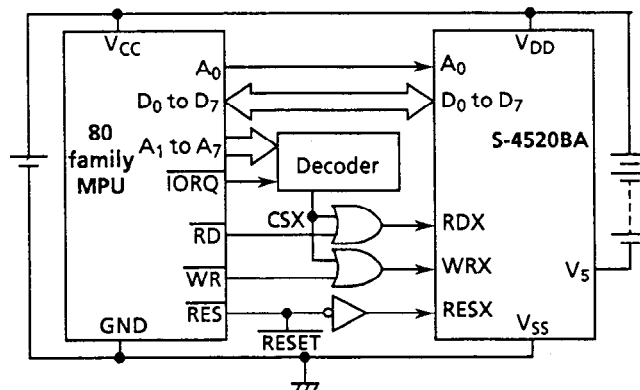


2. Frame frequency



■ Application Circuit Examples

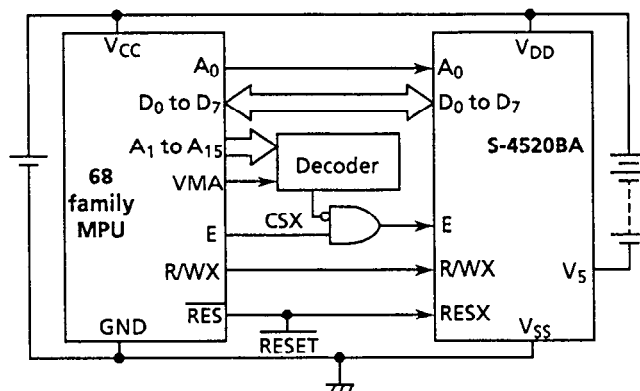
1. 80 family MPU interface



Note: S-4520BA has no CSX terminal. Logic for RDX and WRX must be set outside.

Figure 10

2. 68 family MPU interface



Note: S-4520BA has no CSX terminal. Logic for E must be set outside.

Figure 11

■ Connection Between Two LCD Drivers

1. Connection between two S-4520BAs

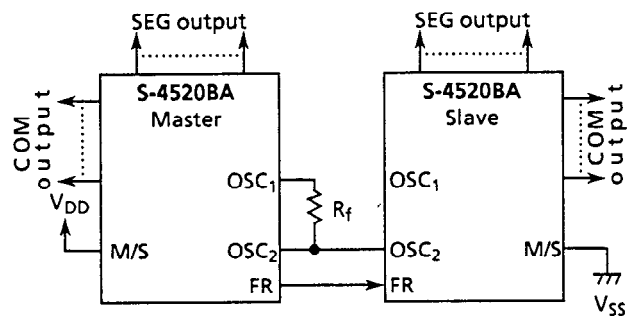


Figure 12

■ LCD Panel Configuration

One character has 5x8 dots.
 One kanji has 16x16 dots.

1. 1/16 duty 12 characters, 2 lines

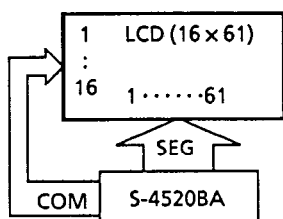


Figure 13

2. 1/16 duty 24 characters, 4 lines

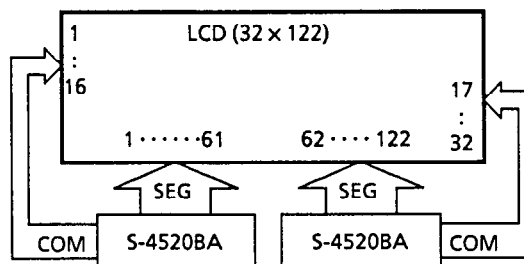
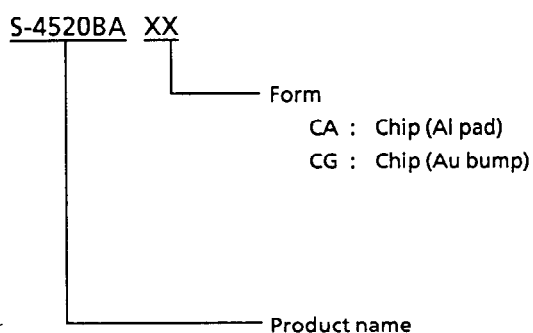
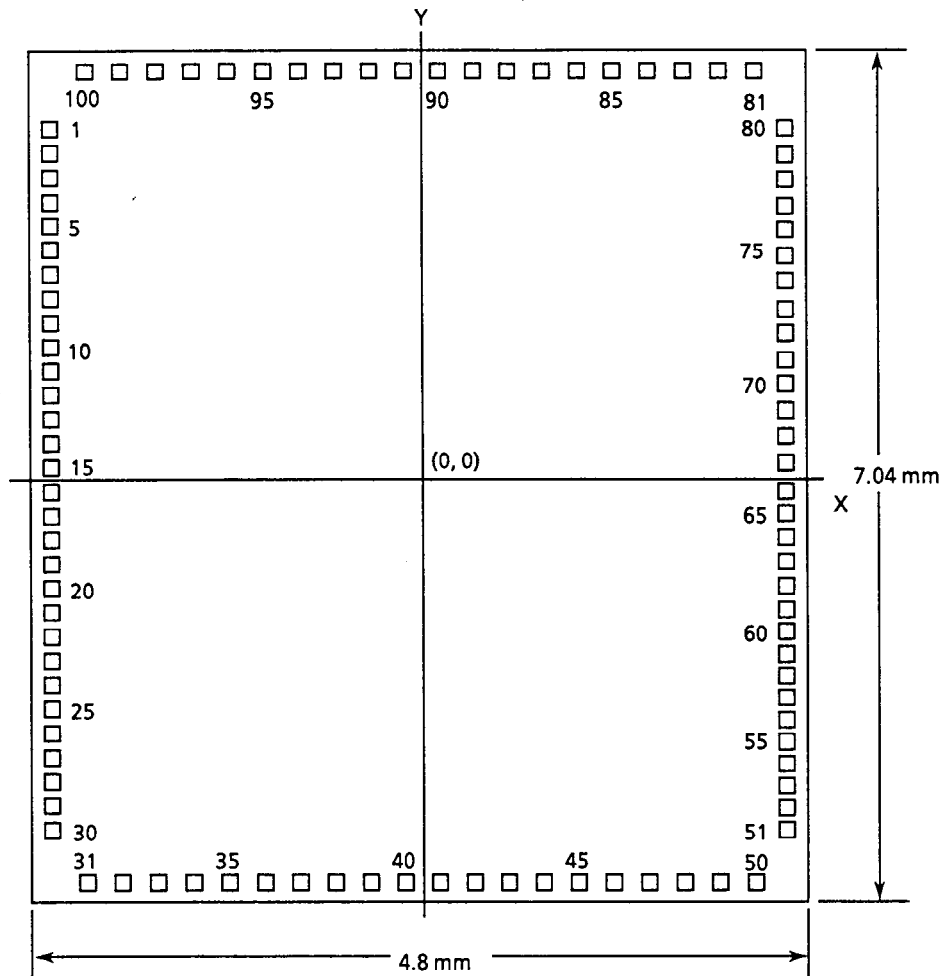


Figure 14

■ Ordering Information



■ Pad Layout



- Al pad :

Chip size	4.8 × 7.04 × 0.4 mm
Min. pad pitch	199 μm
Pad opening	100 × 100 μm
- Au bump :

Chip size	4.8 × 7.04 × 0.525 mm
Min. pad pitch	199 μm
Bump type	Straight
Bump height	22 ± 7 μm
Bump size	116 × 92 μm

Figure 15

Table 21 Pad coordinate

PAD No.	PAD Name	X (μm)	Y (μm)	PAD No.	PAD Name	X (μm)	Y (μm)	PAD No.	PAD Name	X (μm)	Y (μm)
1	COM ₅ (COM ₂₆)	- 2241	2987	30	SEG ₄₂	- 2241	- 3038	70	SEG ₂	2241	827
				31	SEG ₄₁	- 1896	- 3361	71	SEG ₁	2241	1027
2	COM ₆ (COM ₂₅)	- 2241	2788	32	SEG ₄₀	- 1697	- 3361	72	SEG ₀	2241	1269
				33	SEG ₃₉	- 1497	- 3361	73	A ₀	2241	1528
3	COM ₇ (COM ₂₄)	- 2241	2588	34	SEG ₃₈	- 1298	- 3361	74	OSC ₁	2241	1728
				35	SEG ₃₇	- 1098	- 3361	75	OSC ₂	2241	1927
4	COM ₈ (COM ₂₃)	- 2241	2389	36	SEG ₃₆	- 899	- 3361	76	E (RDX)	2241	2127
				37	SEG ₃₅	- 699	- 3361				
5	COM ₉ (COM ₂₂)	- 2241	2199	38	SEG ₃₄	- 500	- 3361	77	R/WX (WRX)	2241	2326
				39	SEG ₃₃	- 300	- 3361				
6	COM ₁₀ (COM ₂₁)	- 2241	1990	40	SEG ₃₂	- 101	- 3361	78	V _{SS}	2241	2587
				41	SEG ₃₁	99	- 3361	79	D ₀	2241	2787
7	COM ₁₁ (COM ₂₀)	- 2241	1790	42	SEG ₃₀	299	- 3361	80	D ₁	2241	2986
				43	SEG ₂₉	498	- 3361	81	D ₂	1895	3364
8	COM ₁₂ (COM ₁₉)	- 2241	1591	44	SEG ₂₈	698	- 3361	82	D ₃	1695	3364
				45	SEG ₂₇	897	- 3361	83	D ₄	1496	3364
9	COM ₁₃ (COM ₁₈)	- 2241	1391	46	SEG ₂₆	1097	- 3361	84	D ₅	1296	3364
				47	SEG ₂₅	1296	- 3361	85	D ₆	1097	3364
10	COM ₁₄ (COM ₁₇)	- 2241	1192	48	SEG ₂₄	1496	- 3361	86	D ₇	897	3364
				49	SEG ₂₃	1695	- 3361	87	V _{DD}	698	3364
11	COM ₁₅ (COM ₁₆)	- 2241	992	50	SEG ₂₂	1895	- 3361	88	RESX	498	3364
				51	SEG ₂₁	2241	- 3038	89	FR	299	3364
12	SEG ₆₀	- 2241	649	52	SEG ₂₀	2241	- 2839	90	V ₅	99	3364
13	SEG ₅₉	- 2241	450	53	SEG ₁₉	2241	- 2639	91	V ₃	- 101	3364
14	SEG ₅₈	- 2241	250	54	SEG ₁₈	2241	- 2440	92	V ₂	- 300	3364
15	SEG ₅₇	- 2241	51	55	SEG ₁₇	2241	- 2240	93	M/S	- 500	3364
16	SEG ₅₆	- 2241	- 149	56	SEG ₁₆	2241	- 2041	94	V ₄	- 699	3364
17	SEG ₅₅	- 2241	- 445	57	SEG ₁₅	2241	- 1841	95	V ₁	- 899	3364
18	SEG ₅₄	- 2241	- 644	58	SEG ₁₄	2241	- 1642		COM ₀		
19	SEG ₅₃	- 2241	- 844	59	SEG ₁₃	2241	- 1442	96	(COM ₃₁)	- 1098	3364
20	SEG ₅₂	- 2241	- 1043	60	SEG ₁₂	2241	- 1243		COM ₁		
21	SEG ₅₁	- 2241	- 1243	61	SEG ₁₁	2241	- 1043	97	(COM ₃₀)	- 1298	3364
22	SEG ₅₀	- 2241	- 1442	62	SEG ₁₀	2241	- 844		COM ₂		
23	SEG ₄₉	- 2241	- 1642	63	SEG ₉	2241	- 644	98	(COM ₂₉)	- 1497	3364
24	SEG ₄₈	- 2241	- 1841	64	SEG ₈	2241	- 445		COM ₃		
25	SEG ₄₇	- 2241	- 2041	65	SEG ₇	2241	- 245	99	(COM ₂₈)	- 1697	3364
26	SEG ₄₆	- 2241	- 2240	66	SEG ₆	2241	- 46		COM ₄		
27	SEG ₄₅	- 2241	- 2440	67	SEG ₅	2241	154	100	(COM ₂₇)	- 1896	3364
28	SEG ₄₄	- 2241	- 2639	68	SEG ₄	2241	428				
29	SEG ₄₃	- 2241	- 2839	69	SEG ₃	2241	628				

- The terminals for which the name differs between Master and Slave

Mode	74	75	96 to 100, 1 to 11	Note
Master Mode	OSC ₁	OSC ₂	COM ₀ to COM ₁₅	M/S = "H"
Slave Mode	NC	OSC ₂ *1	COM ₃₁ to COM ₁₆	M/S = "L"

*1 : Connect to OSC₂ of the master IC.