



## 10-/8-Bit, 1.25-MSPS, MICRO-POWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTERS

### FEATURES

- 1.25-MHz Sample Rate Serial Device
- 10-Bit Resolution – ADS7887
- 8-Bit Resolution – ADS7888
- Zero Latency
- 25-MHz Serial Interface
- Supply Range: 2.35 V to 5.25 V
- Typical Power Dissipation at 1.25 MSPS:
  - 3.8 mW at 3-V  $V_{DD}$
  - 8 mW at 5-V  $V_{DD}$
- $\pm 0.35$  LSB INL, DNL – ADS7887
- $\pm 0.15$  LSB INL,  $\pm 0.1$  LSB DNL – ADS7888
- 61dB SINAD, -84 dB THD – ADS7887
- 49.5 dB SINAD, -67.5 dB THD – ADS7888
- Unipolar Input Range: 0 V to  $V_{DD}$
- Power Down Current: 1  $\mu$ A
- Wide Input Bandwidth: 15 MHz at 3 dB
- 6-Pin SOT23 and SC70 Packages

### APPLICATIONS

- Base Band Converters in Radio Communication
- Motor Current/Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- Battery Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

### DESCRIPTION

The ADS7887 is a 10-bit, 1.25-MSPS analog-to-digital converter (ADC), and the ADS7888 is a 8-bit, 1.25-MSPS ADC. The devices include a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the  $\overline{CS}$  and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of  $\overline{CS}$ , and SCLK is used for conversion and serial data output.

The devices operate from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the devices make them suitable for battery-powered applications. The devices also include a power saving powerdown feature for when the devices are operated at lower conversion speeds.

The high level of the digital input to the device is not limited to device  $V_{DD}$ . This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power up sequencing.

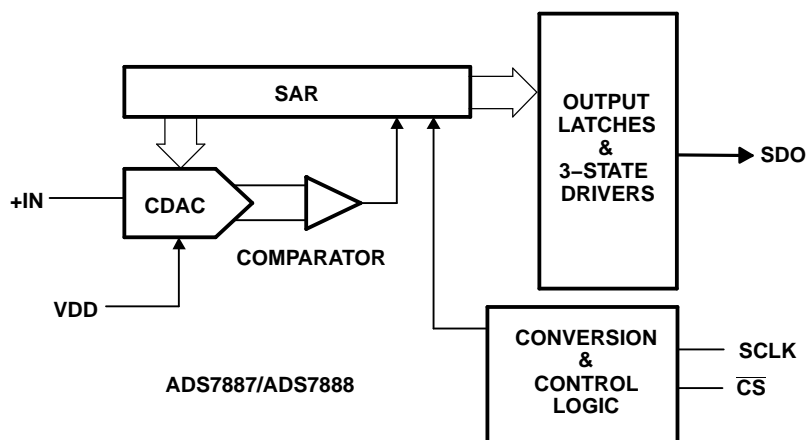
The ADS7887 and ADS7888 are available in 6-pin SOT23 and SC70 packages and are specified for operation from -40°C to 125°C.

#### Micro-Power Miniature SAR Converter Family

| BIT    | < 300 KSPS                              | 300 KSPS – 1.25 MSPS                      |
|--------|---|---|
| 12-Bit | ADS7866 (1.2 $V_{DD}$ to 3.6 $V_{DD}$ ) | ADS7886 (2.35 $V_{DD}$ to 5.25 $V_{DD}$ ) |
| 10-Bit | ADS7867 (1.2 $V_{DD}$ to 3.6 $V_{DD}$ ) | ADS7887 (2.35 $V_{DD}$ to 5.25 $V_{DD}$ ) |
| 8-Bit  | ADS7868 (1.2 $V_{DD}$ to 3.6 $V_{DD}$ ) | ADS7888 (2.35 $V_{DD}$ to 5.25 $V_{DD}$ ) |



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

| DEVICE  | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES AT RESOLUTION (BIT) | PACK-AGE TYPE | PACK-AGE DESIGNATOR | TEMPERATURE RANGE | PACKAGE MARKING | ORDERING INFORMATION | TRANSPORT MEDIA QUANTITY |
|---------|----------------------------------|--------------------------------------|--------------------------------------|---------------|---------------------|-------------------|-----------------|----------------------|--------------------------|
| ADS7887 | ±0.75                            | ±0.5                                 | 10                                   | 6-Pin SOT23   | DBV                 | −40°C to 125°C    | BAWQ            | ADS7887SDBVT         | Tape and reel 250        |
|         |                                  |                                      |                                      |               |                     |                   | BAWQ            | ADS7887SDBVR         | Tape and reel 3000       |
|         |                                  |                                      |                                      | 6-Pin SC70    | DCK                 |                   | BNI             | ADS7887SDCKT         | Tape and reel 250        |
|         |                                  |                                      |                                      |               |                     |                   | BNI             | ADS7887SDCKR         | Tape and reel 3000       |
| ADS7888 | ±0.3                             | ±0.3                                 | 8                                    | 6-Pin SOT23   | DBV                 | −40°C to 125°C    | BAZQ            | ADS7888SDBVT         | Tape and reel 250        |
|         |                                  |                                      |                                      |               |                     |                   | BAZQ            | ADS7888SDBVR         | Tape and reel 3000       |
|         |                                  |                                      |                                      | 6-Pin SC70    | DCK                 |                   | BNH             | ADS7888SDCKT         | Tape and reel 250        |
|         |                                  |                                      |                                      |               |                     |                   | BNH             | ADS7888SDCKR         | Tape and reel 3000       |

(1) For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|  |                      | UNIT   |
|--|----------------------|--|
| +IN to AGND                                |                      | –0.3 V to +V <sub>DD</sub> +0.3 V                    |
| +V <sub>DD</sub> to AGND                   |                      | –0.3 V to 7.0 V                                      |
| Digital input voltage to GND               |                      | –0.3V to (7.0 V)                                     |
| Digital output to GND                      |                      | –0.3 V to (+V <sub>DD</sub> + 0.3 V)                 |
| Operating temperature range                |                      | –40°C to 125°C                                       |
| Storage temperature range                  |                      | –65°C to 150°C                                       |
| Junction temperature (T <sub>J</sub> Max)  |                      | 150°C  |
| Power dissipation, SOT23 and SC70 packages |                      | (T <sub>J</sub> Max–T <sub>A</sub> )/θ <sub>JA</sub> |
| θ <sub>JA</sub> Thermal impedance          | SOT23                | 295.2°C/W  |
|  | SC70                 | 351.3°C/W  |
| Lead temperature, soldering                | Vapor phase (60 sec) | 215°C  |
|  | Infrared (15 sec)    | 220°C  |

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ADS7887 SPECIFICATIONS

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = –40°C to 125°C, f<sub>sample</sub> = 1.25 MHz

| PARAMETER                        |  | TEST CONDITIONS  | MIN                  | TYP   | MAX                   | UNIT               |
|----------------------------------|--|--|----------------------|-------|-----------------------|--------------------|
| <b>ANALOG INPUT</b>              |  |  |                      |       |                       |                    |
|                                  | Full-scale input voltage span <sup>(1)</sup> |  | 0                    |       | V <sub>DD</sub>       | V                  |
|                                  | Absolute input voltage range                 | +IN  | –0.20                |       | V <sub>DD</sub> +0.20 | V                  |
| C <sub>i</sub>                   | Input capacitance <sup>(2)</sup>             |  |                      | 21    |                       | pF                 |
| I <sub>ilk</sub>                 | Input leakage current                        | T <sub>A</sub> = 125°C                                     |                      | 40    |                       | nA                 |
| <b>SYSTEM PERFORMANCE</b>        |  |  |                      |       |                       |                    |
|                                  | Resolution                                   |  |                      | 10    |                       | Bits               |
|                                  | No missing codes                             |  | 10                   |       |                       | Bits               |
| INL                              | Integral nonlinearity                        |  | –0.75                | ±0.35 | 0.75                  | LSB <sup>(3)</sup> |
| DNL                              | Differential nonlinearity                    |  | –0.5                 | ±0.35 | 0.5                   | LSB                |
| E <sub>O</sub>                   | Offset error <sup>(4)</sup> (5)(6)           |  | –1.5                 | ±0.5  | 1.5                   | LSB                |
| E <sub>G</sub>                   | Gain error <sup>(5)</sup>                    |  | –1                   | ±0.5  | 1                     | LSB                |
| <b>SAMPLING DYNAMICS</b>         |  |  |                      |       |                       |                    |
|                                  | Conversion time                              | 25-MHz SCLK  | 530                  | 560   |                       | ns                 |
|                                  | Acquisition time                             |  | 260                  |       |                       | ns                 |
|                                  | Maximum throughput rate                      | 25-MHz SCLK  |                      |       | 1.25                  | MHz                |
|                                  | Aperture delay                               |  |                      | 5     |                       | ns                 |
|                                  | Step Response                                |  |                      | 160   |                       | ns                 |
|                                  | Overvoltage recovery                         |  |                      | 160   |                       | ns                 |
| <b>DYNAMIC CHARACTERISTICS</b>   |  |  |                      |       |                       |                    |
| THD                              | Total harmonic distortion <sup>(7)</sup>     | 100 kHz  |                      | –84   | –72                   | dB                 |
| SINAD                            | Signal-to-noise and distortion               | 100 kHz  | 60.5                 | 61    |                       | dB                 |
| SFDR                             | Spurious free dynamic range                  | 100 kHz  | 73                   | 81    |                       | dB                 |
|                                  | Full power bandwidth                         | At –3 dB   |                      | 15    |                       | MHz                |
| <b>DIGITAL INPUT/OUTPUT</b>      |  |  |                      |       |                       |                    |
| Logic family — CMOS              |  |  |                      |       |                       |                    |
| V <sub>IH</sub>                  | High-level input voltage                     | V <sub>DD</sub> = 2.35 V to 5.25 V                         | V <sub>DD</sub> –0.4 |       | 5.25                  | V                  |
| V <sub>IL</sub>                  | Low-level input voltage                      | V <sub>DD</sub> = 5 V                                      |                      |       | 0.8                   | V                  |
|                                  |  | V <sub>DD</sub> = 3 V                                      |                      |       | 0.4                   | V                  |
| V <sub>OH</sub>                  | High-level output voltage                    | At I <sub>source</sub> = 200 µA                            | V <sub>DD</sub> –0.2 |       |                       | V                  |
| V <sub>OL</sub>                  | Low-level output voltage                     | At I <sub>sink</sub> = 200 µA                              |                      |       | 0.4                   | V                  |
| <b>POWER SUPPLY REQUIREMENTS</b> |  |  |                      |       |                       |                    |
| +V <sub>DD</sub>                 | Supply voltage                               |  | 2.35                 | 3.3   | 5.25                  | V                  |
|                                  | Supply current (normal mode)                 | At V <sub>DD</sub> = 2.35 V to 5.25 V, 1.25-MHz throughput |                      |       | 2                     | mA                 |
|                                  |  | At V <sub>DD</sub> = 2.35 V to 5.25 V, static state        |                      |       | 1.5                   |                    |
|                                  | Power down state supply current              | SCLK off   |                      |       | 1                     | µA                 |
|                                  |  | SCLK on (25 MHz)   |                      |       | 200                   |                    |
|                                  | Power dissipation at 1.25 MHz throughput     | V <sub>DD</sub> = 5 V                                      |                      | 8     | 10                    | mW                 |
|                                  |  | V <sub>DD</sub> = 3 V                                      |                      | 3.8   | 6                     |                    |

(1) Ideal input span; does not include gain or offset error.

(2) Refer [Figure 36](#) for details on sampling circuit

(3) LSB means least significant bit

(4) Measured relative to an ideal full-scale input

(5) Offset error and gain error ensured by characterization.

(6) First transition of 000H to 001H at 0.5 × (V<sub>ref</sub>/2<sup>10</sup>)

(7) Calculated on the first nine harmonics of the input frequency

## ADS7887 SPECIFICATIONS (continued)

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = –40°C to 125°C, f<sub>sample</sub> = 1.25 MHz

| PARAMETER                          | TEST CONDITIONS       | MIN | TYP | MAX | UNIT |
|------------------------------------|-----------------------|-----|-----|-----|------|
| Power dissipation in static state  | V <sub>DD</sub> = 5 V |     | 5.5 | 7.5 | mW   |
|                                    | V <sub>DD</sub> = 3 V |     | 3   | 4.5 |      |
| Power down time                    |                       |     |     | 0.1 | μs   |
| Power up time                      |                       |     |     | 0.8 | μs   |
| Invalid conversions after power up |                       |     |     | 1   |      |
| <b>TEMPERATURE RANGE</b>           |                       |     |     |     |      |
| Specified performance              |                       | –40 |     | 125 | °C   |

## ADS7888 SPECIFICATIONS

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = –40°C to 125°C, f<sub>sample</sub> = 1.25 MHz

| PARAMETER                                    |   | TEST CONDITIONS  | MIN                  | TYP   | MAX                   | UNIT               |
|--|---|--|----------------------|-------|-----------------------|--------------------|
| ANALOG INPUT                                 |   |  |                      |       |                       |                    |
| Full-scale input voltage span <sup>(1)</sup> |   |  | 0                    |       | V <sub>DD</sub>       | V                  |
| Absolute input voltage range                 |   | +IN  | −0.20                |       | V <sub>DD</sub> +0.20 | V                  |
| C <sub>i</sub>                               | Input capacitance <sup>(2)</sup>                          |  |                      | 21    |                       | pF                 |
| I <sub>Ilkg</sub>                            | Input leakage current                                     | T <sub>A</sub> = 125°C                                     |                      | 40    |                       | nA                 |
| SYSTEM PERFORMANCE                           |   |  |                      |       |                       |                    |
| Resolution                                   |   |  |                      | 8     |                       | Bits               |
| No missing codes                             |   |  |                      | 8     |                       | Bits               |
| INL  | Integral nonlinearity                                     |  | −0.3                 | ±0.15 | 0.3                   | LSB <sup>(3)</sup> |
| DNL  | Differential nonlinearity                                 |  | −0.3                 | ±0.1  | 0.3                   | LSB                |
| E <sub>O</sub>                               | Offset error <sup>(4)</sup> <sup>(5)</sup> <sup>(6)</sup> |  | −0.5                 | ±0.15 | 0.5                   | LSB                |
| E <sub>G</sub>                               | Gain error <sup>(5)</sup>                                 |  | −0.5                 | ±0.15 | 0.5                   | LSB                |
| SAMPLING DYNAMICS                            |   |  |                      |       |                       |                    |
| Conversion time                              |   | 25-MHz SCLK  | 450                  | 480   |                       | ns                 |
| Acquisition time                             |   | 1.5 MSPS mode, <a href="#">Figure 3</a>                    | 206                  |       |                       | ns                 |
| Maximum throughput rate                      |   | 25-MHz SCLK  |                      |       | 1.25                  | MHz                |
| Aperture delay                               |   |  |                      | 5     |                       | ns                 |
| Step Response                                |   |  |                      | 160   |                       | ns                 |
| Overvoltage recovery                         |   |  |                      | 160   |                       | ns                 |
| DYNAMIC CHARACTERISTICS                      |   |  |                      |       |                       |                    |
| THD  | Total harmonic distortion <sup>(7)</sup>                  | 100 kHz  |                      | −67.5 | −65                   | dB                 |
| SINAD  | Signal-to-noise and distortion                            | 100 kHz  | 49                   | 49.5  |                       | dB                 |
| SFDR   | Spurious free dynamic range                               | 100 kHz  | 65                   | 77    |                       | dB                 |
| Full power bandwidth                         |   | At −3 dB   |                      | 15    |                       | MHz                |
| DIGITAL INPUT/OUTPUT                         |   |  |                      |       |                       |                    |
| Logic family — CMOS                          |   |  |                      |       |                       |                    |
| V <sub>IH</sub>                              | High-level input voltage                                  | V <sub>DD</sub> = 2.35 V to 5.25 V                         | V <sub>DD</sub> −0.4 |       | 5.25                  | V                  |
| V <sub>IL</sub>                              | Low-level input voltage                                   | V <sub>DD</sub> = 5 V                                      |                      |       | 0.8                   | V                  |
|  |   | V <sub>DD</sub> = 3 V                                      |                      |       | 0.4                   |                    |
| V <sub>OH</sub>                              | High-level output voltage                                 | At I <sub>source</sub> = 200 μA                            | V <sub>DD</sub> −0.2 |       |                       | V                  |
| V <sub>OL</sub>                              | Low-level output voltage                                  | At I <sub>sink</sub> = 200 μA                              |                      |       | 0.4                   |                    |
| POWER SUPPLY REQUIREMENTS                    |   |  |                      |       |                       |                    |
| +V <sub>DD</sub>                             | Supply voltage  |  | 2.35                 | 3.3   | 5.25                  | V                  |
|  | Supply current (normal mode)                              | At V <sub>DD</sub> = 2.35 V to 5.25 V, 1.25-MHz throughput |                      |       | 2                     | mA                 |
|  |   | At V <sub>DD</sub> = 2.35 V to 5.25 V, static state        |                      |       | 1.5                   |                    |
|  | Power down state supply current                           | SCLK off   |                      |       | 1                     | μA                 |
|  |   | SCLK on (25 MHz)   |                      |       | 200                   |                    |
|  | Power dissipation at 1.25 MHz throughput                  | V <sub>DD</sub> = 5 V                                      |                      | 8     | 10                    | mW                 |
|  |   | V <sub>DD</sub> = 3 V                                      |                      | 3.8   | 6                     |                    |

(1) Ideal input span; does not include gain or offset error.

(2) Refer [Figure 36](#) for details on sampling circuit

(3) LSB means least significant bit

(4) Measured relative to an ideal full-scale input

(5) Offset error and gain error ensured by characterization.

(6) First transition of 000H to 001H at (V<sub>ref</sub>/2<sup>8</sup>)

(7) Calculated on the first nine harmonics of the input frequency

## ADS7888 SPECIFICATIONS (continued)

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = –40°C to 125°C, f<sub>sample</sub> = 1.25 MHz

| PARAMETER                          | TEST CONDITIONS       | MIN | TYP | MAX | UNIT |
|------------------------------------|-----------------------|-----|-----|-----|------|
| Power dissipation in static state  | V <sub>DD</sub> = 5 V |     | 5.5 | 7.5 | mW   |
|                                    | V <sub>DD</sub> = 3 V |     | 3   | 4.5 |      |
| Power down time                    |                       |     |     | 0.1 | μs   |
| Power up time                      |                       |     |     | 0.8 | μs   |
| Invalid conversions after power up |                       |     |     | 1   |      |
| <b>TEMPERATURE RANGE</b>           |                       |     |     |     |      |
| Specified performance              |                       | –40 |     | 125 | °C   |

## TIMING REQUIREMENTS (see Figure 1)

All specifications typical at T<sub>A</sub> = –40°C to 125°C, V<sub>DD</sub> = 2.35 V to 5.25 V, unless otherwise specified.

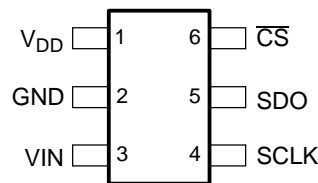
| PARAMETER   |         | TEST CONDITIONS <sup>(1)</sup> | MIN                     | TYP | MAX                    | UNIT |
|---|---------|--------------------------------|-------------------------|-----|------------------------|------|
| t <sub>conv</sub> Conversion time   | ADS7887 | V <sub>DD</sub> = 3 V          |                         |     | 14 × t <sub>SCLK</sub> | ns   |
|   |         | V <sub>DD</sub> = 5 V          |                         |     | 14 × t <sub>SCLK</sub> |      |
|   | ADS7888 | V <sub>DD</sub> = 3 V          |                         |     | 12 × t <sub>SCLK</sub> |      |
|   |         | V <sub>DD</sub> = 5 V          |                         |     | 12 × t <sub>SCLK</sub> |      |
| t <sub>q</sub> Minimum quiet time needed from bus 3-state to start of next conversion   |         | V <sub>DD</sub> = 3 V          | 40                      |     |                        | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 40                      |     |                        |      |
| t <sub>d1</sub> Delay time, $\overline{CS}$ low to first data (0) out   |         | V <sub>DD</sub> = 3 V          |                         | 15  | 25                     | ns   |
|   |         | V <sub>DD</sub> = 5 V          |                         | 13  | 25                     |      |
| t <sub>su1</sub> Setup time, $\overline{CS}$ low to SCLK low  |         | V <sub>DD</sub> = 3 V          | 10                      |     |                        | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 10                      |     |                        |      |
| t <sub>d2</sub> Delay time, SCLK falling to SDO   |         | V <sub>DD</sub> = 3 V          |                         | 15  | 25                     | ns   |
|   |         | V <sub>DD</sub> = 5 V          |                         | 13  | 25                     |      |
| t <sub>h1</sub> Hold time, SCLK falling to data valid <sup>(2)</sup>  |         | V <sub>DD</sub> < 3 V          | 7                       |     |                        | ns   |
|   |         | V <sub>DD</sub> > 5 V          | 5.5                     |     |                        |      |
| t <sub>d3</sub> Delay time, 16th SCLK falling edge to SDO 3-state   |         | V <sub>DD</sub> = 3 V          |                         | 10  | 25                     | ns   |
|   |         | V <sub>DD</sub> = 5 V          |                         | 8   | 20                     |      |
| t <sub>w1</sub> Pulse duration, $\overline{CS}$   |         | V <sub>DD</sub> = 3 V          | 25                      | 40  |                        | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 25                      | 40  |                        |      |
| t <sub>d4</sub> Delay time, $\overline{CS}$ high to SDO 3-state, Figure 3   |         | V <sub>DD</sub> = 3 V          |                         | 17  | 30                     | ns   |
|   |         | V <sub>DD</sub> = 5 V          |                         | 15  | 25                     |      |
| t <sub>WH</sub> Pulse duration, SCLK high   |         | V <sub>DD</sub> = 3 V          | 0.4 × t <sub>SCLK</sub> |     |                        | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 0.4 × t <sub>SCLK</sub> |     |                        |      |
| t <sub>WL</sub> Pulse duration, SCLK low  |         | V <sub>DD</sub> = 3 V          | 0.4 × t <sub>SCLK</sub> |     |                        | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 0.4 × t <sub>SCLK</sub> |     |                        |      |
| Frequency, SCLK   |         | V <sub>DD</sub> = 3 V          |                         |     | 25                     | MHz  |
|   |         | V <sub>DD</sub> = 5 V          |                         |     | 25                     |      |
| t <sub>d5</sub> Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use min spec not to accidentally enter in powerdown) Figure 4 |         | V <sub>DD</sub> = 3 V          | –2                      |     | 5                      | ns   |
|   |         | V <sub>DD</sub> = 5 V          | –2                      |     | 5                      |      |
| t <sub>d6</sub> Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use max spec not to accidentally enter in powerdown) Figure 4   |         | V <sub>DD</sub> = 3 V          | 2                       |     | –5                     | ns   |
|   |         | V <sub>DD</sub> = 5 V          | 2                       |     | –5                     |      |

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.

(2) With 50-pf load.

## DEVICE INFORMATION

### SOT23/SC70 PACKAGE (TOP VIEW)



## TERMINAL FUNCTIONS

| TERMINAL               |     | I/O | DESCRIPTION  |
|------------------------|-----|-----|--|
| NAME                   | NO. |     |  |
| V <sub>DD</sub>        | 1   | –   | Power supply input also acts like a reference voltage to ADC.                                  |
| GND                    | 2   | –   | Ground for power supply, all analog and digital signals are referred with respect to this pin. |
| VIN                    | 3   | I   | Analog signal input  |
| SCLK                   | 4   | I   | Serial clock   |
| SDO                    | 5   | O   | Serial data out  |
| $\overline{\text{CS}}$ | 6   | I   | Chip select signal, active low   |

## ADS7887 NORMAL OPERATION

The cycle begins with the falling edge of  $\overline{\text{CS}}$ . This point is indicated as **a** in Figure 1. With the falling edge of  $\overline{\text{CS}}$ , the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 10-bit data in MSB first format and padded by 2 lagging zeros.

The falling edge of  $\overline{\text{CS}}$  clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with two lagging zeros as shown in Figure 1. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 14th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by **b** in Figure 1.

$\overline{\text{CS}}$  can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling  $\overline{\text{CS}}$  low until the end of the quiet time ( $t_q$ ) after SDO goes to 3-state. To continue normal operation, it is necessary that  $\overline{\text{CS}}$  is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.)  $\overline{\text{CS}}$  going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V<sub>DD</sub>. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels (V<sub>OH</sub> and V<sub>OL</sub>) are governed by V<sub>DD</sub> as listed in the SPECIFICATIONS table.

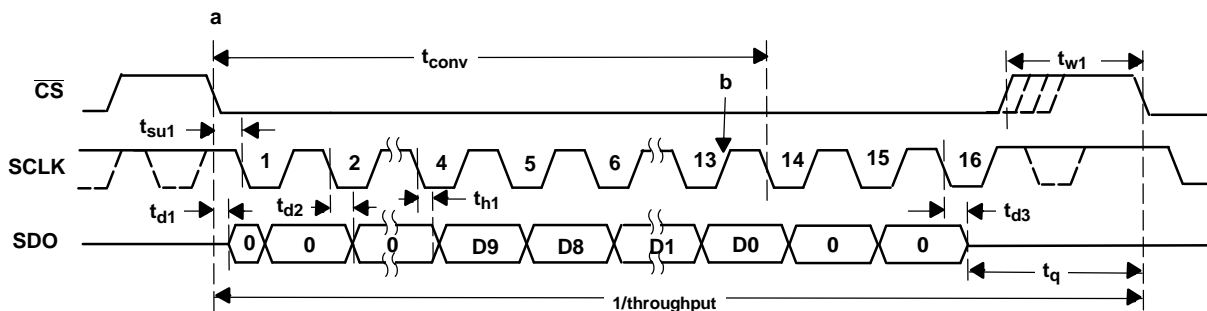


Figure 1. ADS7887 Interface Timing Diagram



## ADS7888 NORMAL OPERATION

The cycle begins with the falling edge of  $\overline{CS}$ . This point is indicated as **a** in Figure 2. With the falling edge of  $\overline{CS}$ , the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 8-bit data in MSB first format and padded by 4 lagging zeros.

The falling edge of  $\overline{CS}$  clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with four lagging zeros as shown in Figure 2. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 12th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 11th falling edge. This point is indicated by **b** in Figure 2.

$\overline{CS}$  can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling  $\overline{CS}$  low until the end of the quiet time ( $t_q$ ) after SDO goes to 3-state. To continue normal operation, it is necessary that  $\overline{CS}$  is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.)  $\overline{CS}$  going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device  $V_{DD}$ . This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels ( $V_{OH}$  and  $V_{OL}$ ) are governed by  $V_{DD}$  as listed in the SPECIFICATIONS section.

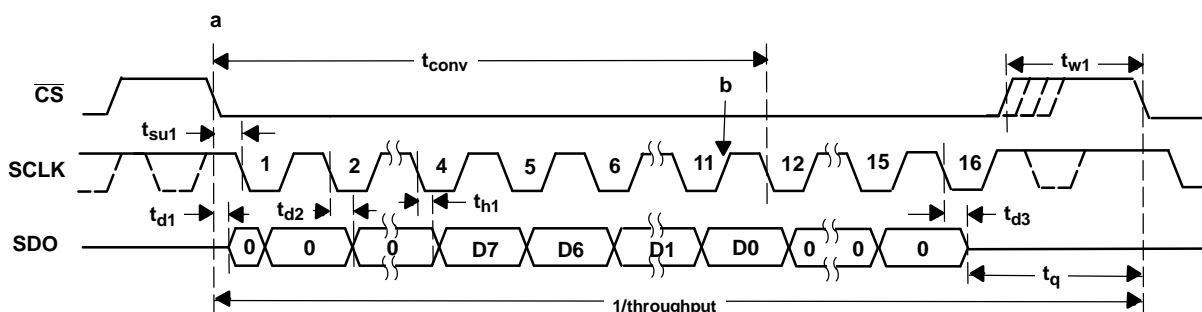


Figure 2. ADS7888 Interface Timing Diagram

As shown in Figure 3, the ADS7888 can achieve 1.5-MSPS throughput.  $\overline{CS}$  can be pulled high after the 12th falling edge (with a 25-MHz SCLK). SDO goes to 3-state after the LSB (as  $\overline{CS}$  is high).  $\overline{CS}$  can be pulled low at the end of the quiet time ( $t_q$ ) after SDO goes to 3-state.

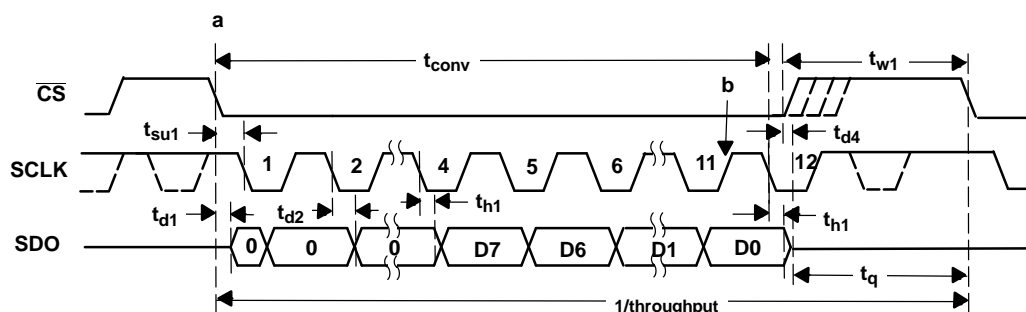
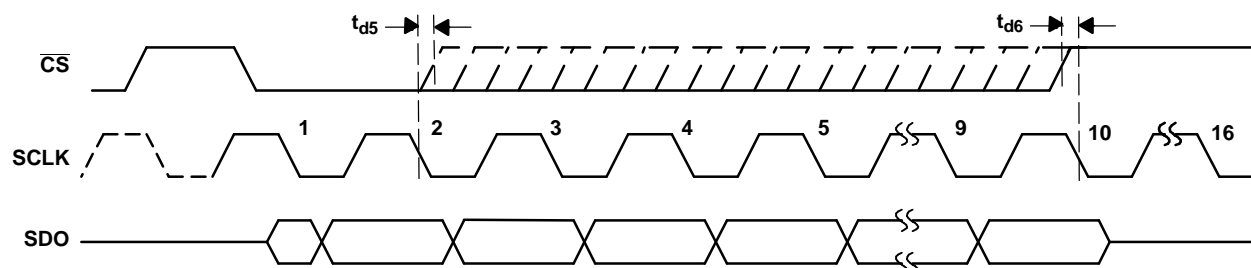


Figure 3. ADS7888 Interface Timing Diagram, Data Transfer with 12-Clock Frame

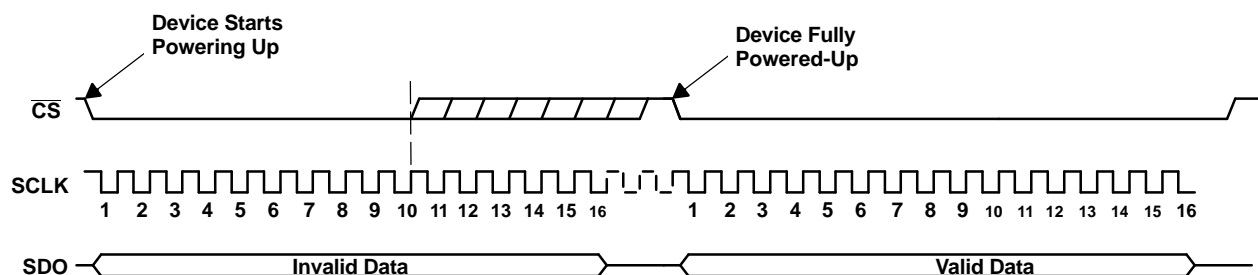
## POWER DOWN MODE

The device enters power down mode if  $\overline{CS}$  goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power down condition as shown in Figure 4.



**Figure 4. Entering Power Down Mode**

A dummy cycle with  $\overline{CS}$  low for more than 10 SCLK falling edges brings the device out of power down mode. For the device to come to the fully powered up condition it takes 0.8  $\mu$ s.  $\overline{CS}$  can be pulled high any time after the 10th falling edge as shown in Figure 5. It is not necessary to continue until the 16th clock if the next conversion starts 0.8  $\mu$ s after  $\overline{CS}$  going low of the dummy cycle and the quiet time ( $t_q$ ) condition is met.



**Figure 5. Exiting Power Down Mode**

# TYPICAL CHARACTERISTICS ADS7887, ADS7888

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

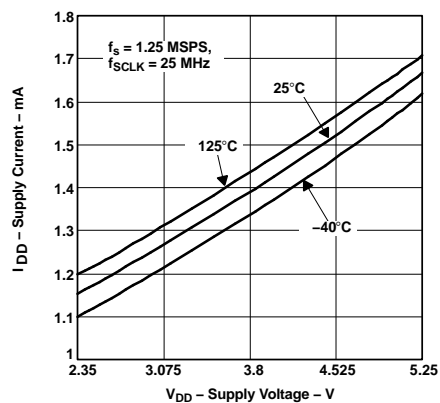


Figure 6.

**SUPPLY CURRENT  
vs  
SCLK FREQUENCY**

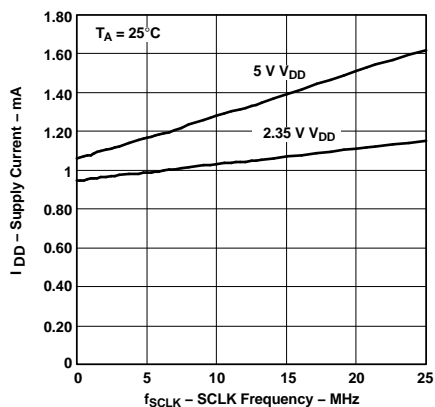


Figure 7.

**SUPPLY CURRENT  
vs  
SAMPLE RATE**

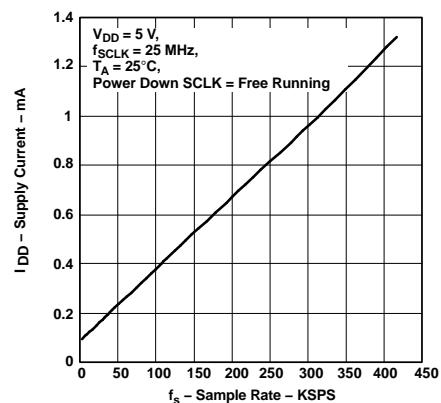


Figure 8.

**ANALOG INPUT  
LEAKAGE CURRENT  
vs  
FREE-AIR TEMPERATURE**

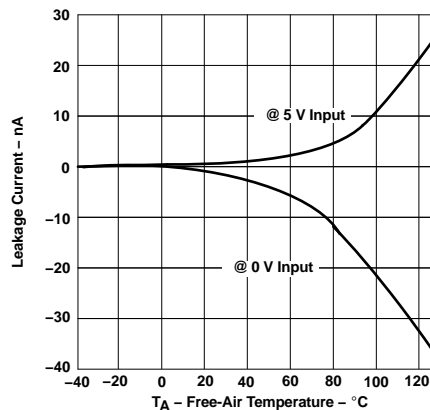


Figure 9.

# TYPICAL CHARACTERISTICS ADS7887

**SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
INPUT FREQUENCY**

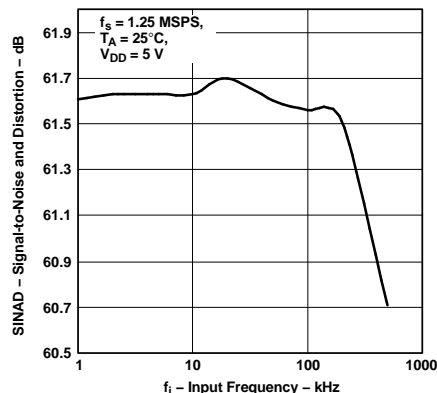


Figure 10.

**SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
SUPPLY VOLTAGE**

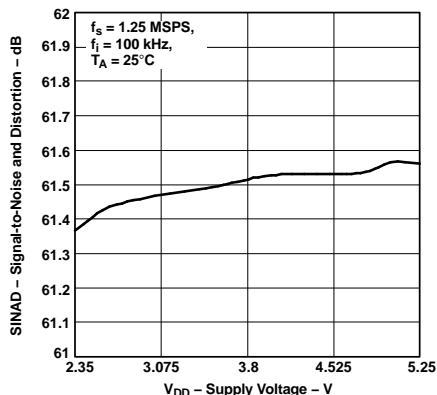


Figure 11.

**TOTAL HARMONIC DISTORTION  
VS  
INPUT FREQUENCY**

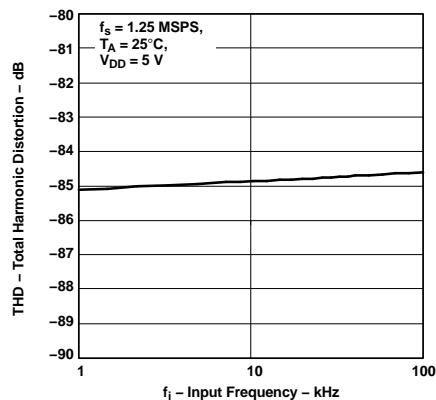


Figure 12.

**TOTAL HARMONIC DISTORTION  
VS  
SUPPLY VOLTAGE**

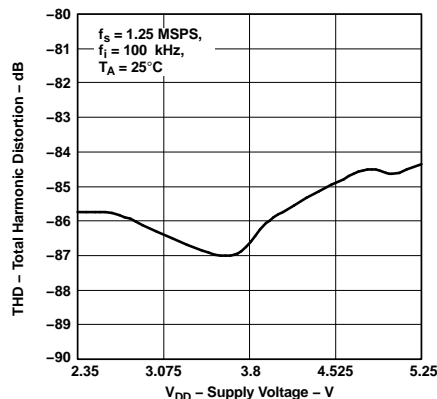


Figure 13.

**SPURIOUS FREE DYNAMIC RANGE  
VS  
INPUT FREQUENCY**

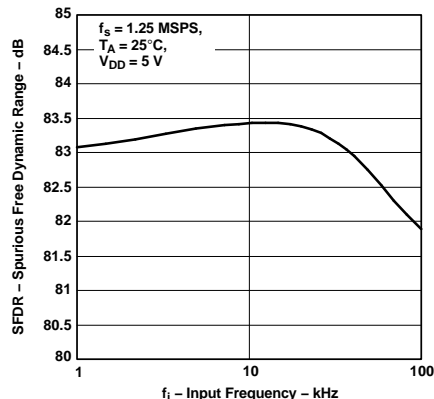


Figure 14.

**SPURIOUS FREE DYNAMIC RANGE  
VS  
SUPPLY VOLTAGE**

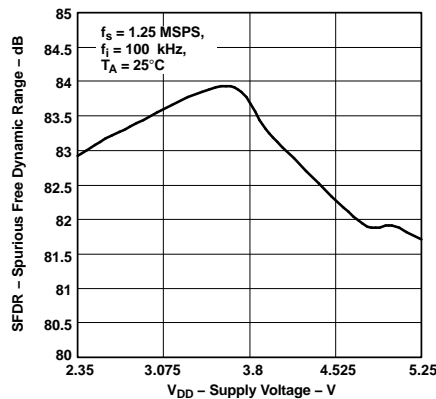


Figure 15.

**OFFSET ERROR  
VS  
SUPPLY VOLTAGE**

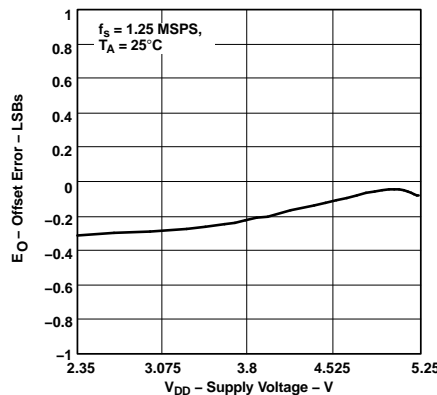


Figure 16.

**OFFSET ERROR  
VS  
FREE-AIR TEMPERATURE**

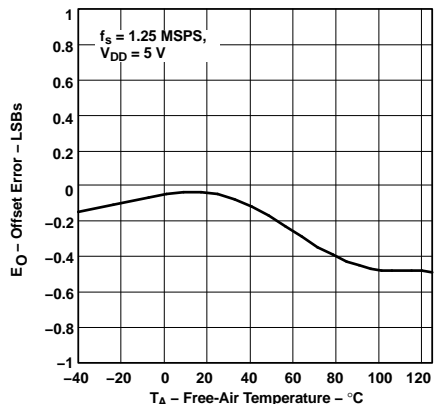


Figure 17.

**GAIN ERROR  
VS  
SUPPLY VOLTAGE**

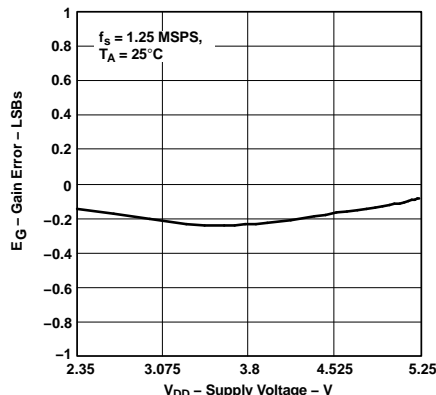


Figure 18.

## TYPICAL CHARACTERISTICS ADS7887 (continued)

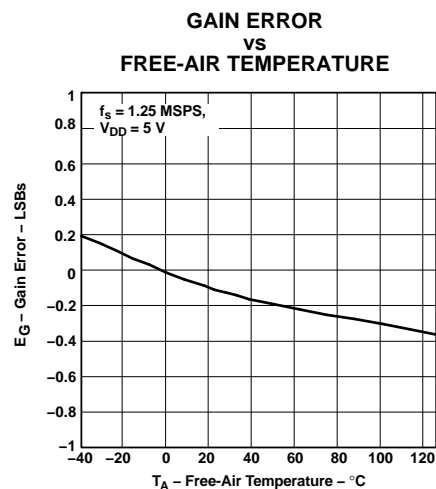


Figure 19.

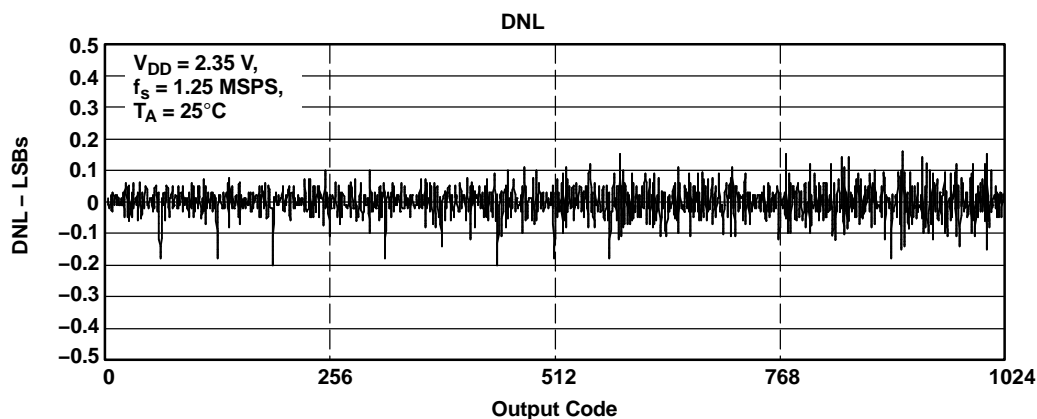


Figure 20.

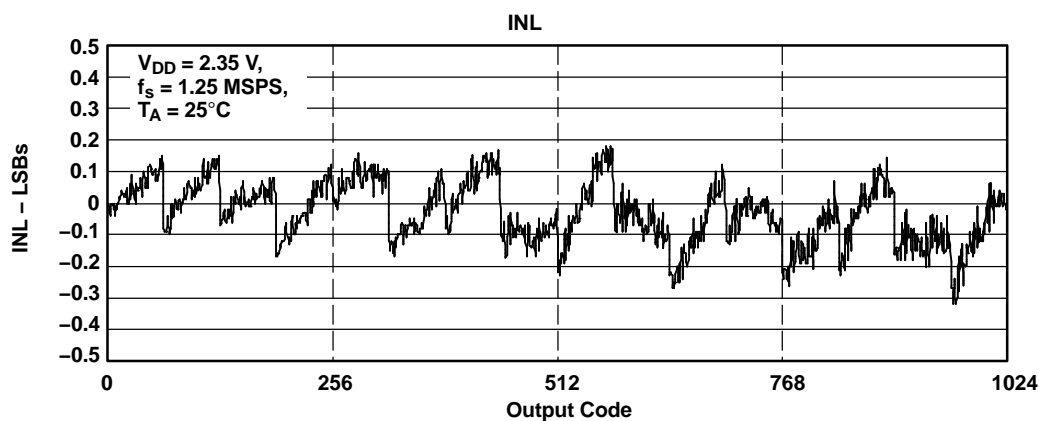
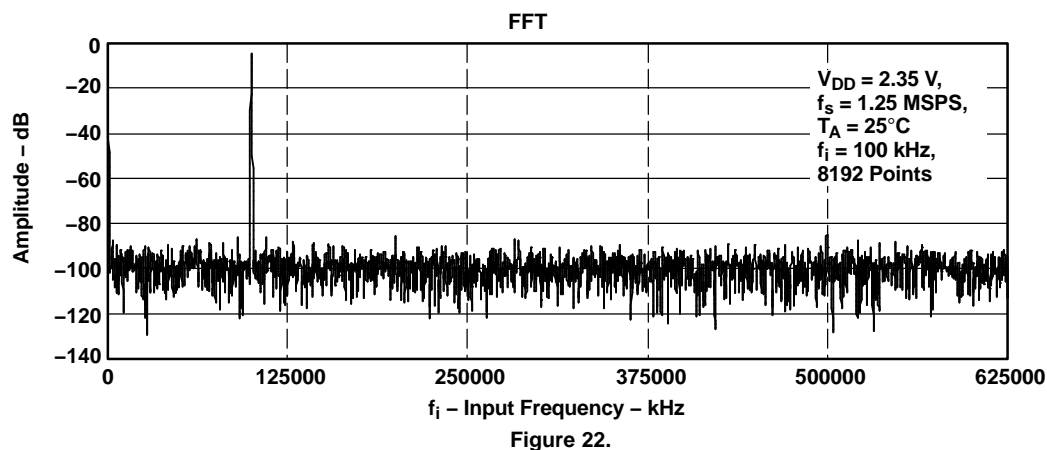


Figure 21.

**TYPICAL CHARACTERISTICS ADS7887 (continued)**



## TYPICAL CHARACTERISTICS ADS7888

**SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
INPUT FREQUENCY**

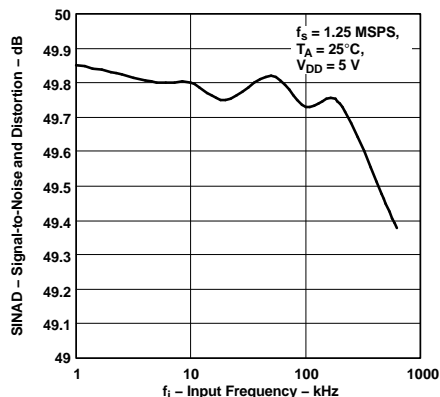


Figure 23.

**SIGNAL-TO-NOISE  
AND DISTORTION  
VS  
SUPPLY VOLTAGE**

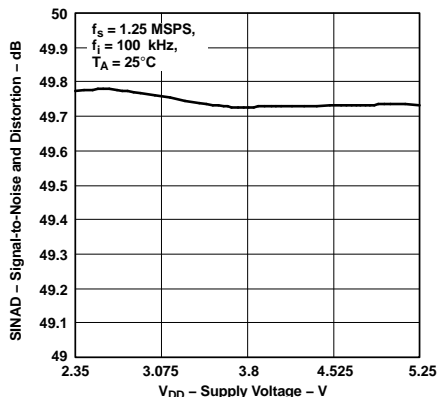


Figure 24.

**TOTAL HARMONIC DISTORTION  
VS  
INPUT FREQUENCY**

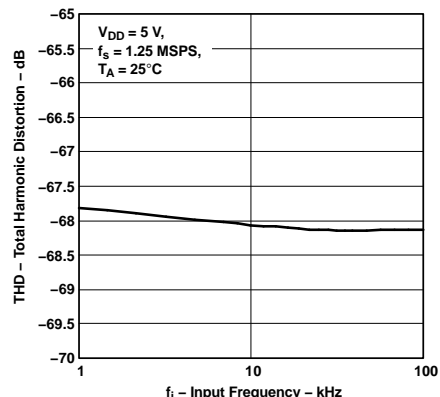


Figure 25.

**TOTAL HARMONIC DISTORTION  
VS  
SUPPLY VOLTAGE**

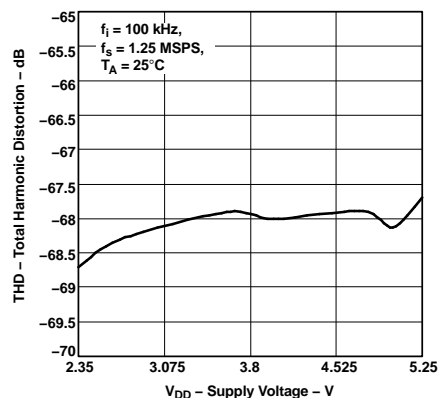


Figure 26.

**SPURIOUS FREE DYNAMIC RANGE  
VS  
INPUT FREQUENCY**

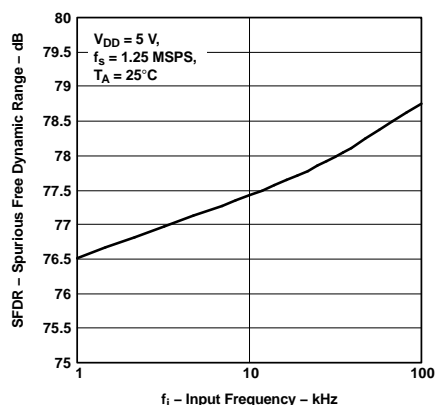


Figure 27.

**SPURIOUS FREE DYNAMIC RANGE  
VS  
SUPPLY VOLTAGE**

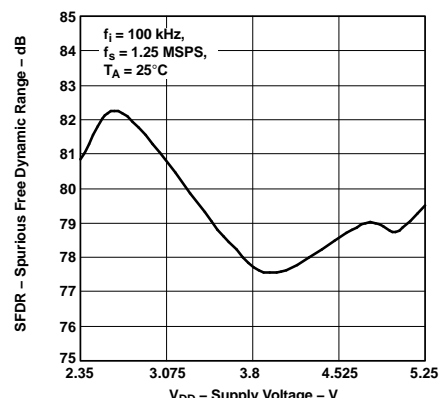


Figure 28.

**OFFSET ERROR  
VS  
SUPPLY VOLTAGE**

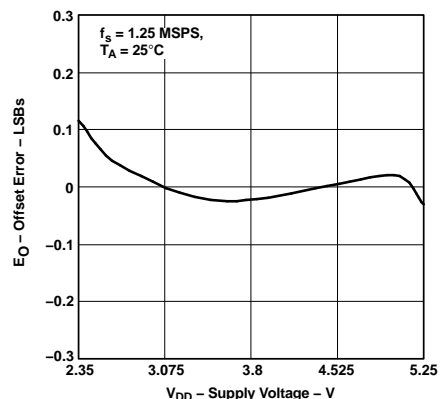


Figure 29.

**OFFSET ERROR  
VS  
FREE-AIR TEMPERATURE**

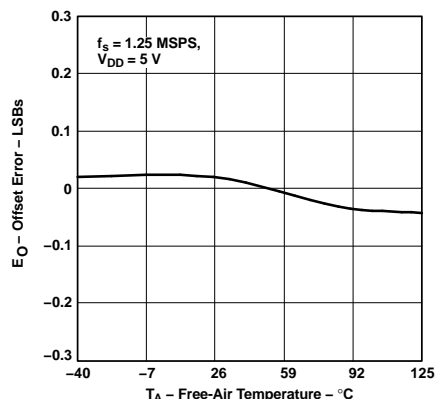


Figure 30.

**GAIN ERROR  
VS  
SUPPLY VOLTAGE**

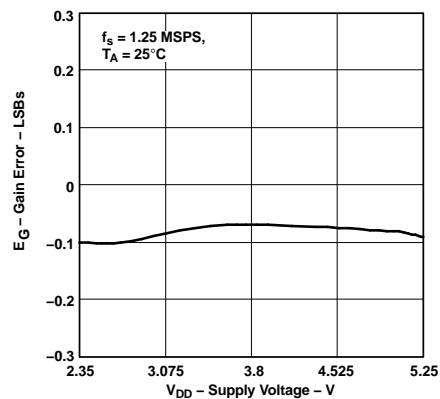


Figure 31.

## TYPICAL CHARACTERISTICS ADS7888 (continued)

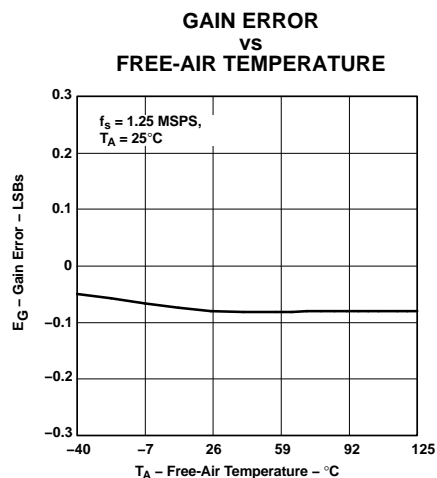


Figure 32.

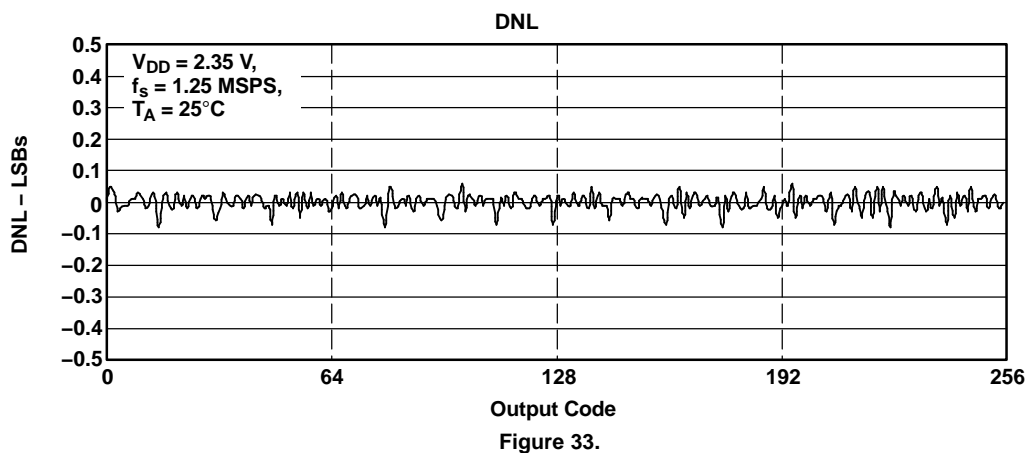


Figure 33.

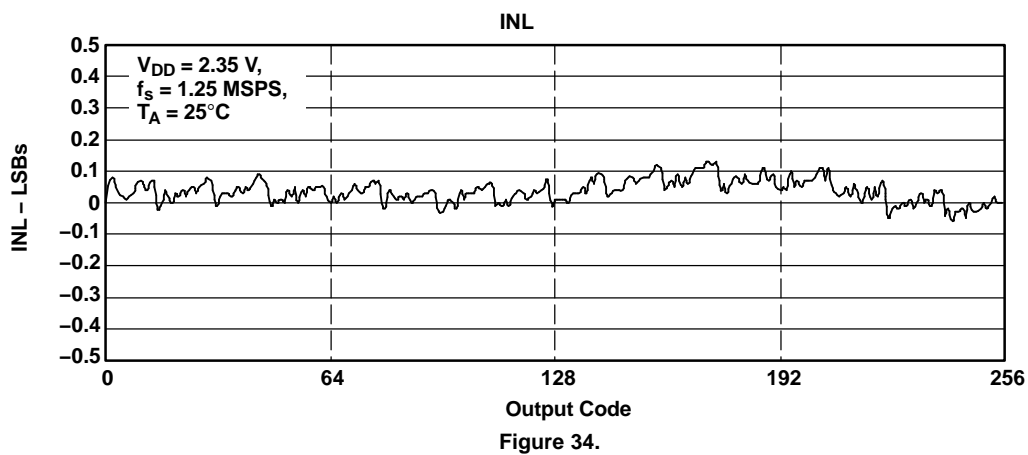


Figure 34.



## TYPICAL CHARACTERISTICS ADS7888 (continued)

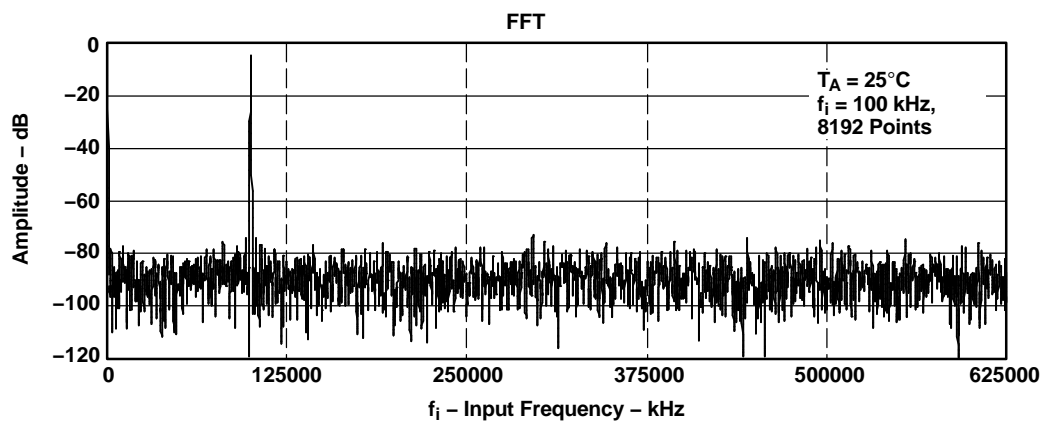


Figure 35.

## APPLICATION INFORMATION

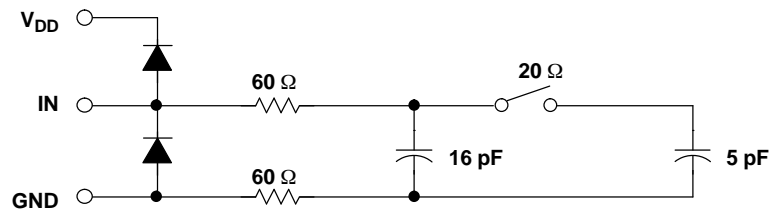


Figure 36. Typical Equivalent Sampling Circuit

### Driving the VIN and V<sub>DD</sub> Pins of the ADS7887 and ADS7888

The VIN input to the ADS7887 and ADS7888 should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-μF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7887 and ADS7888 draw very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like REF3030 or REF3130. The ADS7887 and ADS7888 can operate off a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. [Figure 38](#) shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V<sub>DD</sub> input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. [Figure 39](#) shows one possible application circuit.

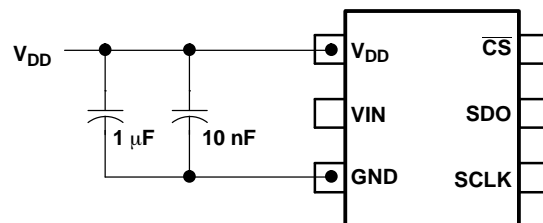


Figure 37. Supply/Reference Decoupling Capacitors

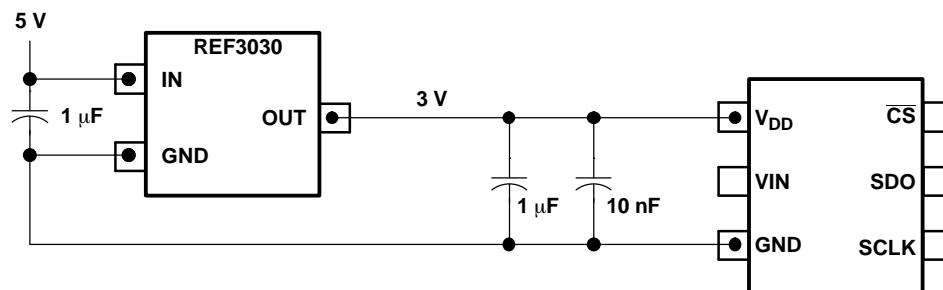
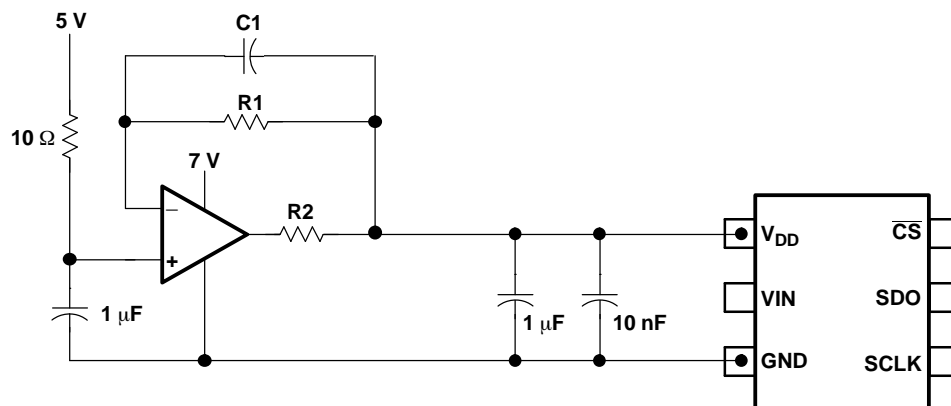


Figure 38. Using the REF3030 Reference

## APPLICATION INFORMATION (continued)



**Figure 39. Buffering with the OPA735**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| ADS7887SDBVR     | ACTIVE                | SOT-23       | DBV             | 6    | 3000        | TBD                     | Call TI          | Call TI                      |
| ADS7887SDBVT     | ACTIVE                | SOT-23       | DBV             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-1-260C-UNLIM           |
| ADS7887SDBVTG4   | ACTIVE                | SOT-23       | DBV             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-1-260C-UNLIM           |
| ADS7887SDCKR     | ACTIVE                | SC70         | DCK             | 6    | 3000        | TBD                     | Call TI          | Call TI                      |
| ADS7887SDCKT     | ACTIVE                | SC70         | DCK             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-2-260C-1 YEAR          |
| ADS7887SDCKTG4   | ACTIVE                | SC70         | DCK             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-2-260C-1 YEAR          |
| ADS7888SDBVR     | ACTIVE                | SOT-23       | DBV             | 6    | 3000        | TBD                     | Call TI          | Call TI                      |
| ADS7888SDBVT     | ACTIVE                | SOT-23       | DBV             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-1-260C-UNLIM           |
| ADS7888SDBVTG4   | ACTIVE                | SOT-23       | DBV             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-1-260C-UNLIM           |
| ADS7888SDCKR     | ACTIVE                | SC70         | DCK             | 6    | 3000        | TBD                     | Call TI          | Call TI                      |
| ADS7888SDCKT     | ACTIVE                | SC70         | DCK             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-2-260C-1 YEAR          |
| ADS7888SDCKTG4   | ACTIVE                | SC70         | DCK             | 6    | 250         | Green (RoHS & no Sb/Br) | Call TI          | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

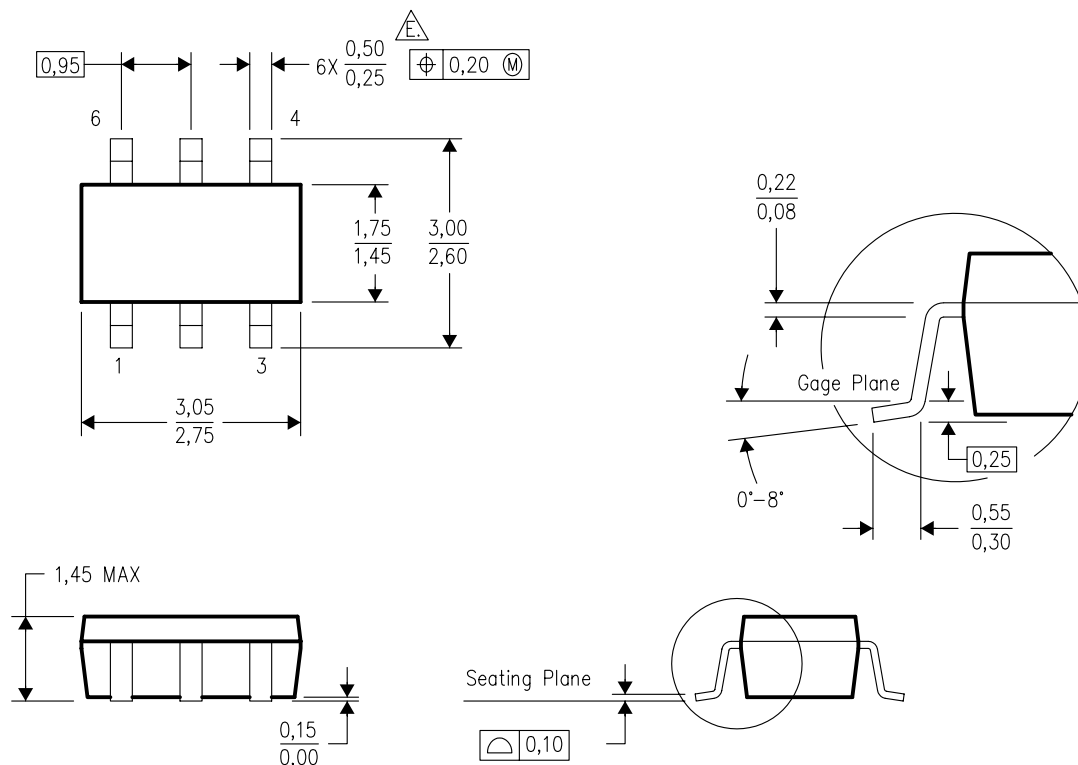
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DBV (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

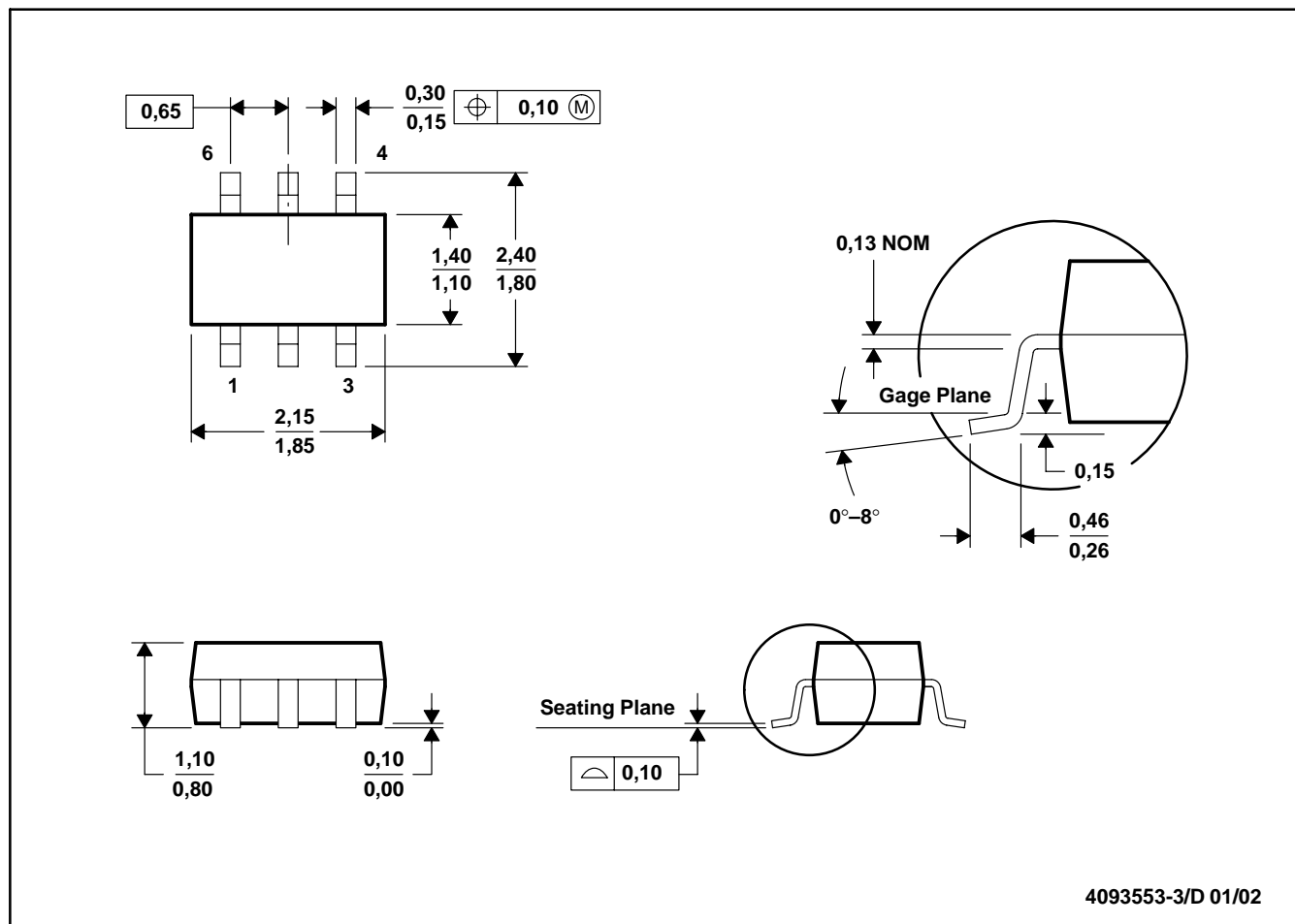


4073253-5/1 04/2005

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-203

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