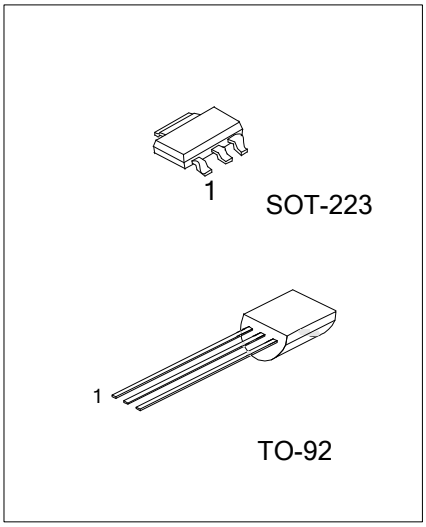
UT131

TRIAC

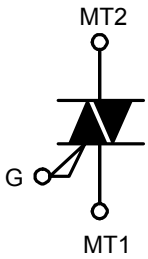
TRIACS LOGIC LEVEL



■ DESCRIPTION

Passivated, sensitive gate triaces in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers. Logic integrated circuits and other low power gate trigger circuits.

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT131L-x-T92-B	UT131L-x-T92-B	TO-92	MT1	GATE	MT2	Tape Box
UT131L-x-T92-K	UT131L-x-T92-K	TO-92	MT1	GATE	MT2	Bulk
UT131L-x-T92-R	UT131L-x-T92-R	TO-92	MT1	GATE	MT2	Tape Reel
UT131L-x-AA3-R	UT131G-x-AA3-R	SOT-223	MT1	MT2	GATE	Tape Reel

UT131L-x-T92-B
(1)Packing Type
(2)Package Type
(3)Peak Voltage
(4)Lead Free

(1) R:Tape Reel, B: Tape Box, K: Bulk
(2) AA3: SOT-223, T92: TO-92
(3) 5: 500V, 6: 600V, 8: 800V
(4) G:Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltage (Note 2)	UT131-5	V_{DRM}	500	V
	UT131-6		600	V
	UT131-8		800	V
RMS On-State Current, Full Sine Wave; Tlead≤51℃		$I_{T(RMS)}$	1	A
Non-Repetitive Peak On-State Current (Full Sine Wave; T_J=25℃ Prior to Surge)	t=20ms	I_{TSM}	16	A
	t=16.7ms		17.6	A
Circuit Fusing	t=10ms	I^2t	1.28	A^2s
Repetitive Rate of Rise of On-State Current after Triggering I_{TM}=1.5A, I_G=0.2A, dI_G/dt=0.2A/μs	T2 + G +	dI_T/dt	50	A/μs
	T2 + G -		50	A/μs
	T2 - G -		50	A/μs
	T2 - G +		10	A/μs
Peak Gate Voltage		V_{GM}	5	V
Peak Gate Current		I_{GM}	2	A
Peak Gate Power		P_{GM}	5	W
Average Gate Power (over any 20ms period)		$P_{G(AV)}$	0.5	W
Junction Temperature		T_J	+125	℃
Storage Temperature		T_{STG}	-40 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Lead	Full Cycle	θ_{JLEAD}	60	K/W
	Half Cycle		80	K/W
Junction to Ambient (Note)		θ_{JA}	150	K/W

Note: PCB mounted; lead length=4mm

■ ELECTRICAL CHARACTERISTICS (T_J=25℃, unless otherwise specified)

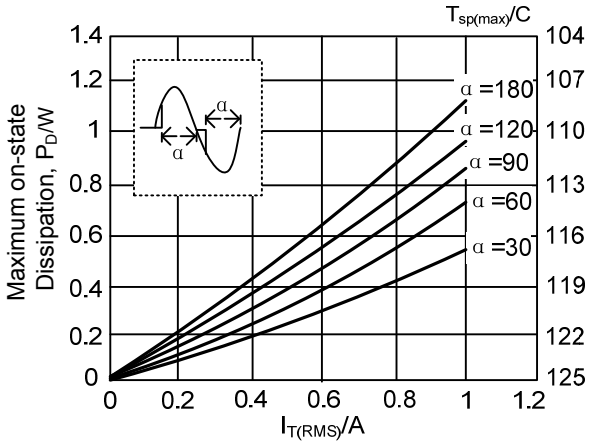
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gate Trigger Current	I_{GT}	V_D=12V, I_T=0.1A	T2 + G +		0.4	3	mA
			T2 + G -		1.3	3	mA
			T2 – G -		1.4	5	mA
			T2 – G +		3.8	7	mA
Latching Current	I_L	V_D=12V, I_{GT}=0.1A	T2 + G +		1.2	5	mA
			T2 + G -		4.0	8	mA
			T2 – G -		1.0	5	mA
			T2 – G +		2.5	8	mA
Holding Current	I_H	V_D=12V, I_{GT}=0.1A			1.3	5	mA
On -State Voltage	V_T	I_T=2.0A			1.2	1.5	V
Gate Trigger Voltage	V_{GT}	V_D=12V, I_T=0.1A			0.7	1.5	V
		V_D=400V, I_T=0.1A, T_J=125℃		0.2	0.3		V
Off-State Leakage Current	I_D	V_D=$V_{DRM(MAX)}$, T_J=125℃			0.1	0.5	mA

■ DYNAMIC CHARACTERISTICS (T_J=25℃, unless otherwise specified)

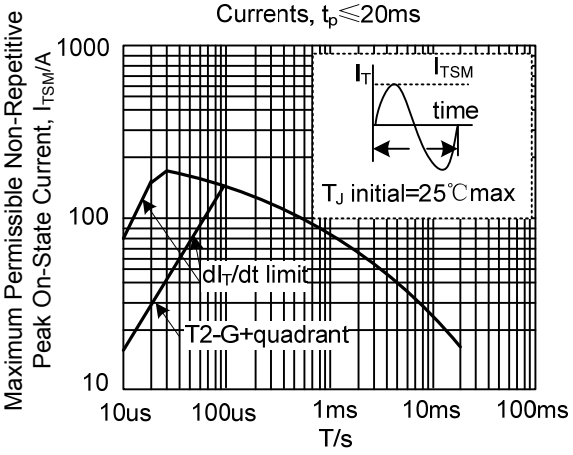
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off-state Voltage	dV_D/dt	V_{DM}=67% $V_{DRM(MAX)}$, T_J=125℃ Exponential waveform, R_{GK}=1kΩ	5	15		V/μs
Gate Controlled Turn-on Time	t_{GT}	I_{TM}=1.5A, V_D=$V_{DRM(MAX)}$, I_G=0.1A dI_G/dt=5A/μs		2		μs

■ TYPICAL CHARACTERISTICS

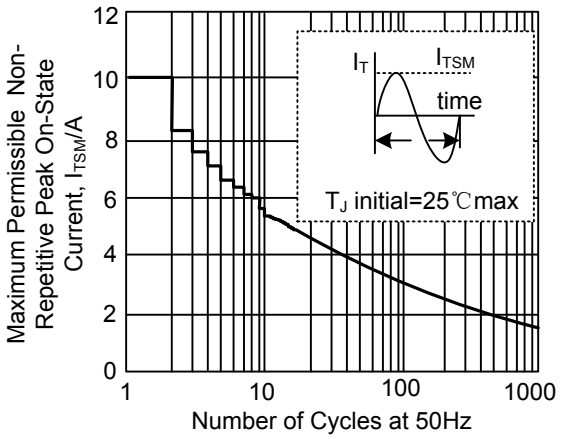
Maximum on-state Dissipation vs. RMS On-state Current, $I_{T(RMS)}$, Where α =conduction Angle



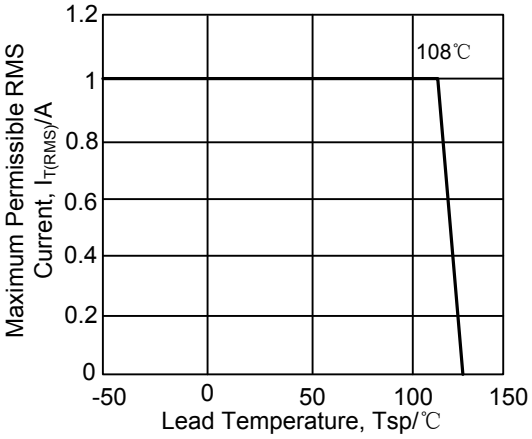
Maximum Permissible Non-repetitive Peak On-state Current vs. Pulse Width t_p, for Sinusoidal Currents, $t_p \leqslant 20ms$



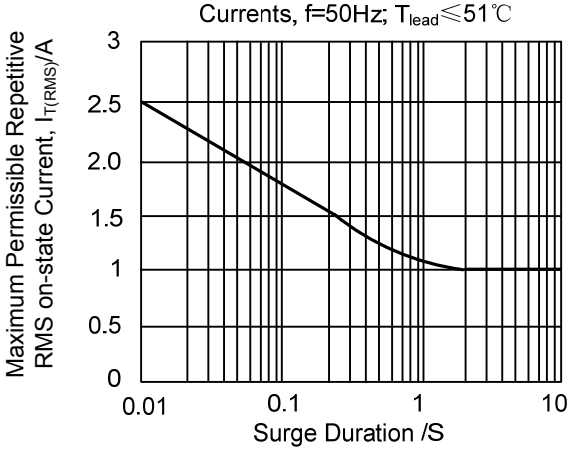
Maximum Permissible Non-Repetitive Peak On-State Current vs. Number of Cycles, for Sinusoidal Currents



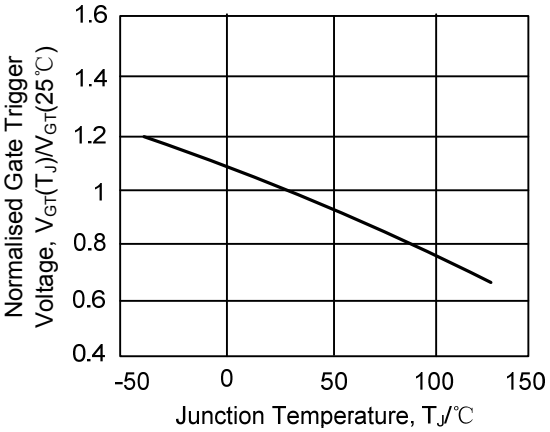
Maximum Permissible RMS Current $I_{T(RMS)}$ vs. Lead Temperature



Maximum Permissible Repetitive RMS on-state Current vs. Surge Duration, for Sinusoidal Currents, f=50Hz; $T_{lead} \leqslant 51℃$

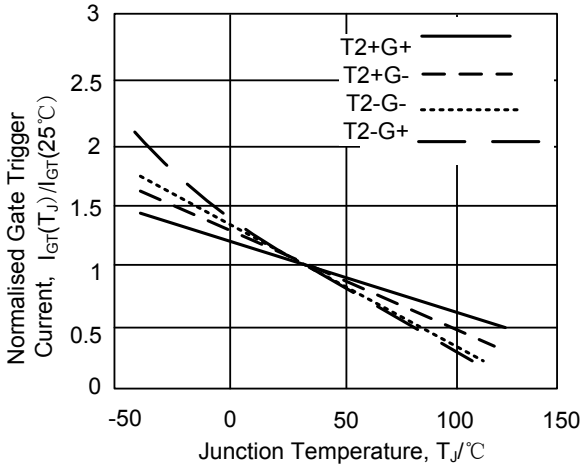


Normalised Gate Trigger Voltage vs. Junction Temperature

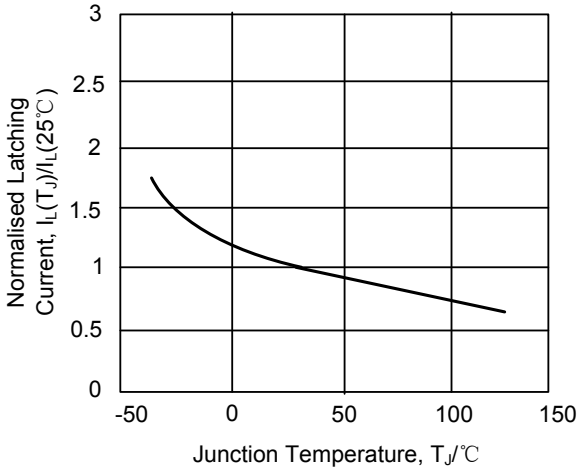


■ TYPICAL CHARACTERISTICS(Cont.)

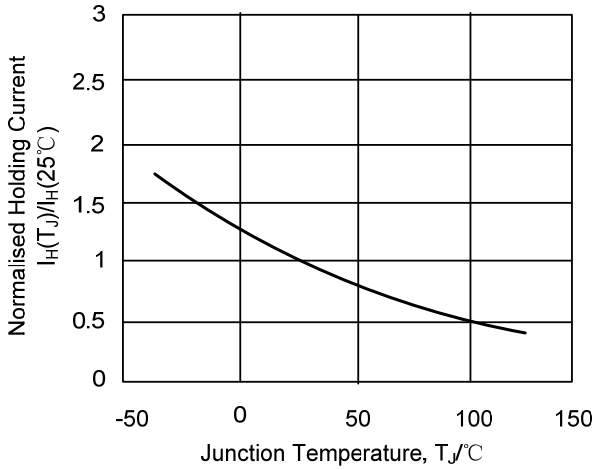
Normalised Gate Trigger Current vs. Junction Temperature



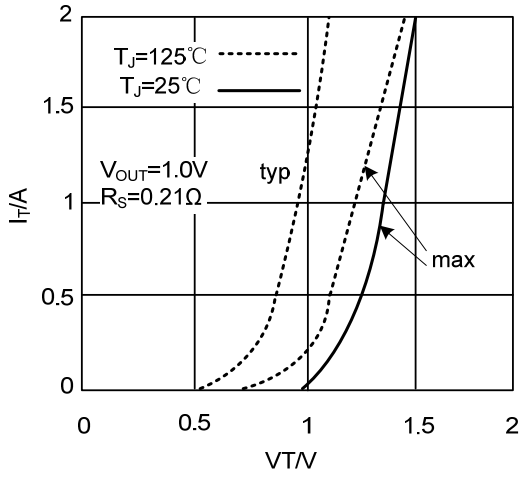
Normalised Latching Current vs. Junction Temperature



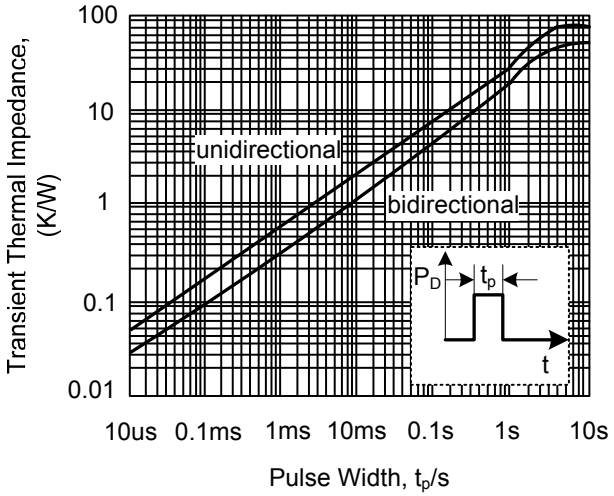
Normalised Holding Current vs. Junction Temperature



Typical and Maximum On-State Characteristic



Transient Thermal Impedance vs. Pulse Width



Typical Critical Rate of Rise of off-state Voltage vs. Junction Temperature