

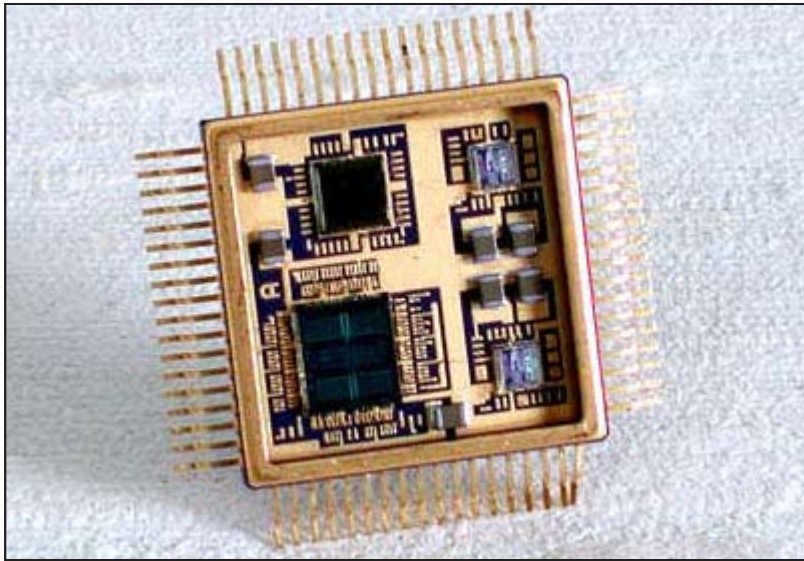
BU-65178/65179*/61588/61688*/61689* MINIATURE ADVANCED COMMUNICATION ENGINE (MINI-ACE) AND MINI-ACE PLUS*

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has...



● FEATURES

- **5 Volt Only**
- **Fully Integrated MIL-STD-1553 A/B STANAG 3838 Compliant Terminals**
- **One-Square-Inch Package**
- **Smallest BC/RT/MT In The Industry**
- **Hardware and Software Compatible with BU-61580 ACE Series**
- **Flexible Processor/Memory Interface**
- **Bootable RT* Option**
- **4K x 16 or 64K x 16* Shared RAM**
- **Automatic BC Retries**
- **Programmable BC Gap Times**
- **Programmable Illegalization**
- **Simultaneous RT/Monitor Mode**
- **Operates From 10*/12/16/20* MHz Clock**



DESCRIPTION

The BU-61588 Mini-ACE and BU-61688 Mini-ACE Plus* integrates two 5-volt-only transceivers, protocol, memory management, processor interface logic, and 4K x 16, or 64K x 16* words of RAM in a choice of pin grid array (PGA), quad flat pack or gull lead packages. The Mini-ACE is packaged in a 1.0 square inch, low profile, cofired ceramic multi-chip-module (MCM) package making it the smallest integrated MIL-STD-1553 BC/RT/MT in the industry.

The Mini-ACE provides full compatibility to DDC's BU-61580 and BU-65170 Advanced Communication Engine (ACE). As such, the Mini-ACE includes all the hardware and software architectural features of the ACE.

The Mini-ACE contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The memory management scheme for RT mode provides three data structures for buffering data. These structures, combined with the Mini-ACE's extensive interrupt capability, serve to ensure data consistency while off-loading the host processor.

The Mini-ACE Plus* can optionally boot-up as a RT with the Busy bit set for 1760 applications. The Mini-ACE BC mode implements several features aimed at providing an efficient real-time software interface to the host processor including automatic retries, programmable intermessage gap times, automatic frame repetition, and flexible interrupt generation.

The advanced architectural features of the Mini-ACE, combined with its small size and high reliability, make it an ideal choice for demanding military and industrial processor-to-1553 applications.

FOR MORE INFORMATION CONTACT:

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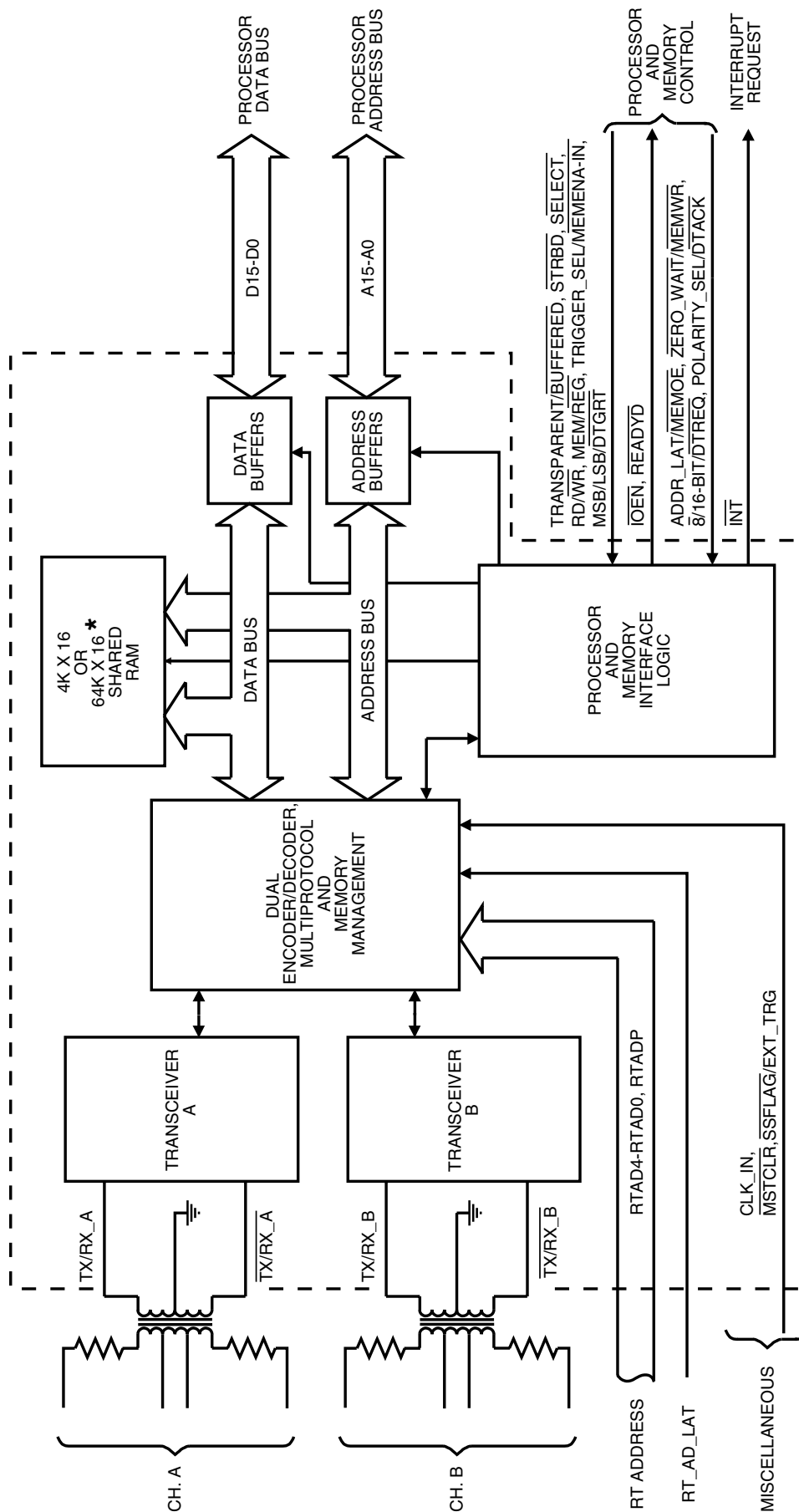


FIGURE 1. BU-65178/65179*/61588/61688*/61689*

TABLE 1. BU-65178/65179*/61588/61688*/61689* SPECIFICATIONS				
PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage				
■ Logic +5 V	-0.3		6.0	V
■ Transceiver +5 V (Note 12)	-0.3		7.0	V
Logic				
■ Voltage Input Range	-0.3		V _{CC} +0.3	V
RECEIVER				
Differential Input Resistance (Notes 1-7)	2.5			kohm
Differential Input Capacitance (Notes 1-7)			5	pF
Threshold Voltage, Transformer Coupled, Measured on Stub	0.20		0.860	V _{p-p}
Common Mode Voltage (Note 7)	0		10	V _{peak}
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	V _{p-p}
■ Transformer Coupled Across 70 Ω, Measured on Bus:				
• Standard Product = – XX0	18	21	27	V _{p-p}
• 1760 Amplitude Compliant Product = – XX2 (Note 13 and Ordering Information – Test Criteria)	20	22	27	V _{p-p}
Output Noise, Differential (Direct Coupled)			10	mV _{p-p} , diff
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250	150	250	mV
Rise/Fall Time	100		300	nsec
LOGIC				
V _{IH}	2.0			V
V _{IL}			0.8	V
I _{IH} (V _{CC} = 5.5 V, V _{IN} = V _{CC})	-10		10	μA
I _{IH} (V _{CC} = 5.5 V, V _{IN} = 2.7 V)				
■ SSFLAG/EXT_TRIG	-692		-84	μA
■ All Other Inputs	-346		-42	μA
I _{IL} (V _{CC} = 5.5 V, V _{IN} = 0.4 V)				
■ SSFLAG/EXT_TRIG	-794		-100	μA
■ All Other Inputs	-397		-50	μA
V _{OH} (V _{CC} = 4.5 V, V _{IH} = 2.7 V, V _{IL} = 0.2 V, I _{OH} = max)	2.4			V
V _{OL} (V _{CC} = 4.5 V, V _{IH} = 2.7 V, V _{IL} = 0.2 V, I _{OL} = max)			0.4	V
I _{OL}				
■ DB15-DB0	6.4			mA
■ A15-A0 MEMOE/ADDR_LAT MEMWR/ZEROWAIT DTREQ/16/8 DTACK/POLARITY_SEL				
■ INT READYD IOEN	3.2			mA
I _{OH}				
■ DB15-DB0			-6.4	mA
■ A15-A0 MEMOE/ADDR_LAT MEMWR/ZEROWAIT DTREQ/16/8 DTACK/POLARITY_SEL				
■ INT READYD IOEN			-3.2	mA
C _I (Input Capacitance)			50	pF
C _{IO} (Bi-directional signal input capacitance)			50	pF

TABLE 1. BU-65178/65179*/61588/61688*/61689* SPECIFICATIONS (CONT.)				
PARAMETER	MIN	TYP	MAX	UNITS
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)- to-Start of Next Message		2.5		μs
BC Intermesssage Gap (Note 8)		9.5		μs
BC/RT/MT Response Timeout (Note 9)				
■ 18.5 nominal	17.5	18.5	19.5	μs
■ 22.5 nominal	21.5	22.5	23.5	μs
■ 50.5 nominal	49.5	50.5	51.5	μs
■ 128.0 nominal	127	129.5	131	μs
T Response Time (Note 11)	4		7	μs
Transmitter Watchdog Timeout		668		μs
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ BU-65178/61588X3				
• +5 V (Logic)	4.5	5.0	5.5	V
• +5 V (Ch. A, Ch. B)	4.75	5.0	5.25	V
Current Drain (Total Hybrid)				
■ BU-65178/65179/61588X0				
• +5 V (Logic)		23	100	mA
■ BU-65178/65179/61588X3				
• +5 V (Logic, Ch. A, Ch. B)				
• Idle		116	160	mA
• 25% Transmitter Duty Cycle		222	265	mA
• 50% Transmitter Duty Cycle		328	370	mA
• 100% Transmitter Duty Cycle		540	580	mA
■ BU-61688*/61689X0*				
• +5 V (Logic)		46	200	mA
■ BU-61688*/61689X3*				
• +5 V (Logic, Ch. A, Ch. B)				
• Idle		116	180	mA
• 25% Transmitter Duty Cycle		217	285	mA
• 50% Transmitter Duty Cycle		318	390	mA
• 100% Transmitter Duty Cycle		519	600	mA
POWER DISSIPATION				
Total Hybrid				
■ BU-65178/65179/61588X0				
• +5 V (Logic)		0.115	0.5	W
■ BU-65178/61588/65179X3				
• Idle		0.64	0.88	W
• 25% Duty Cycle		0.93	1.11	W
• 50% Duty Cycle		1.22	1.33	W
• 100% Duty Cycle		1.81	1.97	W
■ BU-61688*/61689X0*				
• +5 V (Logic)		0.230	1.0	W
■ BU-61688*/61689X3*				
• Idle		0.64	0.99	W
• 25% Duty Cycle		0.93	1.22	W
• 50% Duty Cycle		1.22	1.45	W
• 100% Duty Cycle		1.80	1.90	W
Hottest Die				
■ BU-65178/61588X3/65179X3*/ BU-61688*/61689X3*				
• Idle		0.18	0.28	W
• 25% Duty Cycle		0.42	0.51	W
• 50% Duty Cycle		0.66	0.75	W
• 100% Duty Cycle		1.14	1.22	W

* Mini-ACE PLUS with 64K Words of RAM. RAM impact to Power Supply is based on Host Processor activity; subtract 140 mA if Host is idle.

TABLE 1. BU-65178/65179*/61588/61688*/61689* SPECIFICATIONS (CONT.)				
PARAMETER	MIN	TYP	MAX	UNITS
Frequency				
■ BU-61588/61688*/65178				
• Default Mode		16		MHz
• Software Programmable Option		12		MHz
■ BU-61689*				
• Default Mode		20		MHz
• Software Programmable Option		10		MHz
■ BU-65179*				
• Pin Programmable Option		10/12/16/20		MHz
Long Term Tolerance				
• 1553A Mode			0.01	%
• 1553B Mode			0.1	%
Short Term Tolerance, 1 second				
• 1553A Mode			0.001	%
• 1553B Mode			0.01	%
Duty Cycle				
• 16 MHz	33		67	%
• 12 MHz	40		60	%
• 10 MHz*	40		60	%
• 20 MHz	40		60	%
THERMAL				
Thermal Resistance, Junction-to-Case, Hottest Die (θJC)			6.8	°C/W
■ BU-65178/61588X3*			150	°C
Operating Junction Temperature	-55		150	°C
Storage Temperature	-65		150	°C
Lead Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
Size				
■ BU-65178/61588 P			1.0 X 1.0 X 0.150	in.
BU-65179*/61688*/61689*			(25.4 x 25.4 x 3.81)	(mm)
■ BU-65178/61588 F/G			1.0 X 1.0 X 0.155	in.
BU-65179*/61688*/61689*			(25.4 x 25.4 x 3.94)	(mm)
Weight				
■ BU-65178/61588 F/P/G			0.3	oz
BU-65179*/61688*/61689*			(9)	(g)

Table 1 Notes (Cont.):

- (8) Typical value for minimum intermessage gap time. Under software control, may be lengthened to (65,535 μs minus message time), in increments of 1 μs.
- (9) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).
- (10) For both +5 V logic and transceiver. +5 V for channels A and B.
- (11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
- (12) External 10 μF Tantalum and 0.1 μF capacitors should be located as close as possible to Pins 20 and 72 on the Flat Package and Pins A9 and J3 on the PGA package, and 0.1 μF at Pin 37/D3.
- (13) MIL-STD-1760 requires that the Mini-ACE produce a 20 Vp-p minimum output on the stub connection.

Notes: Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

- (1) Specifications include both transmitter and receiver (tied together internally).
- (2) Measurement of impedance is directly between pins TX/RX A(B) and TX/RX A(B) of the BU-65178/61588X3 hybrid.
- (3) Assuming the connection of all power and ground inputs to the hybrid.
- (4) The specifications are applicable for both unpowered and powered conditions.
- (5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
- (6) Minimum resistance and maximum capacitance parameters are guaranteed, but not tested, over the operating range.
- (7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), referenced to hybrid ground. Use a DDC recommended transformer or other transformer that provides an equivalent CMRR.

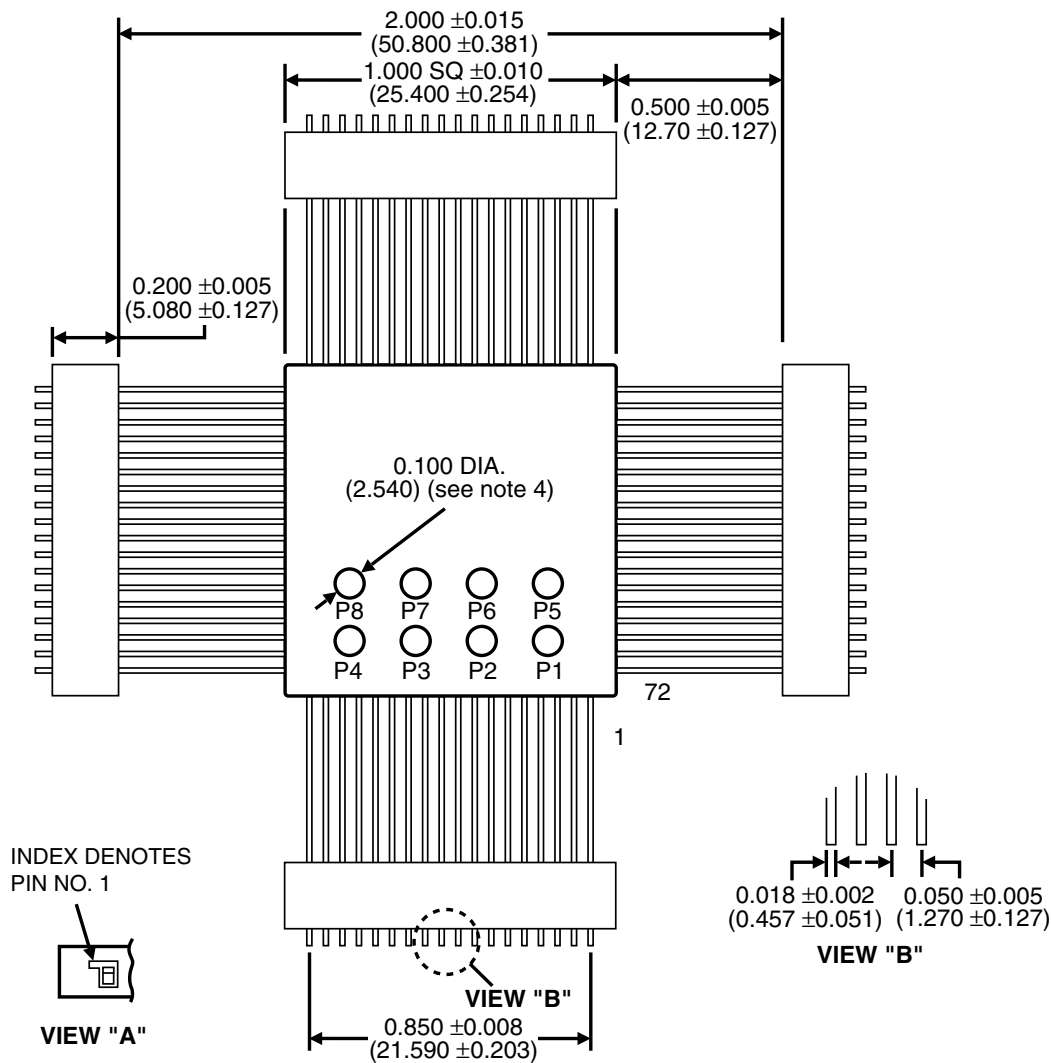
TABLE 2. BU-65178/65179*/61588/61688*/61689* PIN LISTINGS (QFP QUAD FLAT PACK, PGA-PIN GRID ARRAY AND GULL LEAD)

QFP	PGA	NAME	QFP	PGA	NAME
1	B4	MEM/REG	42	H9	D00
2	B5	MSTCLR	43	F9	D02
3	C2	A11	44	F7	D03
4	C3	A10	45	G5	D05
5	C1	TX/RX-A	46	E7	D08
6	D2	A08	47	E9	D07
7	D1	TX/RX-A	48	D7	D13
8	C4	A14, See NOTE 1	49	B2	D12
9	E3	A04	50	D9	D14
10	F2	A03	51	B9	D09
11	E1	A07	52	A2	D11
12	F3	A02	53	D8	D15
13	G1	TX/RX-B	54	A1	D10
14	G4	MEMOE/ADDR_LAT	55	C9	TRANSPARENT/ BUFFERED
15	G3	A00	56	B8	READYD
16	H1	TX/RX-B	57	C8	INT
17	A7	LOGIC GND	58	A3	IOEN
18	A8	LOGIC GND	59	B7	TX_INH_A
19	J8	LOGIC GND	60	C7	TX_INH_B
20	A9	+5V VCC2	61	C6	SELECT
21	J7	RTAD2	62	A6	STRBD
22	F1	A06	63	A5	RD/WR
23	J2	MEMWR/ ZEROWAIT	64	J1	DTGRT/MSB/LSB
24	H5	DTREQ/16/8	65	A4	Test Output (RX-A)
25	H3	Test Output (RX-B)	66	C5	A15, See NOTE 1
26	H4	Test Output (RX-B)	67	B6	Test Output (RX-A)
27	G2	A01	68	E2	A05
28	J5	MEMENA_IN/ TRIGGER_SEL	69	J4	A09
29	J6	DTACK/ POLARITY_SEL	70	B3	A12, See NOTE 2
30	H6	CLOCK_IN	71	B1	A13, See NOTE 3
31	G7	RT_AD_LAT	72	J3	+5V VCC1
32	H2	SSFLAG/EXT_TRIG	**	D4	TestOutput(A_RExt)
33	H7	RTAD0	**	D5	Test Output (A_Test1)
34	G8	RTAD3	**	D6	Test Output (AB_Test4)
35	H8	RTAD4	**	E4	TestOutput(B_RExt)
36	E8	D06	**	E6	TestOutput (AB_Tstck)
37	D3	+5V VCC	**	F4	TestOutput (AB_Test2)
38	F8	D01	**	F5	TestOutput (AB_Test3)
39	G6	D04	**	F6	TestOutput (B_Test1)
40	G9	RTADP	**	F6	TestOutput (B_Test1)
41	J9	RTAD1	N/A	E5	No Connect

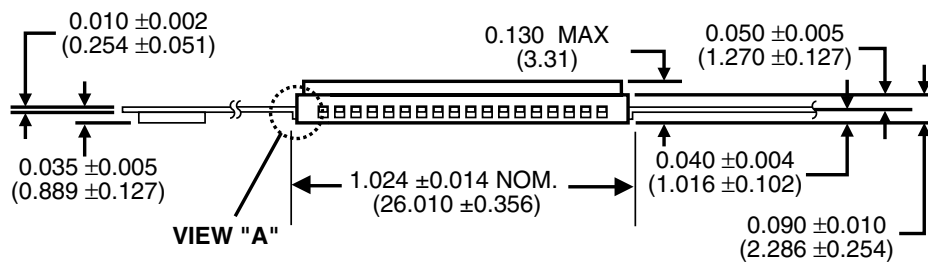
NOTES

** Note that the Test Output pins on the flat pack are pads located on the bottom of the package.

1. BU-65179*, A15/A14 pins are actually CLK SEL 1 / CLK SEL 0 respectively.
2. BU-65179*, A12 pin selects the RT_BOOT_L OPTIONAL MODE.
3. BU-65179*, A13 pin has no connection.



BOTTOM VIEW



SIDE VIEW

Notes:

- 1) Dimensions are in inches (mm).
- 2) Package Material: Alumina (Al_2O_3)
- 3) Lead Material: Kovar, Plated by 50 μ in. minimum nickel under 60 μ in. minimum gold.
- 4) There are 8 test pads located on the bottom of the package. These pads are recessed so as not to interfere when mounting the hybrid.

FIGURE 2. BU-65178F / 65179F* / 61588F / 61688F* / 61689F* MECHANICAL OUTLINE (QUAD FLAT PACK - QFP)

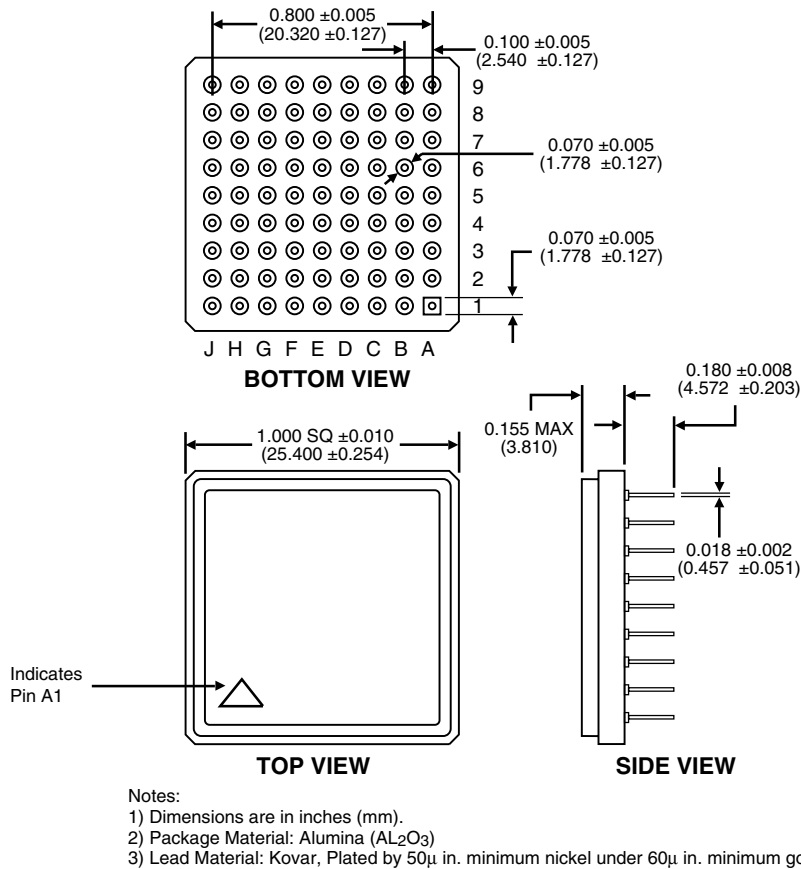


FIGURE 3. BU-65178P / 65179P* / 61588P / 61688P* / 61689P* MECHANICAL OUTLINE (PIN GRID ARRAY - PGA)

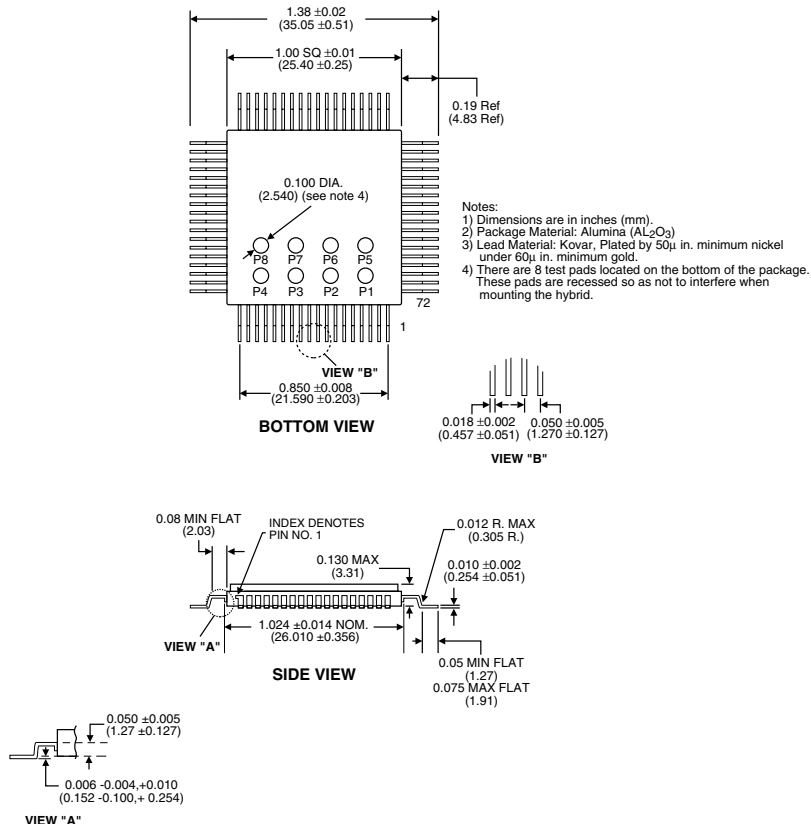


FIGURE 4. BU-65178G / 65179G* / 61588G / 61688G* / 61689G* MECHANICAL OUTLINE (GULL LEAD)

TRANSFORMERS

In selecting isolation transformers to be used with the Mini-ACE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 μ H, and is measured as follows:

The side of the transformer that connects to the Mini-ACE is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding.

This inductance must be less than 6.0 μ H. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0 μ H.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 μ H.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 3 provides a listing of many of these transformers. For further information, contact BTTC at 631-244-7393 or at www.bttec-beta.com.

TABLE 3. BTTC TRANSFORMERS FOR USE WITH MINI-ACE

TRANSFORMER CONFIGURATION	BTTC PART NO.
Single epoxy transformer, through-hole, 0.625" X 0.625", 0.250" max height	B-3067 B-3226
Single epoxy transformer, through-hole, 0.625" X 0.625", 0.220" max height.	B-3818
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.275" max height	B-3231
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.275" max height	B-3227
Single epoxy transformer, surface mount, hi-temp solder, 0.625" X 0.625", 0.220" max height.	B-3819
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.150" max height	LPB-5014
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.150" max height	LPB-5015
Single epoxy transformer, through hole, transformer coupled only, 0.500" X 0.350", 0.250" max height	B-3229
Dual epoxy transformer, twin stacked, 0.625" X 0.625", 0.280" max height	TST-9007
Dual epoxy transformer, twin stacked, surface mount, 0.625" X 0.625", 0.280" max height	TST-9017
Dual epoxy transformer, twin stacked, flat pack, 0.625" X 0.625", 0.280" max height	TST-9027
Dual epoxy transformer, side by side, through-hole, 0.930" X 0.630", 0.155" max height	TLP-1205
Dual epoxy transformer, side by side, flat pack, 0.930" X 0.630", 0.155" max height	TLP-1105
Dual epoxy transformer, side by side, surface mount, 0.930" X 0.630", 0.155" max height	TLP-1005
Dual epoxy transformer, side by side, surface mount, 1.410" X 0.750", 0.130" max height	DLP-7115 (see note1)
Single metal transformer, hermetically sealed, flat pack, 0.630" X 0.630", 0.175" max height	HLP-6014
Single metal transformer, hermetically sealed, surface mount, 0.630" X 0.630", 0.175" max height	HLP-6015
NOT RECOMMENDED	DLP-7014 SLP-8007 SLP-8024

Notes:

1. DLP-7115 operates to +85°C max. All other transformers listed operate to +130°C max.

INTERFACE TO MIL-STD-1553 BUS

FIGURE 5 illustrates the interface between the various versions of the Mini-ACE and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well

as the nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

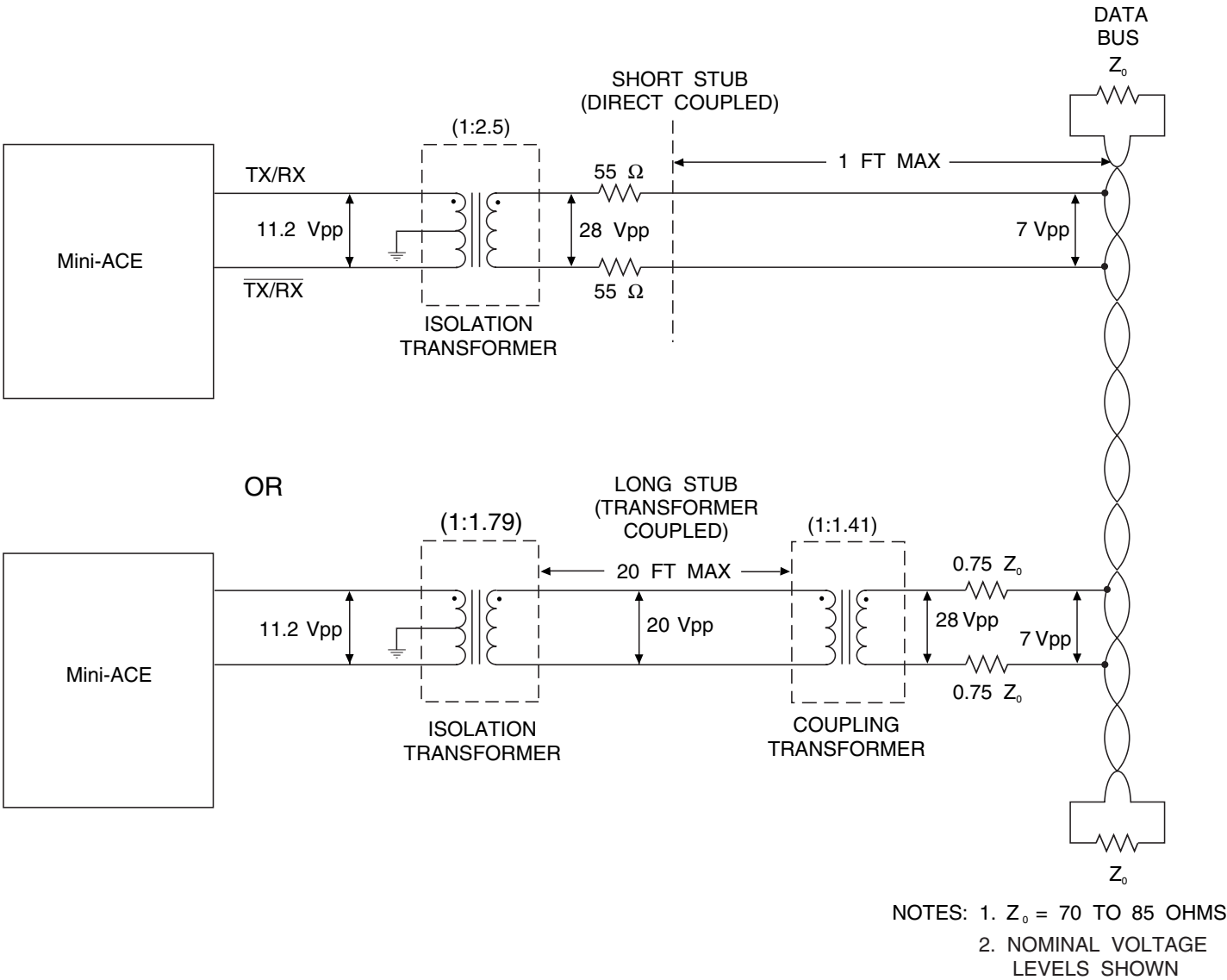


FIGURE 5. MINIATURE ADVANCED COMMUNICATIONS ENGINE INTERFACE TO MIL-STD-1553 BUS

ORDERING INFORMATION

BU-61588F3-11XX

Supplemental Process Requirements:

S = Pre-Cap Source Inspection
L = Pull Test
Q = Pull Test and Pre-Cap Source Inspection
K = One Lot Date Code
W = One Lot Date Code and Pre-Cap Source Inspection
Y = One Lot Date Code and 100% Pull Test
Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
Blank = None of the Above

Test Criteria:

0 = Standard Testing
2 = MIL-STD-1760 Amplitude Compliant - Applies to +5 Volt Transceiver Option Only

Process Requirements:

0 = Standard DDC processing, no Burn-In (See table on next page)
1 = MIL-PRF-38534 Compliant
2 = B*
3 = MIL-PRF-38534 Compliant with PIND Testing
4 = MIL-PRF-38534 Compliant with Solder Dip
5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
6 = B* with PIND Testing
7 = B* with Solder Dip
8 = B* with PIND Testing and Solder Dip
9 = Standard DDC Processing with Solder Dip, no Burn-In (See table on next page)

Temperature Range/Data Requirements:

1 = -55°C to +125°C
2 = -40°C to +85°C
3 = 0°C to +70°C
4 = -55°C to +125°C with Variables Test Data
5 = -40°C to +85°C with Variables Test Data
8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:

0 = No Transceivers
3 = +5 Volts, rise/fall times=100 to 300 ns (-1553B) (See **Test Criteria** - 1760 Compliant with option -XX2)

Package Type:

F = 72-Pin Quad Flat Pack
P = 81-Pin PGA
G = 72-Pin Gull Lead (Contact factory.)

Product Type:

65178 = RT Only, 16/12 MHz, 4K RAM
61588 = BC/RT/MT, 16/12 MHz, 4K RAM
65179 = RT/RT_BOOT, 10/12/16/20 MHz, 4K RAM
61688 = BC/RT/MT, 12/16 MHz, 64K RAM
61689 = BC/RT/MT, 10/20 MHz, 64K RAM

*Standard DDC Processing with burn-in and full temperature test, see table on next page.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:

1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.

2. When applicable.

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Specifications are subject to change without notice.

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Germany - Tel: +49-(0)89-15 00 12-11, Fax: +49-(0)89-15 00 12-22

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