MHS

data sheet

T-46-23-10

HM 65789

16K x 4
HIGH SPEED CMOS SRAM

OCTOBER 1987

Features

- **FAST ACCESS TIME : 25/35/45 ns max**
- **STANDBY CURRENT : 15 mA max**
- **OPERATING CURRENT : 100 mA**
- **ASYNCHRONOUS INPUTS**
- **OUTPUT ENABLE FEATURE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SINGLE 5 VOLT SUPPLY**
- **300 MILS WIDTH PACKAGE**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE**
- **WIDE TEMPERATURE RANGE : – 55°C TO + 125°C**

Description

The HM 65789 is a high speed CMOS static RAM organised as 16384 x 4 bits. It is manufactured using MHS's high performance, CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 550 mW.

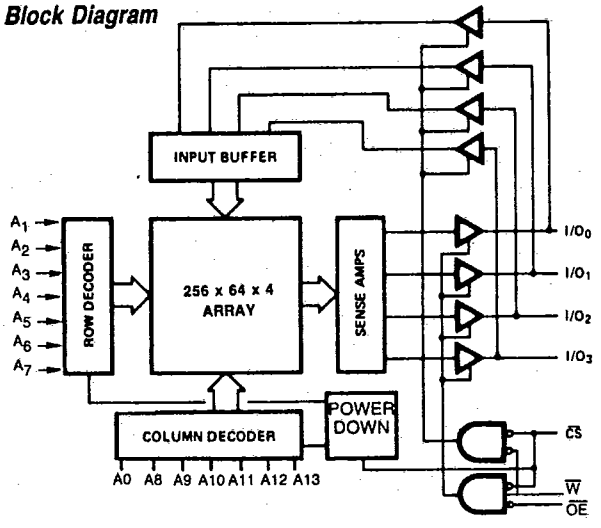
The HM 65789 features fully static operation requiring no external clocks or timing strobes, additionally the automatic power-down feature reduces the power consumption by 60 % when deselected. Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

All inputs and outputs of the HM 65789 are TTL compatible and operate from a single 5V supply thus simplifying system design.

The HM 65789 is packaged in a plastic/ceramic 300 mils 24 pins DIL, SO 24 pins DIL or a 28 pins Leadless Chip Carrier allowing high board-level packing densities.

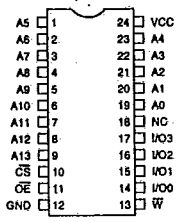
The HM 65789 is 100 % processed following the test methods of MIL STD 883C.

Block Diagram

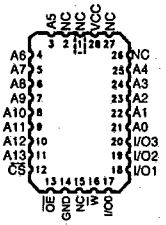


Pinouts (TOP VIEW)

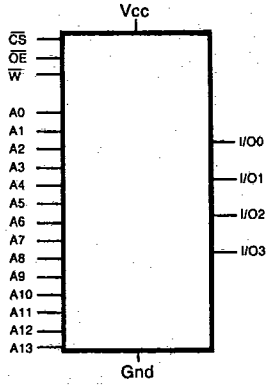
DIL (24 PINS)



LCC (28 PINS)



Logic Symbol



PIN NAMES

A0-A13	: Address inputs	$\overline{OE}$	: Output enable
I/O	: Input/Output	Gnd	: Ground
$\overline{CS}$	: Chip select	$\overline{W}$	: Write enable
Vcc	: Power		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	Din	Dout	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	H	H	Valid	Z	Deselect

L = Low, H = High, X = H or L

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• ABSOLUTE MAXIMUM RATINGS	• OPERATING RANGE		
		Operating Voltage	Operating Temperature
Supply voltage (VCC-GND) — 0.5 V to + 7 V DC input or output voltage : – 3.0 to 7.0V DC output voltage in high Z state : – 0.5V to 7.0V Storage temperature : – 65° C to + 150° C Output current into outputs (low) : 20 mA	Military - 2	VCC ± 10 %	– 55° C to + 125° C
	Commercial - 5	VCC ± 10 %	– 0° C to + 70° C

Electro Static Discharge Voltage > 2000V
(per MIL STD 883C, Method 3015.2)

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

Symbol	Parameter	65788H-5 65789H-5	65788K-5 65789K-5 65788M-5 65789M-5 65788N-5 65789N-5	65788K-2 65789K-2 65788M-2 65789M-2 65788N-2 65789N-2	Unit	Value
ICCSB1 (1)	Stand by supply current	40	40	40	mA	max
ICCSB2 (2)	Stand by supply current	15	15	20	mA	max
ICCOP (3)	Average operating supply current	100	100	110	mA	max
IIX (4)	Input leakage current	± 10	± 10	± 10	µA	max
IOZ (4)	Output leakage current	± 10	± 10	± 10	µA	max
VIL (5)	Input low voltage	0.8	0.8	0.8	V	max
VIH (5)	Input high voltage	2.2	2.2	2.2	V	min
VOL (6)	Output low voltage	0.4	0.4	0.4	V	max
VOH (6)	Output high voltage	2.4	2.4	2.4	V	min
I OS (7)	Output short circuit current	– 350	– 350	- 350	mA	max
C IN (8)	Input capacitance	5	5	5	PF	max
C OUT (8)	Output capacitance	7	7	7	PF	max

Note 1 : $\overline{CS} \geqslant$ VIH. Min Duty Cycle = 100 %
Note 2 : $\overline{CS} \geqslant$ VCC – 0.3V VIN $\geqslant$ VCC – 0.3V or VIN $\leqslant$ 0.3V
Notes 1 & 2 : A pull up resistor to VCC on the $\overline{CS}$ input is required to keep the device deselected during VCC power up, otherwise ICCSB will exceed values given.
Note 3 : VCC max, Iout = 0 mA
Note 4 : GND $\leqslant$ VI $\leqslant$ VCC, GND $\leqslant$ VO $\leqslant$ VCC Output disabled
Note 5 : VIL min = – 3.0V, VIH max = VCC
Note 6 : VCC min, IOH = – 4 mA, IOL = 8.0 mA
Note 7 : VCC = max, Vout = GND, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time
Note 8 : This parameter is sampled and not 100 % tested. TA = 25°C, F = 1 MHz, VCC = 5.0V

AC PARAMETERS

Conditions
- Input pulse levels: GND to 3.0 V
- Input rise time: 5 ns
- Input timing reference levels: 1.5 V
- Output loading IOL/IOH (see fig. 1a and 1b): + 30 pF

Read cycle

Parameter	Description	65788H-5 65789H-5	65788K-5 65788K-2 65789K-5 65789K-2	65788M-5 65788M-2 65789M-5 65789M-2	65788N-5 65788N-2 65789N-5 65789N-2	Unit	Value
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address to data valid	25	35	45	55	ns	max
TAVQX	Data hold from address change	3	3	5	5	ns	min
TELQV	$\overline{CS}$ low to data valid	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z (10)	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z (9, 10)	15	15	15	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICCL	$\overline{CS}$ high to power down	25	25	30	35	ns	max
TGLQV	$\overline{OE}$ low to data valid (65789)	15	25	30	35	ns	max
TGLQX	$\overline{OE}$ low to low Z (65789)	0	0	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z (65789)	15	15	15	20	ns	max

Write cycle (11)

Parameter	Description	65788H-5 65789H-5	65788K-5 65788K-2 65789K-5 65789K-2	65788M-5 65788M-2 65789M-5 65789M-2	65788N-5 65788N-2 65789N-5 65789N-2	Unit	Value
TAVAV	Write cycle time	20	30	40	50	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	35	45	ns	min
TAVWH	Address set up to write end	20	30	35	45	ns	min
TWHAX	Address hold from write end	0	0	0	0	ns	min
TAVWL	Address set up to write start	0	0	0	0	ns	min
TWLWH	$\overline{W}$ pulse width	20	30	35	45	ns	min
TDVWH	Data set up to write end	10	15	20	25	ns	min
TWHDX	Data hold from write end	0	0	5	5	ns	min
TWLQZ	$\overline{W}$ Low to high Z (9, 10)	10	15	15	20	ns	max
TWHQX	$\overline{W}$ high to low Z (10)	5	5	8	8	ns	min

Note 9 : TEHQZ, TWLQZ are tested with CL = 5 pF as in figure 1b. Transition is measured ± 500 mV from steady state voltage.
Note 10 : At any given temperature and voltage condition, TQZ is less than TQX for all devices.
These parameters are sampled and not 100 % tested.
Note 11 : Data input set up and hold timing should be referenced to the using edge of the signal that terminates the write.

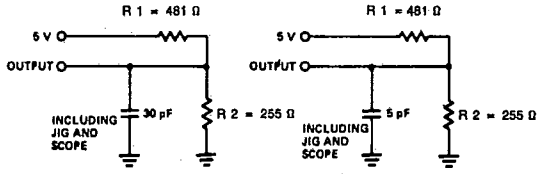


Figure 1a

Figure 1b

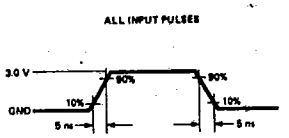
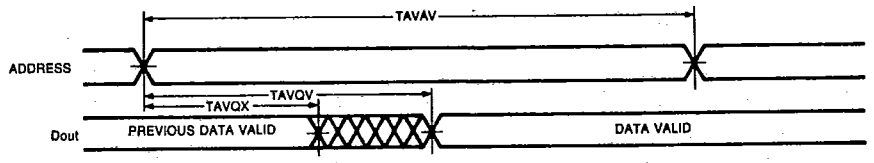


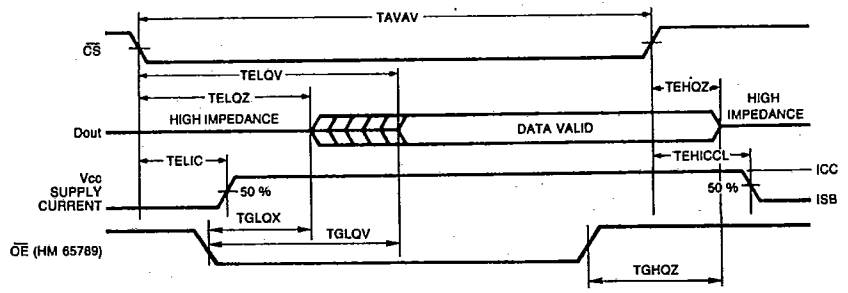
Figure 2

SWITCHING WAVEFORMS

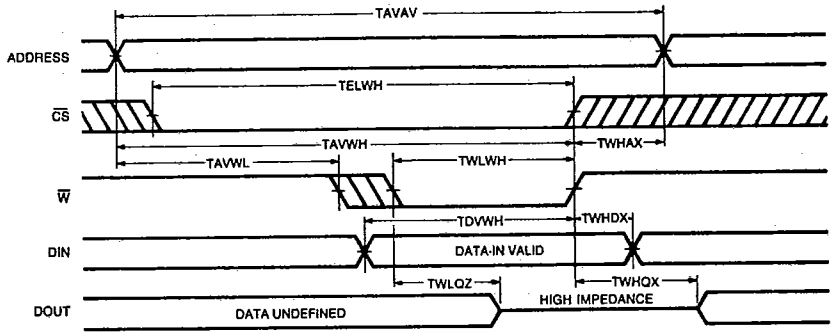
READ CYCLE No. 1 (Notes 12, 13)



READ CYCLE No. 2 (Notes 12, 14)



WRITE CYCLE No. 1 ($\overline{W}$ Controlled) (Notes 11,15)



Note 12 : $\overline{W}$ is high for read cycle
Note 13 : Device is continuously selected, $\overline{CS}$ = VIL (HM 65789 $\overline{OE}$ = VIL also)
Note 14 : Address valid prior to or concident with $\overline{CS}$ transition low
Note 15 : HM 65789 only : Data I/O will be high impedance if $\overline{OE}$ = VIH

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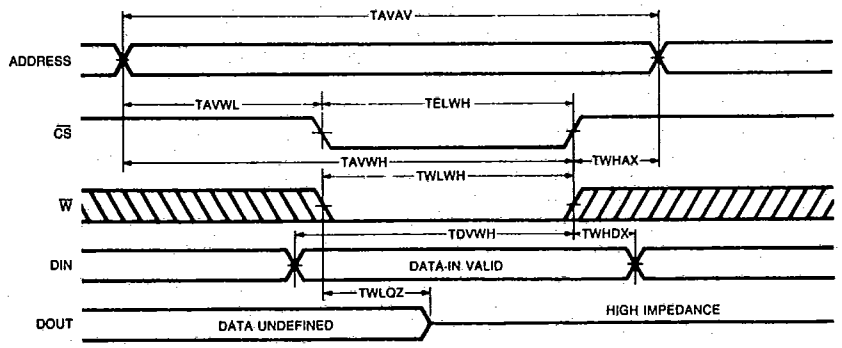
WRITE CYCLE No. 2 ($\overline{CS}$ Controlled) (Notes 11, 15)



Note : If $\overline{CS}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.

Ordering information

DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1-65788 ( )-5/HM1-65789 ( )-5	CERAMIC DIL	0°C to + 70°C
HM1-65788 ( )-2/HM1-65789 ( )-2	CERAMIC DIL	– 55°C to + 125°C
HM1-65788 ( )-8/HM1-65789 ( )-8	CERAMIC DIL	– 55°C to + 125°C
HMT-65788 ( )-5/HMT-65789 ( )-5	SO PLASTIC DIL	0°C to + 70°C
HM3-65788 ( )-5/HMT-65789 ( )-5	PLASTIC DIL	0°C to + 70°C
HM4-65788 ( )-5/HM4-65789 ( )-5	LCC 22/28 PIN	0°C to + 70°C
HM4-65788 ( )-2/HM4-65789 ( )-2	LCC 22/28 PIN	– 55°C to + 125°C
HM4-65788 ( )-8/HM4-65789 ( )-8	LCC 22/28 PIN	– 55°C to 125°C

TEMPERATURE RANGE (– 2, – 5, – 8)

PERFORMANCE :
- H : 25 ns (commercial only)
- K : 35 ns
- M : 45 ns
- N : 55 ns

DEVICE TITLE

PACKAGE (1, 3, 4, T)
- 1 : CERAMIC
- 3 : PLASTIC
- 4 : LCC
- T : SO