

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62308BP-1, TD62308BF

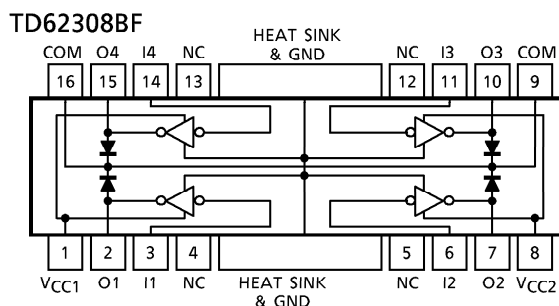
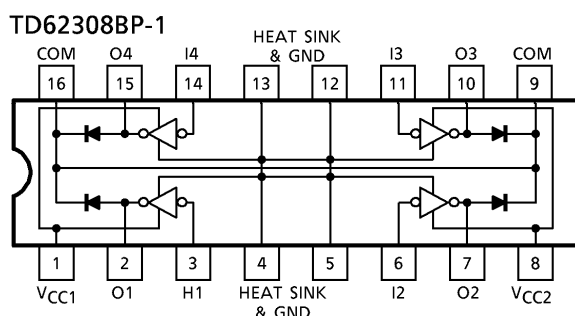
4ch LOW INPUT ACTIVE HIGE-CURRENT DARLINGTON SINK DRIVER

The TD62308BP-1 and TD62308BF are non-inverting transistor array which are comprised of four NPN darlington output stages and PNP input stages. This device is low level input active driver and are suitable for operation with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers. Applications include relay, hammer, lamp and stepping motor drivers.

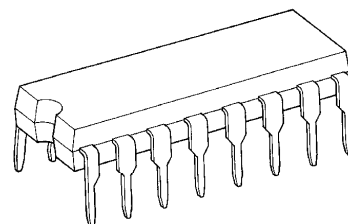
FEATURES

- Two V_{CC} Terminals V_{CC1} , V_{CC2} (Separated)
- Package Type BP-1 : DIP-16pin
BF : PFP-16pin
- High Sustaining Voltage Output : $V_{CE(SUS)} = 80V$ (Min.)
- Output Current (Single Output) : $I_{OUT} = 1.5A$ (Max.)
- Output Clamp Diodes
- Low Level Active Input
- GND and SUB Terminal = Heat Sink
- Input Compatible with TTL and 5V CMOS
- Standard Supply Voltage

PIN CONNECTION (TOP VIEW)

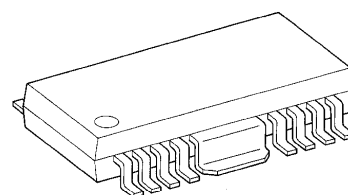


TD62308BP-1



DIP16-P-300-2.54A

TD62308BF

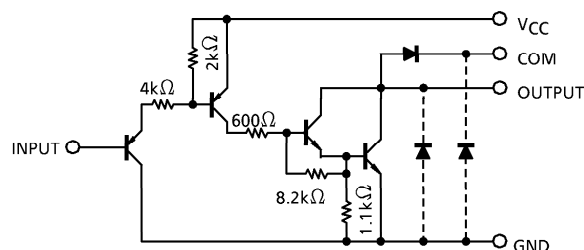


HSOP16-P-300-1.00

Weight

DIP16-P-300-2.54A : 1.11g (Typ.)
HSOP16-P-300-1.00 : 0.50g (Typ.)

SCHEMATICS (EACH DRIVER)



(Note) The output parasitic diode cannot be used as clamp diode.

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	7	V
Output Sustaining Voltage	V _{CE(SUS)}	− 0.5~80	V
Parasitic Transistor Output Voltage	V _{CEF} (*1)	80	V
Output Current	I _{OUT}	1.5	A / ch
Input Current	I _{IN}	− 10	mA
Input Voltage	V _{IN}	7	V
Clamp Diode Reverse Voltage	V _R	80	V
Clamp Diode Forward Current	I _F	1.5	A
Power Dissipation	BP-1	P _D	W
	BF		
Operating Temperature	T _{opr}	− 40~85	°C
Storage Temperature	T _{stg}	− 55~150	°C

(*1) Parasitic Transistor (COMMON - GND - OUTPUT) Output Voltage

(*2) On Glass Epoxy PCB (50 × 50 × 1.6mm Cu 50%)

(*3) On Glass Epoxy PCB (60 × 30 × 1.6mm Cu 30%)

RECOMMENDED OPERATING CONDITIONS (Ta = − 40~85°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CC}	—	4.5	—	5.0	V
Output Sustaining Voltage	V _{CE(SUS)}	—	0	—	80	V
Output Current	I _{OUT}	DC 1 Circuit, Ta = 25°C	0	—	1.25	A / ch
		T _{pw} = 25ms				
		4 Circuits				
		T _j = 120°C				
		Ta = 85°C				
Input Voltage	V _{IN}	—	0	—	25	V
	Output On	V _{IN(ON)}	0	—	V _{CC} − 3.6	V
	Output Off	V _{IN(OFF)}	V _{CC} − 1.0	—	V _{CC}	
Clamp Diode Reverse Voltage	V _R	—	—	—	80	V
Clamp Diode Forward Current	I _F	—	—	—	1.25	A
Power Dissipation	BP-1	P _D	—	—	1.4	W
	BF				0.7	

(*1) On Glass Epoxy PCB (50 × 50 × 1.6mm Cu 50%)

(*2) On Glass Epoxy PCB (60 × 30 × 1.6mm Cu 30%)

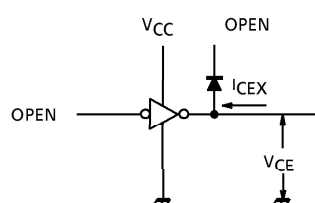
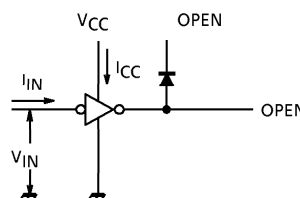
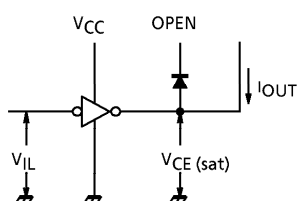
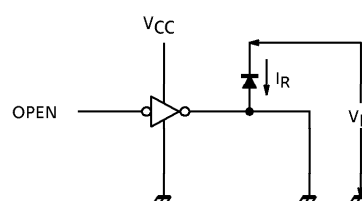
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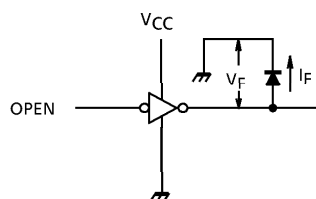
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V_{IH}	—	—	$V_{CC} - 1.6$	—	V_{CC}	V
	"L" level	V_{IL}	—	—	—	—	$V_{CC} - 3.6$	
Input Current	"H" level	I_{IH}	2	—	—	—	10	μA
	"L" level	I_{IL}	2	$V_{CC} = 5.5V, V_{IN} = 0.4V$	—	-0.05	-0.36	mA
Output Leakage Current		I_{CEX}	1	$V_{OUT} = 80V, Ta = 25^{\circ}C$	—	—	50	μA
				$V_{OUT} = 80V, Ta = 85^{\circ}C$	—	—	100	
Output Saturation Voltage		$V_{CE(sat)}$	3	$V_{CC} = 4.5V, I_{OUT} = 1.25A$	—	1.3	1.8	V
Clamp Diode Reverse Current		I_R	4	$V_R = 80V, Ta = 25^{\circ}C$	—	—	50	μA
Clamp Diode Forward Voltage		V_F	5	$I_F = 1.25A$	—	1.5	2.0	V
Supply Current	Output On	$I_{CC(ON)}$	2	$V_{CC} = 5.5V, V_{IN} = 0V$	—	8.5	12.5	mA / ch
	Output Off	$I_{CC(OFF)}$	2	$V_{CC} = 5.5V, V_{IN} = V_{CC}$	—	—	10	μA
Turn-On Delay		t_{ON}	6	$V_{OUT} = 80V, R_L = 68\Omega$	—	0.2	—	μs
Turn-Off Delay		t_{OFF}			—	5.0	—	
Parasitic Transistor Output Voltage		V_{CEF}	7	$I_{CEF} = 150mA$	80	—	—	V

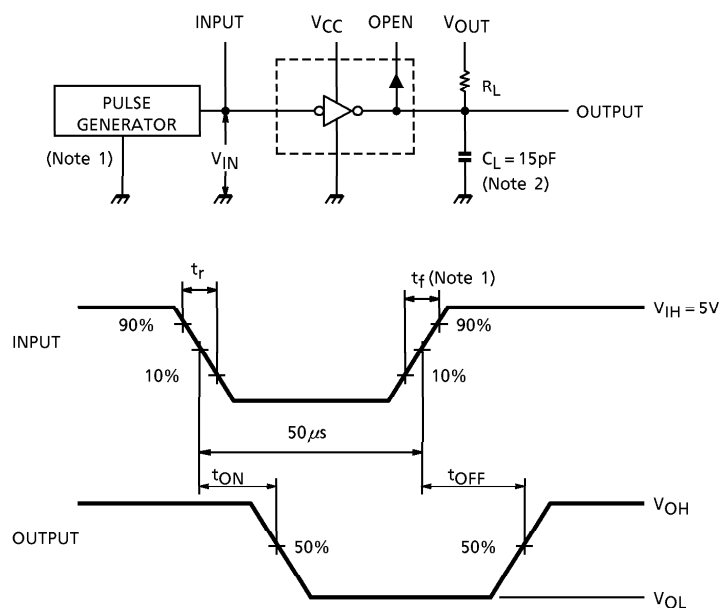
TEST CIRCUIT

1. I_{CEX} 2. I_{CC}, I_{IN} 3. $V_{CE(sat)}$ 4. I_R 

5. V_F



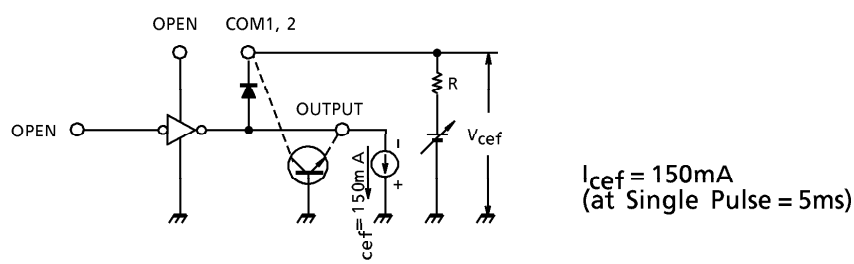
6. t_{ON} , t_{OFF}



(Note 1) Pulse Width $50\mu s$, Duty Cycle 10%、
Output Impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$

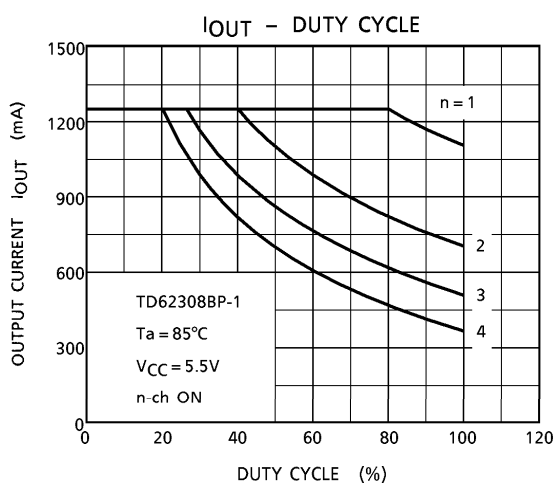
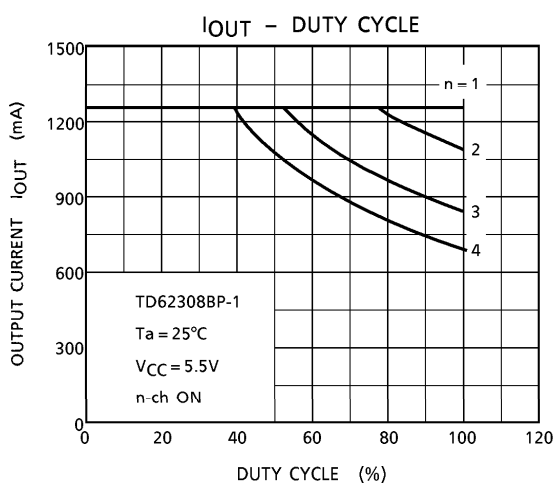
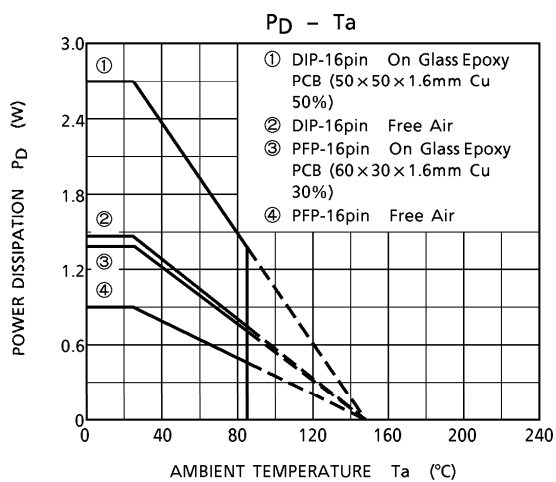
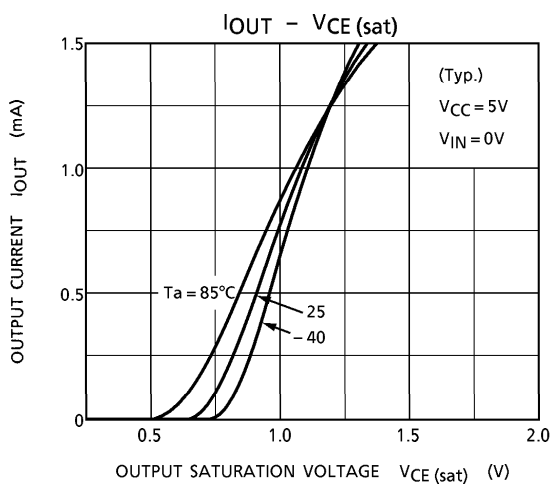
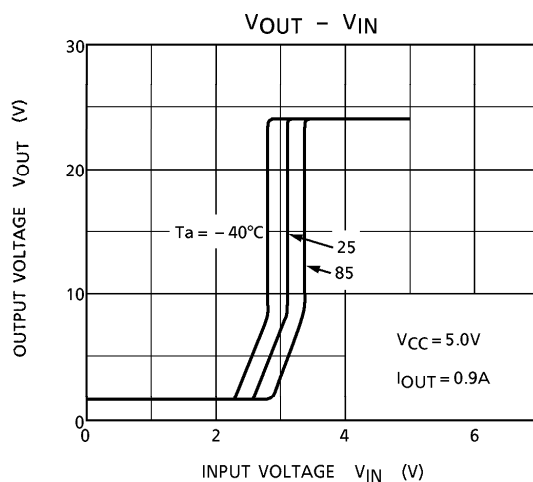
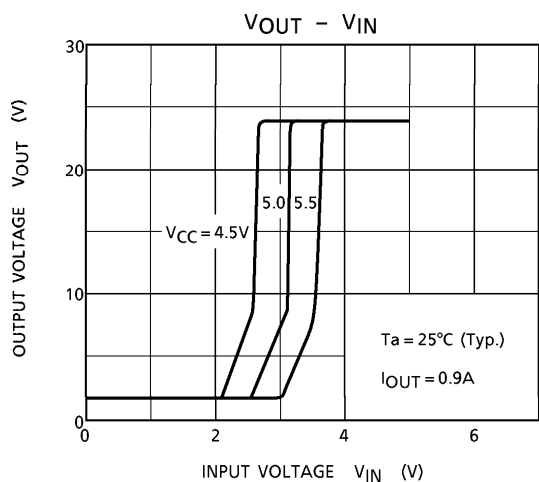
(Note 2) C_L includes probe and jig capacitance

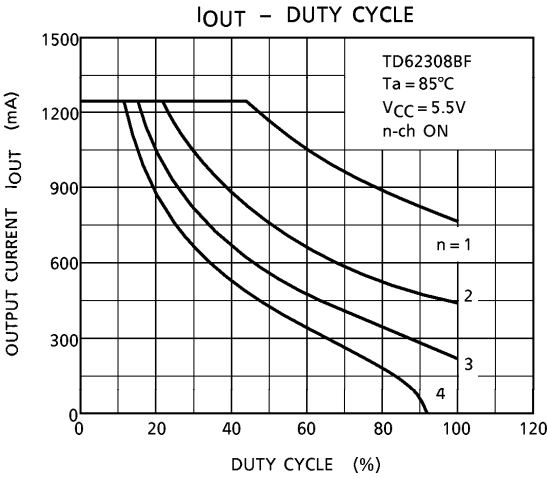
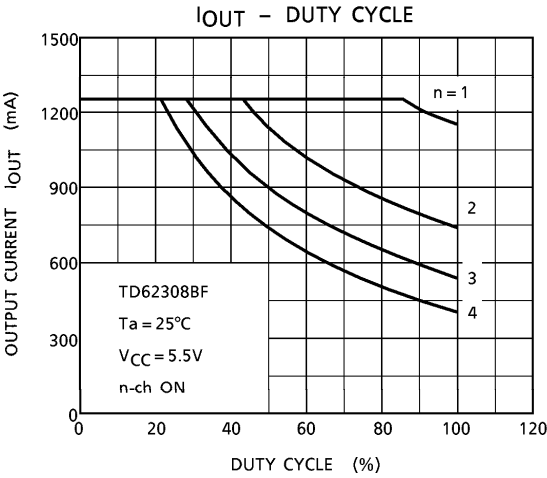
7. V_{cef}



PRECAUTIONS for USING

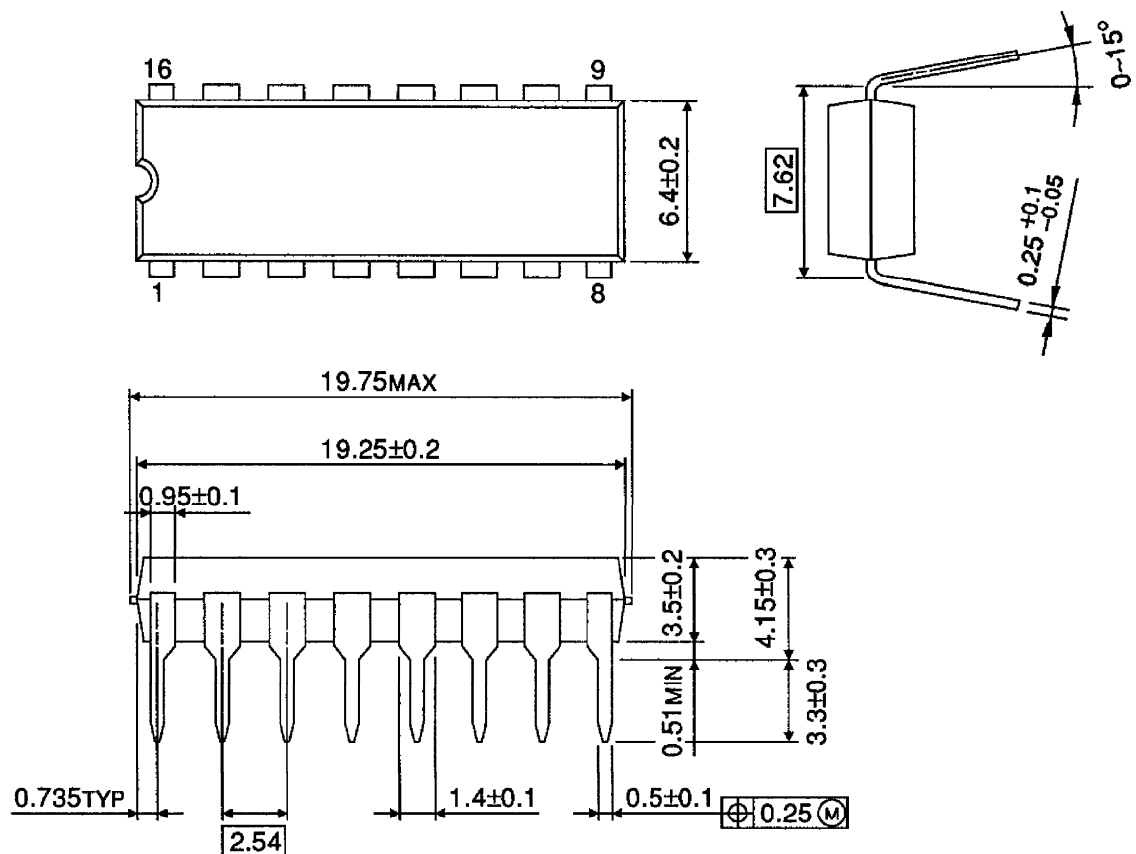
Utmost care is necessary in the design of the output line, V_{CC} , COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.





OUTLINE DRAWING
DIP16-P-300-2.54A

Unit : mm

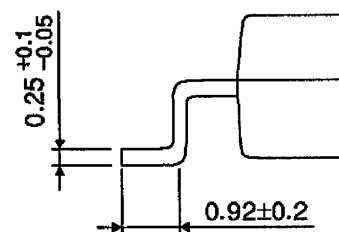
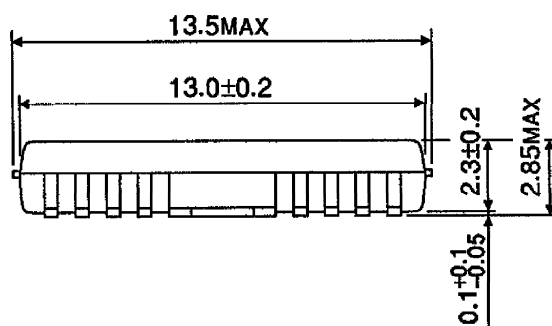
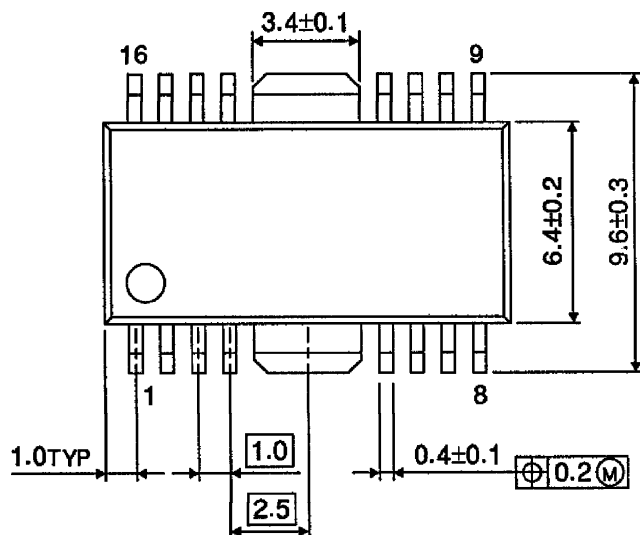


Weight : 1.11g (Typ.)

OUTLINE DRAWING

HSOP16-P-300-1.00

Unit : mm



Weight : 0.50g (Typ.)