

N-Channel Reduced Q_g , Fast Switching WFET™

PRODUCT SUMMARY

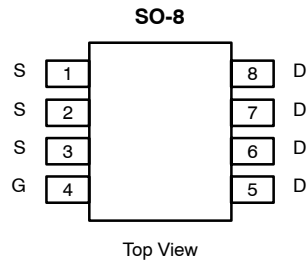
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0032 @ $V_{GS} = 10$ V	25
	0.0036 @ $V_{GS} = 4.5$ V	22

FEATURES

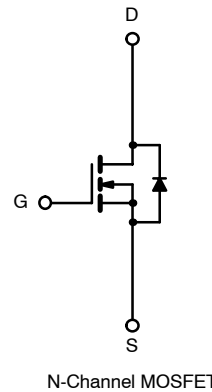
- Extremely Low Q_{gd} WFET Technology for Switching Losses Improvement
- TrenchFET® Gen II Power MOSFET
- 100% R_g Tested

APPLICATIONS

- Low-Side DC/DC Conversion
 - Notebook, Server, VRM Module
- Fixed Telecom



Ordering Information: Si4368DY—E3
Si4368DY-T1—E3 (Lead Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	25	17	A
	T _A = 70°C		20	13	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	70		
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.3	
Avalanch Current	L= 0.1 mH	i _{AS}	50		
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.5	1.6	W
	T _A = 70°C		2.2	1	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	29	35	$^\circ\text{C/W}$
	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	16	

Notes

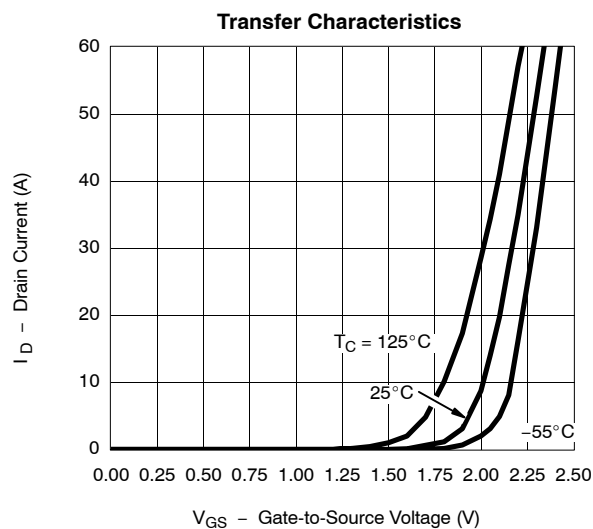
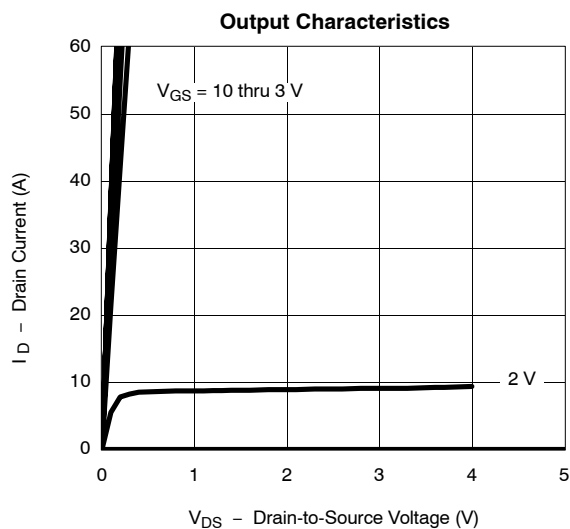
a. Surface Mounted on 1" x 1" FR4 Board.

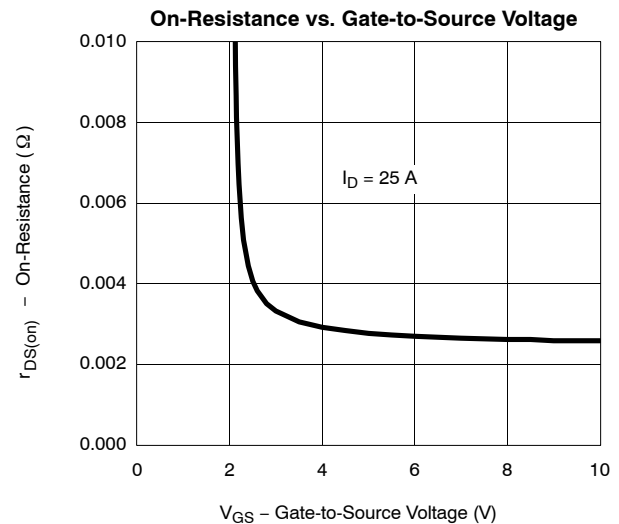
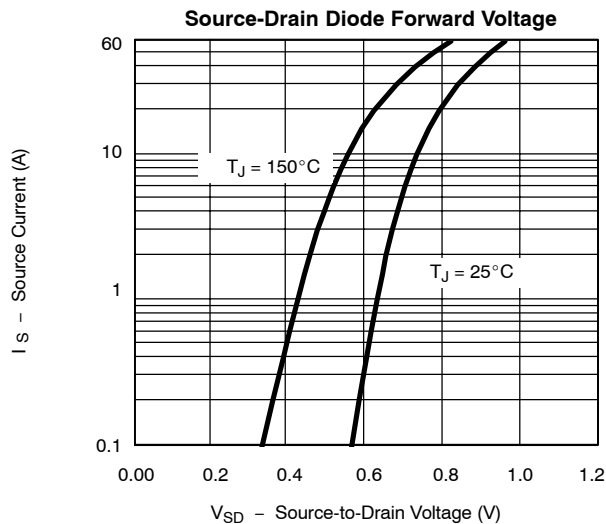
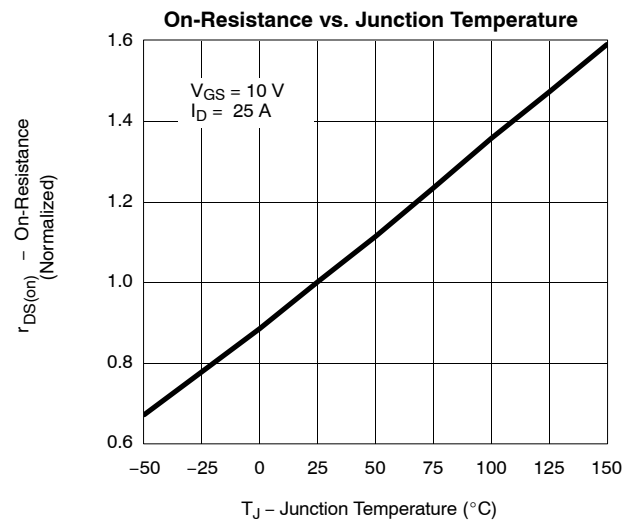
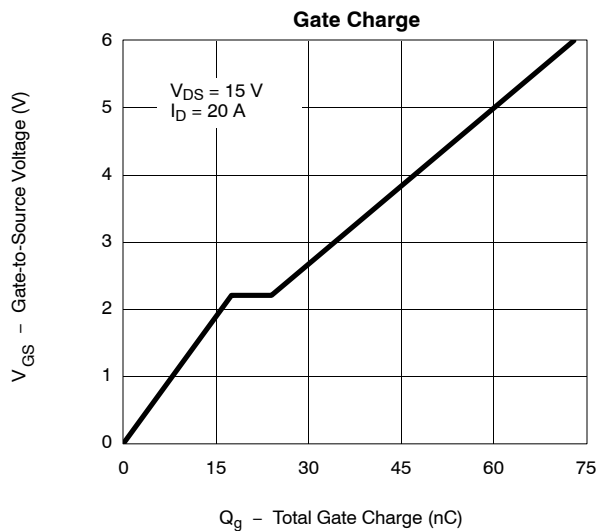
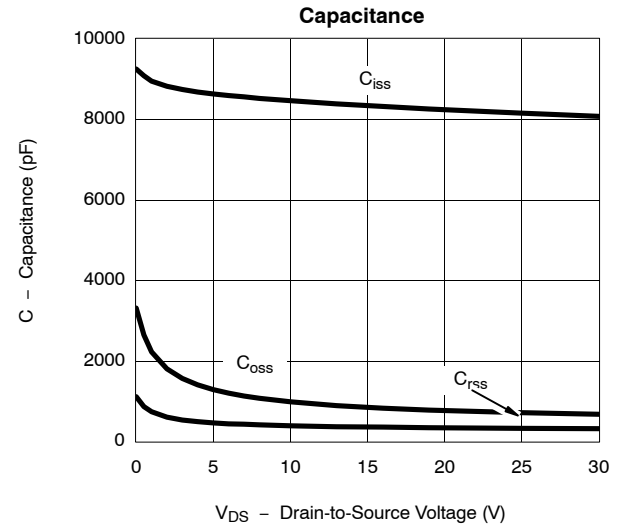
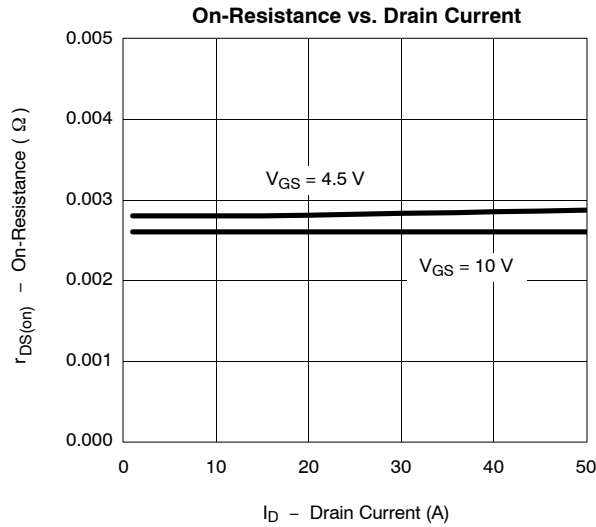
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

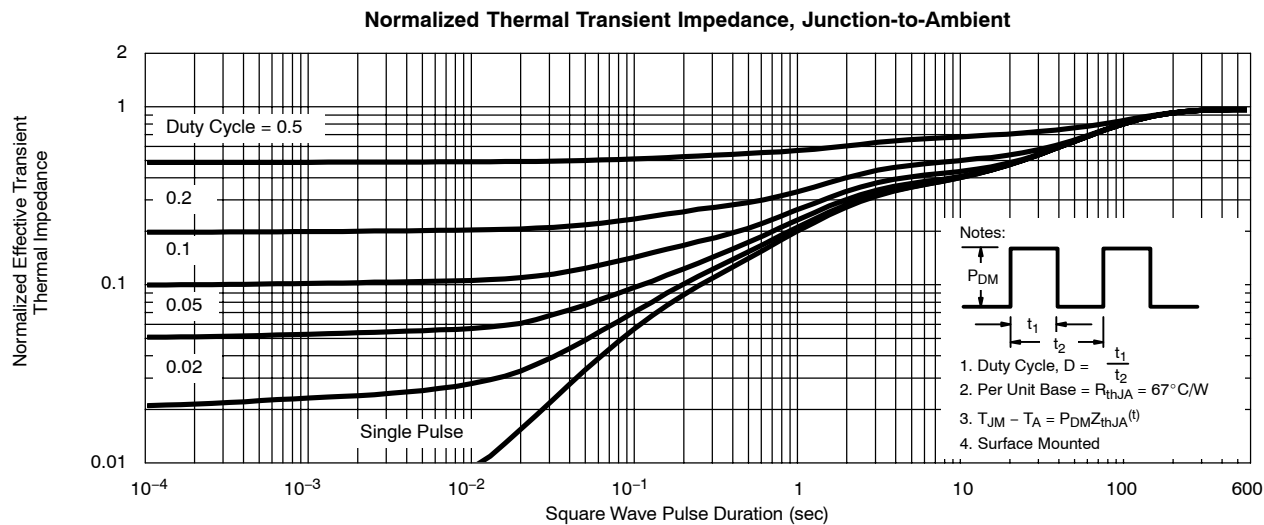
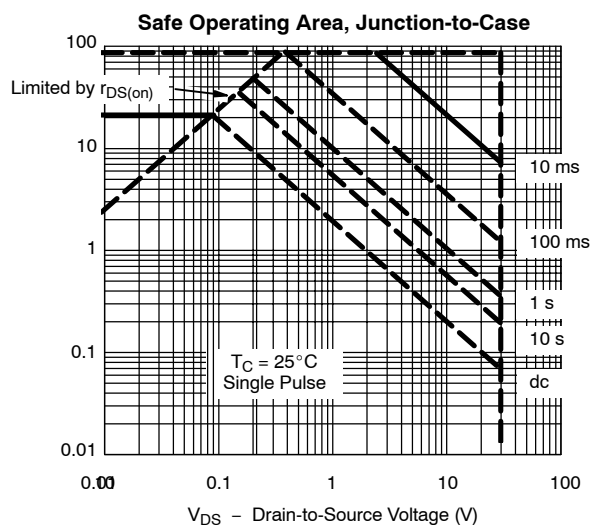
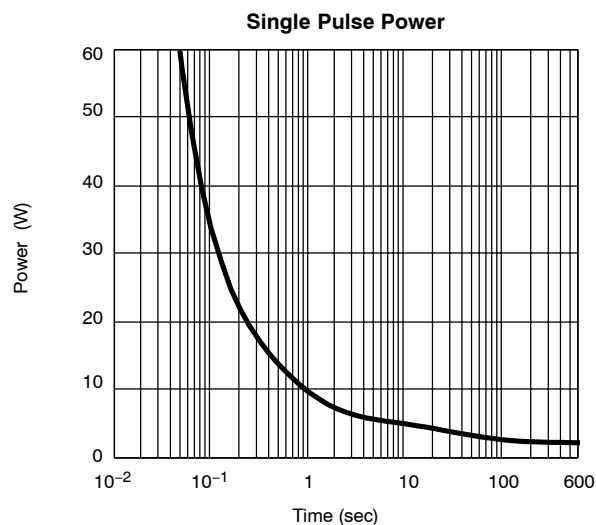
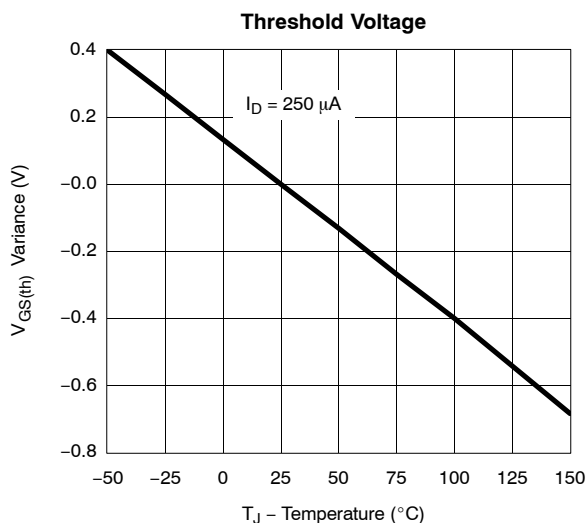
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 25\ \text{A}$		0.0026	0.0032	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 22\ \text{A}$		0.0029	0.0036	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 25\ \text{A}$		150		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.66	1.1	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		8340		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			355		
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 20\ \text{A}$		53	80	nC
Gate-Source Charge	Q_{gs}			17.5		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	$f = 1\ \text{MHz}$	0.8	1.2	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		25	38	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			172	260	
Fall Time	t_f			41	62	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		42	60	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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