



U74LVC2G04

CMOS IC

DUAL INVERTER

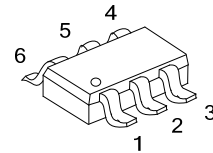
DESCRIPTION

The **U74LVC2G04** is a dual inverter gate and it provides the Boolean function $Y = \overline{A}$ in positive logic.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

FEATURES

- * Operate From 1.65V To 5.5V
- * Inputs Accept Voltages To 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Max t_{PD} Of 3.2 ns At 5V



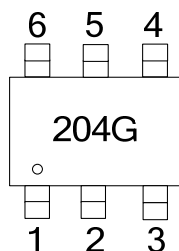
SOT-363

ORDERING INFORMATION

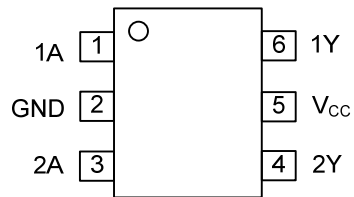
Ordering Number	Package	Packing
U74LVC2G04G-AL6-R	SOT-363	Tape Reel

U74LVC2G04G-AL6-R	(1)Packing Type (2)Package Type (3)Halogen Free	(1) R: Tape Reel (2) AL6: SOT-363 (3) G: Halogen Free
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MARKING



■ PIN CONFIGURATION

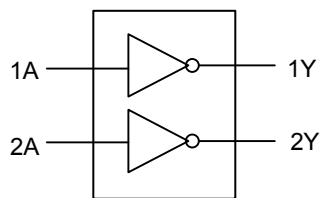


■ FUNCTION TABLE

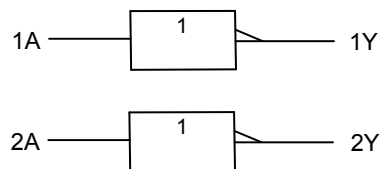
INPUT(nA)	OUTPUT(nY)
H	L
L	H

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +6.5	V
Input Voltage	V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Active Mode	$-0.5 \sim V_{CC} + 0.5$	V
	Power-Down Mode	-0.5 ~ +6.5	V
V_{CC} or GND Current	I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})	I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}>V_{CC}$ or $V_{OUT}<0$)	I_{OK}	±50	mA
Power Dissipation ($T_A=-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$)	P_D	300	mW
Operating Junction Temperature	T_J	-40 ~ +125	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	1.65		5.5	V
Input Voltage	V_{IN}	0		5.5	V
Output Voltage	Active Mode	0		V_{CC}	V
	Power-Down Mode	0		5.5	V
Input Transition Rise or Fall Rate	$V_{CC}=1.65\text{V to }2.7\text{V}$	0		20	ns/V
	$V_{CC}=2.7\text{V to }5.5\text{V}$	0		10	ns/V

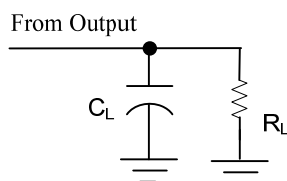
■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$	$0.65 \cdot V_{CC}$			V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$	1.7			V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$	2			V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$	$0.7 \cdot V_{CC}$			V
Low-level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$			$0.35 \cdot V_{CC}$	V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$			0.7	V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$			0.8	V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$			$0.3 \cdot V_{CC}$	V
High-Level Output Voltage	V_{OH}	$I_{OH}=-100\mu\text{A}$ $V_{CC}=1.65 \sim 5.5\text{V}$	$V_{CC}-0.1$			V
		$I_{OH}=-4\text{mA}$ $V_{CC}=1.65\text{V}$	1.2			V
		$I_{OH}=-8\text{mA}$ $V_{CC}=2.3\text{V}$	1.9			V
		$I_{OH}=-12\text{mA}$ $V_{CC}=2.7\text{V}$	2.2			V
		$I_{OH}=-24\text{mA}$ $V_{CC}=3.0\text{V}$	2.3			V
		$I_{OH}=-32\text{mA}$ $V_{CC}=4.5\text{V}$	3.8			V
Low-Level Output Voltage	V_{OL}	$I_{OL}=100\mu\text{A}$ $V_{CC}=1.65 \sim 5.5\text{V}$			0.1	V
		$I_{OL}=4\text{mA}$ $V_{CC}=1.65\text{V}$			0.45	V
		$I_{OL}=8\text{mA}$ $V_{CC}=2.3\text{V}$			0.3	V
		$I_{OL}=12\text{mA}$ $V_{CC}=2.7\text{V}$			0.4	V
		$I_{OL}=24\text{mA}$ $V_{CC}=3.0\text{V}$			0.55	V
		$I_{OL}=32\text{mA}$ $V_{CC}=4.5\text{V}$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5\text{V}$ or GND, $V_{CC}=5.5\text{V}$		±0.1	±5	μA
Power OFF Leakage Current	I_{OFF}	V_{IN} or $V_{OUT}=5.5\text{V}$, $V_{CC}=0\text{V}$		±0.1	±10	μA
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$ $V_{CC}=5.5\text{V}$		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=2.3 \sim 5.5\text{V}$, One input at $V_{CC}-0.6\text{V}$, Other inputs at V_{CC} or GND		5	500	μA

■ **SWITCHING CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$)

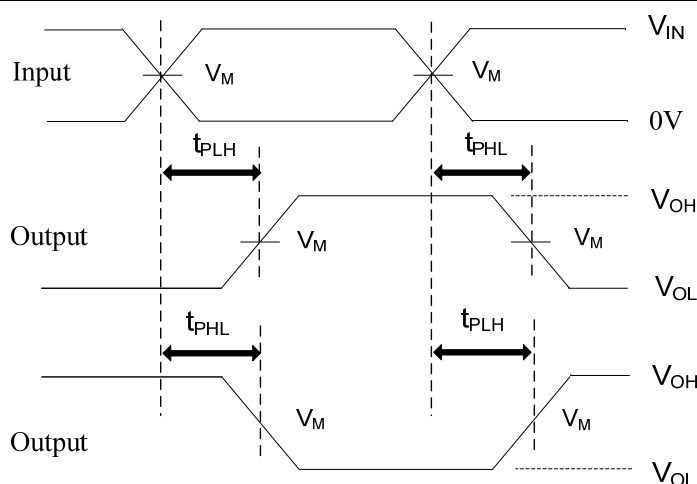
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH}	$V_{CC}=1.8\pm0.15\text{V}$, $R_L=1\text{K}\Omega$	1.0	3.5	8.0	ns
		$V_{CC}=2.5\pm0.2\text{V}$, $R_L=500\Omega$	1.0	2.2	4.4	ns
	t_{PHL}	$V_{CC}=2.7\text{V}$, $R_L=500\Omega$	1.0	2.7	5.2	ns
		$V_{CC}=3.3\pm0.3\text{V}$, $R_L=500\Omega$	0.5	2.7	4.1	ns
		$V_{CC}=5\pm0.5\text{V}$, $R_L=500\Omega$	1.0	1.9	3.2	ns

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	50pF	500 Ω



PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$.

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