Features

- AVR® High Performance and Low Power RISC Architecture
- 118 Powerful Instructions Most Single Clock Cycle Execution
- · 2K bytes of In-System Reprogrammable Flash
 - SPI Serial Interface for Program Downloading
 - Endurance: 1,000 Write/Erase Cycles
- 128 bytes EEPROM
 - Endurance: 100,000 Write/Erase Cycles
- 128 bytes Internal RAM
- 32 x 8 General Purpose Working Registers
- 15 Programmable I/O Lines
- V_{CC}: 2.7 6.0V
- Fully Static Operation
 - 0 10 MHz, 4.0 6.0V
 - 0 4 MHz, 2.7 6.0V
- Up to 10 MIPS Throughput at 10 MHz
- One 8-Bit Timer/Counter with Separate Prescaler
- One 16-Bit Timer/Counter with Separate Prescaler and Compare and Capture Modes
- Full Duplex UART
- · Selectable 8, 9 or 10 bit PWM
- External and Internal Interrupt Sources
- Programmable Watchdog Timer with On-Chip Oscillator
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes
- Programming Lock for Software Security
- 20-Pin Device

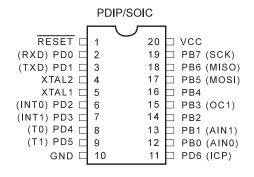
Description

The AT90S2313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

(continued)

Pin Configuration





8-Bit AVR®
Microcontroller
with 2K bytes
In-System
Programmable
Flash

AT90S2313

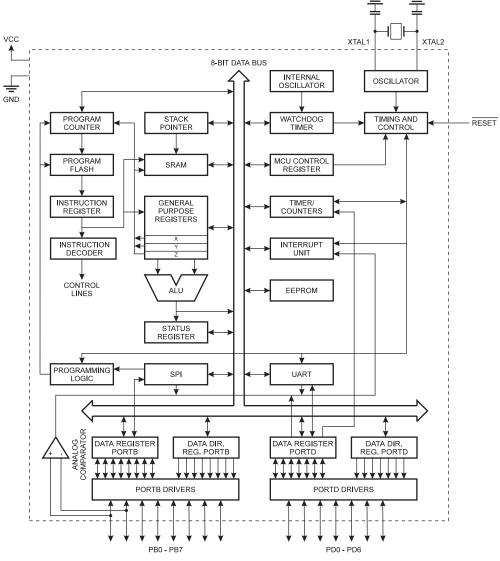
Rev. 0839DS-07/98





Block Diagram

Figure 1. The AT90S2313 Block Diagram



The AT90S2313 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 15 general purpose I/O lines, 32 general purpose working registers, flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, programmable Watchdog Timer with internal oscillator, an SPI serial port for Flash Memory downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip In-System

Programmable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S2313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S2313 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, incircuit emulators, and evaluation kits.

Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). PB0 and PB1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip analog comparator. The Port B output buffers can sink 20mA and can drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port B also serves the functions of various special features of the AT90S2313 as listed on page 38.

Port D (PD6..PD0)

Port D has seven bi-directional I/O pins with internal pull-up resistors, PD6..PD0. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Port D also serves the functions of various special features of the AT90S2313 as listed on page 43.

RESET

Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or a ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 3.

Figure 2. Oscillator Connections

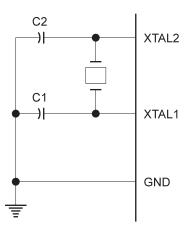
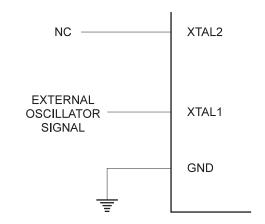


Figure 3. External Clock Drive Configuration







AT90S2313 Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file in one clock cycle.

Six of the 32 registers can be used as three 16-bits indirect address register pointers for Data Space addressing enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bits X-register, Y-register and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S2313 AVR Enhanced RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses (\$00 - \$1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O memory

can be accessed directly, or as the Data Space locations following those of the register file, \$20 - \$5F.

The AVR has Harvard architecture - with separate memories and buses for program and data. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-system Programmable Flash memory.

With the relative jump and call instructions, the whole 1K address space is directly accessed. Most *AVR* instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

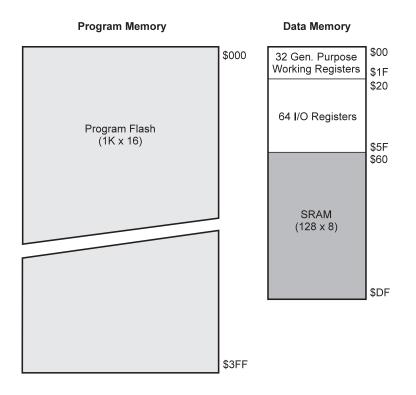
The 128 bytes data SRAM + register file and I/O registers can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 4. The AT90S2313 AVR Enhanced RISC Architecture

AVR AT90S2313 Architecture Data Bus 8-bit Program Counter Status and Test Control 1K x 16 Registrers Program FLASH Interrupt 32 x 8 General Unit Instruction Register Purpose Registrers SPI Unit Instruction Decoder Serial UART Indirect Addressing Direct Addressing ALU Control Lines 8-bit Timer/Counter Timer/Counter with PWM 128 x 8 Data SRAM Watchdog Timer 128 x 8 EEPROM Analog Comparator 15 I/O Lines

Figure 5. Memory Maps







AT90S2313 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F (\$5F)	SREG	l	Т	Н	S	V	N	Z	С	17
\$3E (\$5E)	Reserved		T		T ===	1	T	T ===	1	
\$3D (\$5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	18
\$3C (\$5C)	Reserved				1	1	1	1	1	
\$3B (\$5B)	GIMSK	INT1	INT0	-	-	-	-	-	-	23
\$3A (\$5A)	GIFR	INTF1	INTF0			TIQUEA		TOLES		23
\$39 (\$59)	TIMSK	TOIE1	OCIE1A	-	-	TICIE1	-	TOIE0	-	23
\$38 (\$58) \$37 (\$57)	TIFR	TOV1	OCF1A	-	-	ICF1	-	TOV0	-	24
	Reserved									
\$36 (\$56) \$35 (\$55)	Reserved MCUCR	_	l -	SE	SM	ISC11	ISC10	ISC01	ISC00	25
\$34 (\$54)	Reserved	-	-	J SE	SIVI	13011	13010	13001	13000	20
\$33 (\$53)	TCCR0			_	_		CS02	CS01	CS00	28
\$32 (\$52)	TCNT0	Timer/Cou	nter0 (8 Bit)				0302	0301	0300	29
\$32 (\$52)	Reserved	Timer/Cou	ritero (o bit)							29
\$30 (\$50)	Reserved									
\$2F (\$4F)	TCCR1A	COM1A1	COM1A0	_	_	I -	_	PWM11	PWM10	30
\$2E (\$4E)	TCCR1B	ICNC1	ICES1		_	CTC1	CS12	CS11	CS10	31
\$2D (\$4D)	TCNT1H			er Register Hig	nh Byte	0101	0012	0011	0010	32
\$2C (\$4C)	TCNT1L			er Register Lo						32
\$2B (\$4B)	OCR1AH			are Register H						32
\$2A (\$4A)	OCR1AL			are Register L	,					32
\$29 (\$49)	Reserved			aro regiotor <u>-</u>	o 2510					02
\$28 (\$48)	Reserved									
\$27 (\$47)	Reserved									
\$26 (\$46)	Reserved									
\$25 (\$45)	ICR1H	Timer/Cou	nter1 - Input C	Capture Regist	ter High Byte					33
\$24 (\$44)	ICR1L			Capture Regist	0 ,					33
\$23 (\$43)	Reserved		,	, ,	Í					
\$22 (\$42)	Reserved									
\$21 (\$41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	35
\$20 (\$40)	Reserved									
\$1F (\$3F)	Reserved									
\$1E (\$3E)	EEAR	-		Address Regis	ter					36
\$1D (\$3D)	EEDR	EEPROM	Data register							37
\$1C (\$3C)	EECR	-	-	-	-	-	EEMWE	EEWE	EERE	37
\$1B (\$3B)	Reserved									
\$1A (\$3A)	Reserved									
\$19 (\$39)	Reserved									
\$18 (\$38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	46
\$17 (\$37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	46
\$16 (\$36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	46
\$15 (\$35)	Reserved									
\$14 (\$34)	Reserved									
\$13 (\$33)	Reserved		T =							
\$12 (\$32)	PORTD	-	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	51
\$11 (\$31)	DDRD	-	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	51
\$10 (\$30)	PIND	-	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	51
\$0F (\$2F)	Reserved									
\$0E (\$2E)	Reserved									
\$0D (\$2D)	Reserved	11455 :::								40
\$0C (\$2C)	UDR		Data Register							40
\$0B (\$2B)	USR	RXC	TXC	UDRE	FE	OR	-	-	-	40
\$0A (\$2A)	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	41
\$09 (\$29)	UBRR		d Rate Regist		40:	40:5	1000	40:01	4.0:00	43
\$08 (\$28)	ACSR	ACD	-	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	44
 #00 (#00)	Reserved									
\$00 (\$20)	Reserved									l

AT90S2313 Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTIO	NS			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl – K	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd v Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	Rd ← \$FF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← \$00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd v K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	Rd ← \$FF	None	1
BRANCH INSTRUCT	IONS				
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	1	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (R(b)=1) PC ← PC + 2 or 3	None	1/2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V= 0) then PC \leftarrow PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2





Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER	RINSTRUCTIONS	· ·			
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1$, $Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z)$ $Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1$, $Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect and Tre-Dec. Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect Store Indirect and Post-Inc.			2
			$(X) \leftarrow Rr, X \leftarrow X + 1$	None	
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1$, $(Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
BIT AND BIT-TES	T INSTRUCTIONS				
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0)\leftarrow C, Rd(n+1)\leftarrow Rd(n), C\leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	i i	$Rd(n) \leftarrow Rd(n+1), n=06$	2,0,11,1	
71011		I Arithmetic Shift Right		Z C N V	
SWAP		Arithmetic Shift Right Swap Nibbles		Z,C,N,V None	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1 1
BSET	Rd s	Swap Nibbles Flag Set	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$	None SREG(s)	1 1 1
BSET BCLR	Rd s s	Swap Nibbles Flag Set Flag Clear	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$	None SREG(s) SREG(s)	1 1 1 1
BSET BCLR BST	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \end{array} $	None SREG(s) SREG(s) T	1 1 1 1
BSET BCLR BST BLD	Rd s s	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \end{array} $	None SREG(s) SREG(s) T None	1 1 1 1 1
BSET BCLR BST BLD SEC	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C	1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \end{array} $	None SREG(s) SREG(s) T None C C	1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C C N	1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \end{array} $	None SREG(s) SREG(s) T None C C N N	1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C C N N Z	1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \end{array} $	None SREG(s) SREG(s) T None C C N N	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C C N N Z	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$	None SREG(s) SREG(s) T None C C N N Z Z I	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$ $S \leftarrow 1$	None SREG(s) SREG(s) T None C C N N I I I I I I S	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Clear Argound Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$ $S \leftarrow 1$ $S \leftarrow 0$	None SREG(s) SREG(s) T None C C N N I I I I I I S S S	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$ $S \leftarrow 1$ $S \leftarrow 0$ $V \leftarrow 1$	None SREG(s) SREG(s) T None C C N N I S I S S I I I S S S V	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SES	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Clear Argound Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$ $S \leftarrow 1$ $S \leftarrow 0$	None SREG(s) SREG(s) T None C C N N I I I I I I S S S	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SES CLS SEV CLV	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$ $SREG(s) \leftarrow 0$ $T \leftarrow Rr(b)$ $Rd(b) \leftarrow T$ $C \leftarrow 1$ $C \leftarrow 0$ $N \leftarrow 1$ $N \leftarrow 0$ $Z \leftarrow 1$ $Z \leftarrow 0$ $I \leftarrow 1$ $I \leftarrow 0$ $S \leftarrow 1$ $S \leftarrow 0$ $V \leftarrow 1$	None SREG(s) SREG(s) T None C C N N I S I S S I I I S S S V	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV CLV	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \\ I \leftarrow 0 \\ S \leftarrow 1 \\ S \leftarrow 0 \\ V \leftarrow 1 \\ V \leftarrow 0 \\ \end{array} $	None SREG(s) SREG(s) T None C C N N I S S S S V V V	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV CLV SET CLT	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Clear Sero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG Clear T in SREG	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \\ I \leftarrow 0 \\ S \leftarrow 1 \\ S \leftarrow 0 \\ V \leftarrow 1 \\ V \leftarrow 0 \\ T \leftarrow 1 \\ T \leftarrow 0 \\ \end{array} $	None SREG(s) SREG(s) T None C C N N S S S S V V V T T	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV CLV SET CLT SEH	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG Clear T in SREG Set Half Carry Flag in SREG	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \\ I \leftarrow 0 \\ S \leftarrow 1 \\ S \leftarrow 0 \\ V \leftarrow 1 \\ V \leftarrow 0 \\ T \leftarrow 1 \\ T \leftarrow 0 \\ H \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C C N N S S S S V V T T H	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV CLV SET CLT SEH CLH	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG Clear T in SREG Set Half Carry Flag in SREG Clear Half Carry Flag in SREG	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \\ I \leftarrow 0 \\ S \leftarrow 1 \\ S \leftarrow 0 \\ V \leftarrow 1 \\ V \leftarrow 0 \\ T \leftarrow 1 \\ T \leftarrow 0 \\ \end{array} $	None SREG(s) SREG(s) T None C C N N S S S S V V V T T H H H	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
BSET BCLR BST BLD SEC CLC SEN CLN SEZ CLZ SEI CLI SES CLS SEV CLV SET	Rd s s Rr, b	Swap Nibbles Flag Set Flag Clear Bit Store from Register to T Bit load from T to Register Set Carry Clear Carry Set Negative Flag Clear Negative Flag Set Zero Flag Clear Zero Flag Global Interrupt Enable Global Interrupt Disable Set Signed Test Flag Clear Signed Test Flag Set Twos Complement Overflow Clear Twos Complement Overflow Set T in SREG Clear T in SREG Set Half Carry Flag in SREG	$ \begin{array}{c} Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30) \\ SREG(s) \leftarrow 1 \\ SREG(s) \leftarrow 0 \\ T \leftarrow Rr(b) \\ Rd(b) \leftarrow T \\ C \leftarrow 1 \\ C \leftarrow 0 \\ N \leftarrow 1 \\ N \leftarrow 0 \\ Z \leftarrow 1 \\ Z \leftarrow 0 \\ I \leftarrow 1 \\ I \leftarrow 0 \\ S \leftarrow 1 \\ S \leftarrow 0 \\ V \leftarrow 1 \\ V \leftarrow 0 \\ T \leftarrow 1 \\ T \leftarrow 0 \\ H \leftarrow 1 \end{array} $	None SREG(s) SREG(s) T None C C N N S S S S V V T T H	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1