SPANSION™ MCP

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50225-2E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & FCRAM

CMOS

128M (×16) FLASH MEMORY & 32M (×16) Mobile FCRAM™

MB84VP24491HK-70

■ FEATURES

- **Power Supply Voltage of 2.7 V to 3.1 V**
- **High Performance**
  20 ns maximum page read access time, 70 ns maximum random access time (Flash)
  20 ns maximum page read access time, 70 ns maximum random access time (FCRAM)
- **Operating Temperature**
  –30 °C to +85 °C
- **Package 73-ball FBGA**

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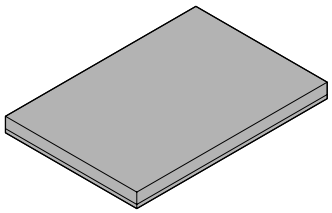
■ PRODUCT LINEUP

	Flash	FCRAM
Supply Voltage (V)	$V_{CC}f^*$ = 3.0 V $^{+0.1V}_{-0.3\ V}$	$V_{CC}r^*$ = 3.0 V $^{+0.1V}_{-0.3\ V}$
Max Random Address Access Time (ns)	70	70
Max Page Address Access Time (ns)	20	20
Max $\overline{CE}$ Access Time (ns)	70	70
Max $\overline{OE}$ Access Time (ns)	20	40

*: Both $V_{CC}f$ and $V_{CC}r$ must be the same level when either part is being accessed.

■ PACKAGE

73-ball plastic FBGA



(BGA-73P-M03)

FUJITSU

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— **FLASH MEMORY**

- **0.13 µm Process Technology**
- **Dual Chip Enable ($\overline{CE}$0f, $\overline{CE}$1f)**
  $\overline{CE}$0f controls 64M bits (Bank A and Bank B) region and $\overline{CE}$1f controls 64M bits (Bank C and Bank D) bits region.
- **Single 3.0 V Read, Program and Ease**
  Minimized system level power requirements
- **Simultaneous Read/Write Operations (Dual Bank)**
- **FlexBank™ *1**
  Bank A($\overline{CE}$0f): 16 Mbit (4 KW ×8 and 32 KW ×31)
  Bank B($\overline{CE}$0f): 48 Mbit (32 KW ×96)
  Bank C($\overline{CE}$1f): 48 Mbit (32 KW ×96)
  Bank D($\overline{CE}$1f): 16 Mbit (4 KW ×8 and 32 KW ×31)
- **High Performance Page Mode**
  20 ns maximum page access time (70 ns random access time)
- **8 words Page Access Capability**
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**
  Eight 4 Kwords, two hundred fifty-four 32 Kwords, eight 8 Kwords sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Dual Boot Block**
  Sixteen 4Kwords boot block sectors, eight at the top of the address range and eight at the bottom of the address range
- **HiddenROM Region**
  256 byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{WP}$/ACC Input Pin**
  At V_{IL}, allows protection of “outermost” 2×4 K words on both ends of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™ *2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{Data}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready/Busy Output (RY/$\overline{BY}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, the device automatically switches itself to low power mode
- **Low V_{CC} Write Inhibit ≤ 2.5 V**
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Hardware Reset Pin ($\overline{RESET}$)**
  Hardware method to reset the device for reading array data

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- **New Sector Protection**
  Persistent Sector Protection
  Password Sector Protection
- **Please refer to “MBM29RM12DH” Datasheet in detailed function**

— FCRAM™ *3

- **Power Dissipation**
  Operating : 30 mA Max
  Standby : 100 µA Max
- **Power Down Mode**
  Sleep : 10 µA Max
  4M Partial : 45 µA Max
  8M Partial : 55 µA Max
  16M Partial: 70 µA Max
- **Power Down Control by CE2r**
- **Byte Write Control: $\overline{LB}$(DQ_7 to DQ_0), $\overline{UB}$(DQ_{15} to DQ_8)**
- **8 words Page Access Capability**

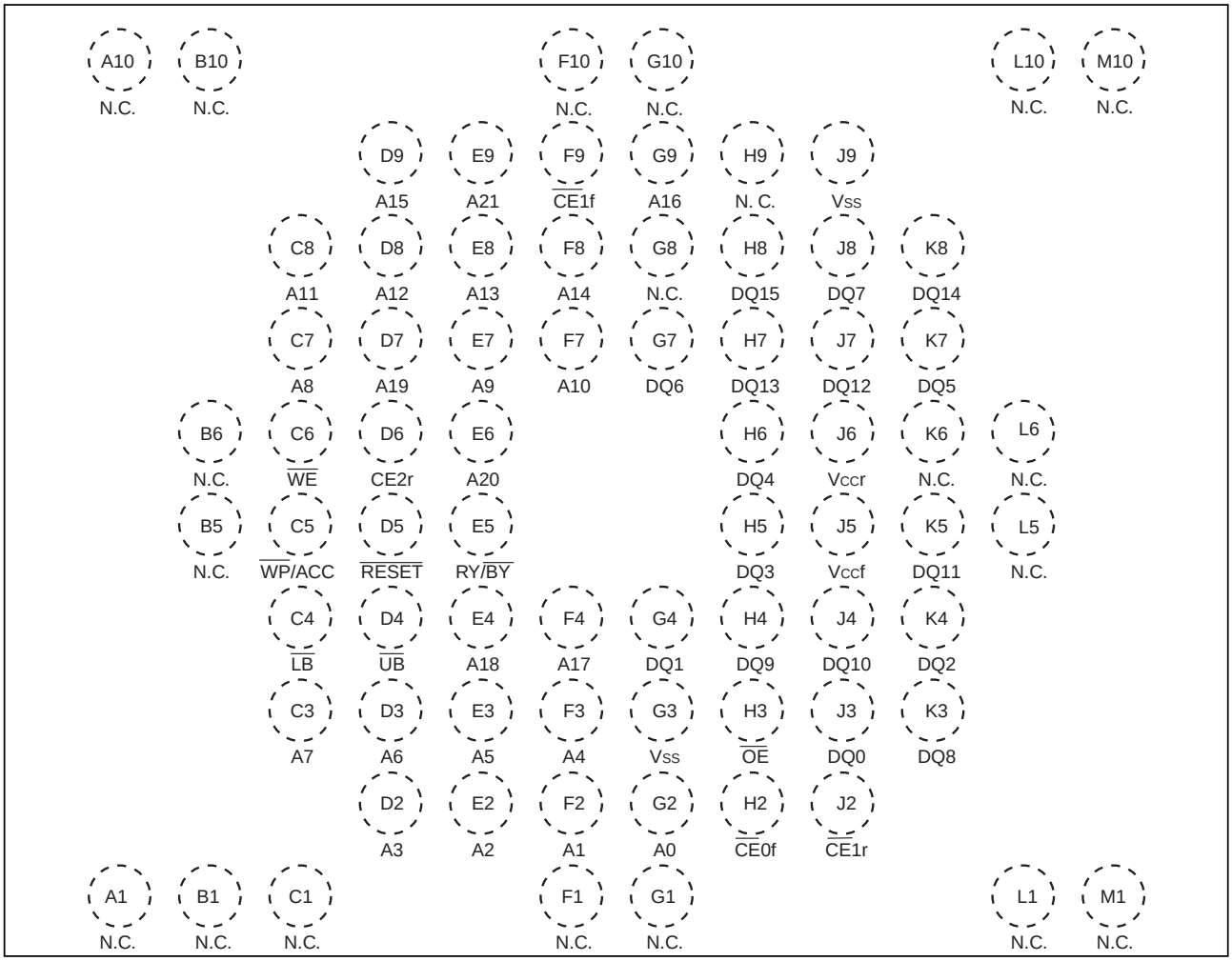
*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

*3: Mobile FCRAM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

(Top View)
Marking Side



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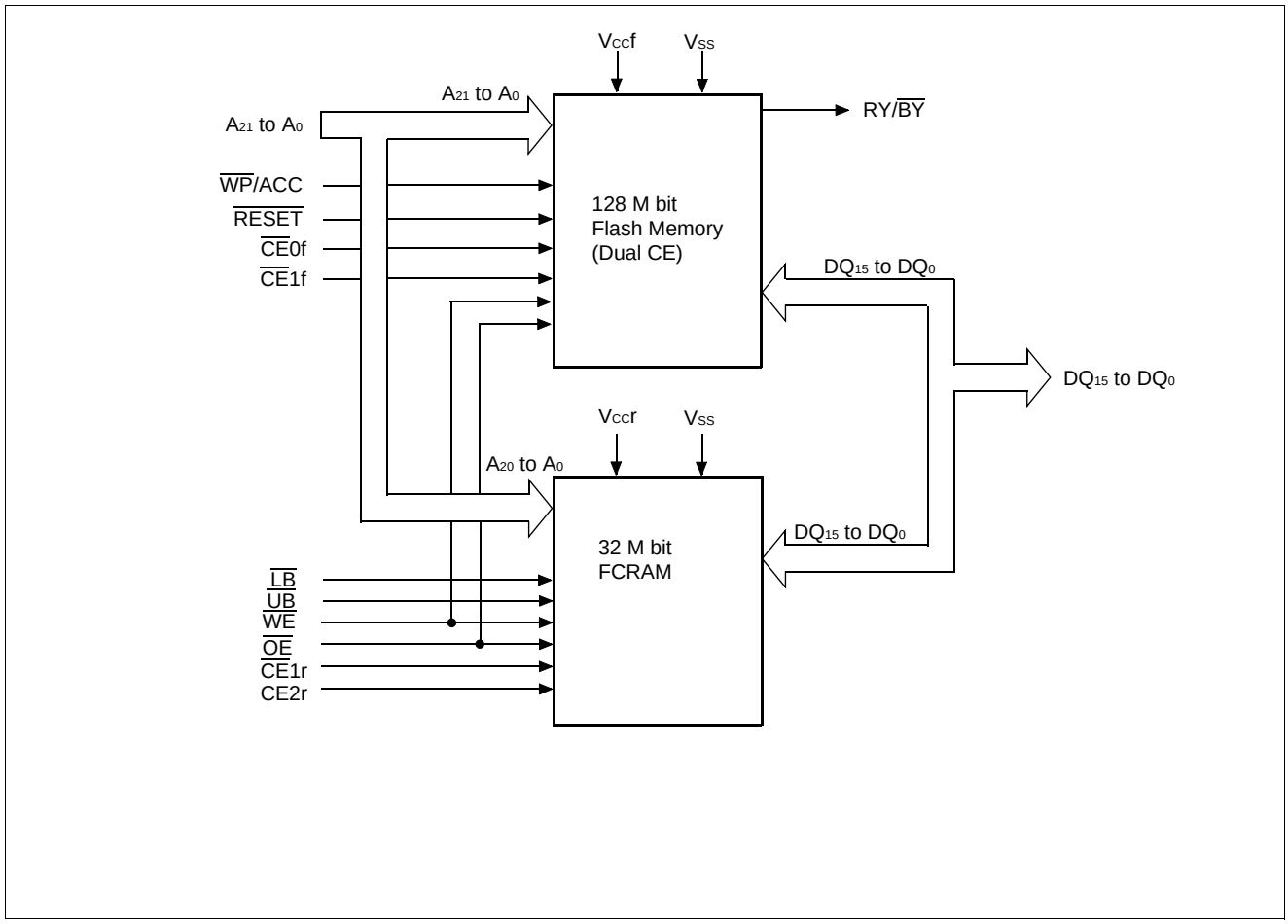
■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A_{20} to A_0	I	Address Inputs (Common)
A_{21}	I	Address Input (Flash)
DQ_{15} to DQ_0	I/O	Data Inputs/Outputs (Common)
$\overline{CE}$0f	I	Chip Enable (Flash)
$\overline{CE}$1f	I	Chip Enable (Flash)
$\overline{CE}$1r	I	Chip Enable (FCRAM)
CE2r	I	Chip Enable (FCRAM)
$\overline{OE}$	I	Output Enable (Common)
$\overline{WE}$	I	Write Enable (Common)
RY/$\overline{BY}$	O	Ready/Busy Output (Flash) Open Drain Output
$\overline{UB}$	I	Upper Byte Control (FCRAM)
$\overline{LB}$	I	Lower Byte Control (FCRAM)
$\overline{RESET}$	I	Hardware Reset Pin/Sector Protection Unlock (Flash)
$\overline{WP}$/ACC	I	Write Protect / Acceleration (Flash)
N.C.	—	No Internal Connection
V_{SS}	Power	Device Ground (Common)
V_{CC}f	Power	Device Power Supply (Flash)
V_{CC}r	Power	Device Power Supply (FCRAM)

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

Operation*1, *2	$\overline{CE}$0f	$\overline{CE}$1f	$\overline{CE}$1r	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	A_{21} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ ACC *9
Full Standby	H	H	H	H	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable*3	H	H	L	H	H	H	X	X	X*8	High-Z	High-Z	H	X
	L	H	H						X				
	H	L	H										
Read from Flash*4	L	H	H	H	L	H	X	X	Valid	D_{OUT}	D_{OUT}	H	X
	H	L											
Write to Flash	L	H	H	H	H	L	X	X	Valid	D_{IN}	D_{IN}	H	X
	H	L	H	H	H	L	X	X	Valid	D_{IN}	D_{IN}	H	X
Read from FCRAM	H	H	L	H	L	H	L	L	Valid	D_{IN}	D_{IN}	H	X
							H	L		High-Z	D_{IN}		
							L	H		D_{IN}	High-Z		
FCRAM No Read	H	H	L	H	L	H	H	H	Valid	High-Z	High-Z	H	X
Write to FCRAM	H	H	L	H	H*7	L	L	L	Valid	D_{IN}	D_{IN}	H	X
							H	L		High-Z	D_{IN}		
							L	H		D_{IN}	High-Z		
FCRAM No Write	H	H	L	H	H*7	L	H	H	Valid	High-Z	High-Z	H	X
Flash Temporary Sector Group Unprotection*5	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	X	H	H	X	X	X	X	X	High-Z	High-Z	L	X
Flash Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L
FCRAM Power Down*6	X	X	X	L	X	X	X	X	X	X	X	X	X

Legend: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance.
See ■DC CHARACTERISTICS for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : Do not apply for two or more states of the following conditions at the same time;
- $\overline{CE}$0f = V_{IL}
- $\overline{CE}$1f = V_{IL}
- $\overline{CE}$1r = V_{IL} and CE2r = V_{IH}

*3 : Should not be kept FCRAM Output Disable condition longer than 1µs.

*4 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*5 : It is also used for the extended sector group protections.

*6 : FCRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Power Down Program. Please refer to “Power Down Program” in FCRAM Characteristics part.

*7 : $\overline{OE}$ can be V_{IL} during Write operation if the following conditions are satisfied;
1) Write pulse is initiated by $\overline{CE}$1r (refer to $\overline{CE}$1r Controlled Write timing), or cycle time of the previous operation cycle is satisfied.
2) $\overline{OE}$ stays V_{IL} during Write cycle.

*8 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*9 : Protect “outer most” 2x8K bytes (4 words) on both ends of the boot block sectors.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins except $\overline{\text{RESET}}$, $\overline{\text{WP}}$/ACC *1	V_{IN}, V_{OUT}	–0.3	$V_{CC}f$ +0.3	V
			$V_{CC}r$ +0.3	V
$V_{CC}f$/$V_{CC}r$ Supply *1	$V_{CC}f$, $V_{CC}r$	–0.3	+3.3	V
$\overline{\text{RESET}}$ *2	V_{IN}	–0.5	+ 13.0	V
$\overline{\text{WP}}$/ACC *3	V_{IN}	–0.5	+10.5	V

*1 Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –1.0 V for periods of up to 5 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$ + 0.3 V or $V_{CC}r$ + 0.3V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$ + 2.0 V or $V_{CC}r$ + 1.0 V for periods of up to 5 ns.

*2: Minimum DC input voltage on $\overline{\text{RESET}}$ pin is –0.5 V. During voltage transitions $\overline{\text{RESET}}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} – $V_{CC}f$) does not exceed +9.0 V. Maximum DC input voltage on $\overline{\text{RESET}}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on $\overline{\text{WP}}$/ACC pin is –0.5 V. During voltage transitions, $\overline{\text{WP}}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP}}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	–30	+85	°C
$V_{CC}f$/$V_{CC}r$ Supply Voltages	$V_{CC}f$, $V_{CC}r$	+2.7	+3.1	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ DC CHARACTERISTICS

Parameter	Sym-bol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}f, V_{CC}r		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}f, V_{CC}r, Output Disable		–1.0	—	+1.0	µA
$\overline{\text{RESET}}$ Inputs Leakage Current (Flash)	I_{LIT}	V_{CC}f = V_{CC}f Max, $\overline{\text{RESET}}$ = 12.5 V		—	—	35	µA
$\overline{\text{WP}}$/ACC Acceleration Program Current (Flash)	I_{LIA}	V_{CC}f = V_{CC}f Max, $\overline{\text{WP}}$/ACC = V_{ACC} Max		—	—	20	mA
Flash V_{CC} Active Current (Read) *1	I_{CC1}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$= V_{IH}	f = 10 MHz	—	—	45	mA
		$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$= V_{IH}	f = 5 MHz	—	—	25	mA
Flash V_{CC} Active Current *2	I_{CC2}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$f= V_{IH}		—	—	25	mA
Flash V_{CC} Current (Standby)	I_{SB1}f	V_{CC}f = V_{CC}f Max,$\overline{\text{CE}}$0f, $\overline{\text{CE}}$1f = V_{CC}f ±0.3 V $\overline{\text{RESET}}$= V_{CC}f ±0.3 V, $\overline{\text{WP}}$/ACC =V_{CC}f ±0.3 V		—	1	5	µA
Flash V_{CC} Current (Standby, Reset)	I_{SB2}f	V_{CC}f = V_{CC}f Max, $\overline{\text{RESET}}$= V_{SS} ±0.3 V		—	1	5	µA
Flash V_{CC} Current (Automatic Sleep Mode) *3	I_{SB3}f	V_{CC}f = V_{CC}f Max, $\overline{\text{CE}}$0f, $\overline{\text{CE}}$1f= V_{SS} ±0.3 V, $\overline{\text{RESET}}$= V_{CC}f ±0.3 V, V_{IN} = V_{CC}f ±0.3 V or V_{SS}f±0.3 V		—	1	5	µA
Flash V_{CC} Active Current (Read-while-Program) *5	I_{CC3}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$= V_{IH}		—	—	45	mA
Flash V_{CC} Active Current (Read-while-Erase) *5	I_{CC4}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$= V_{IH}		—	—	45	mA
Flash V_{CC} Active Current (Erase Suspend Program)	I_{CC5}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$= V_{IH}		—	—	25	mA
Flash V_{CC} Active Current (Page Mode Read)	I_{CC6}f	$\overline{\text{CE}}$ ($\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f) = V_{IL}, $\overline{\text{OE}}$ = V_{IH}, 8 Word Read		—	—	10	mA
FCRAM V_{CC} Active Current *8	I_{CC1}r	V_{CC}r = V_{CC}r Max, $\overline{\text{CE}}$1r = V_{IL}, CE2r = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA*7	t_{RC} / t_{WC} =Min	—	—	30	mA
	I_{CC2}r		t_{RC} / t_{WC} =1 µs	—	—	3	
FCRAM V_{CC} Page Read Current *8	I_{CC3}r	V_{CC}r = V_{CC}r Max, V_{IN} = V_{IH} or V_{IL}, $\overline{\text{CE}}$1r = V_{IL}, CE2r = V_{IH}, I_{OUT} = 0 mA *7, t_{PRC}=Min		—	—	10	mA
FCRAM V_{CC} Standby Current *8	I_{SB1}r	V_{CC}r = V_{CC}r Max, V_{IN} ≤ 0.2V or ≥ V_{CC}r – 0.2V $\overline{\text{CE}}$1r ≥ V_{CC}r – 0.2V, CE2r ≥ V_{CC}r– 0.2V		—	—	100	µA
FCRAM V_{CC} Power Down Current *8	I_{DDPS}r	V_{CC}r = V_{CC}r Max, CE2r ≤ 0.2V, V_{IN} = V_{IH} or V_{IL}	Sleep	—	—	10	µA
	I_{DDP4}r		4M Partial	—	—	45	µA
	I_{DDP8}r		8M Partial	—	—	55	µA
	I_{DDP16}r		16M Partial	—	—	70	µA

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Parameter	Sym-bol	Conditions		Value			Unit
				Min	Typ	Max	
Input Low Level	V_{IL}	—		–0.3	—	$V_{CC} \times 0.2$ *6	V
Input High Level	V_{IH}	—		$V_{CC} \times 0.8$	—	V_{CC}+ 0.2 *6	V
Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) *4	V_{ID}	—		11.5	12	12.5	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration *4	V_{ACC}	—		8.5	9.0	9.5	V
Output Low Voltage Level	$V_{OL}f$	$V_{CC}f$ = $V_{CC}f$ Min, I_{OL} = 0.1 mA	Flash	—	—	$V_{CC}f \times 0.15$	V
	$V_{OL}r$	$V_{CC}r$ = $V_{CC}r$ Min, I_{OL} = 1.0 mA	FCRAM	—	—	0.4	V
Output High Voltage Level	$V_{OH}f$	$V_{CC}f$ = $V_{CC}f$ Min, I_{OH} = –0.1 mA	Flash	$V_{CC}f \times 0.85$	—	—	V
	$V_{OH}r$	$V_{CC}r$ = $V_{CC}r$ Min, I_{OH} = –0.5 mA	FCRAM	2.4	—	—	V
Flash Low $V_{CC}f$ Lock-Out Voltage	V_{LKO}	—		2.3	2.4	2.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only $V_{CC}f$ applying.

*5: Embedded Algorithm (program or erase) is in progress. (@5 MHz)

*6: V_{CC} indicates lower of $V_{CC}f$ or $V_{CC}r$.

*7: FCRAM Characteristics are measured after following POWER-UP timing.

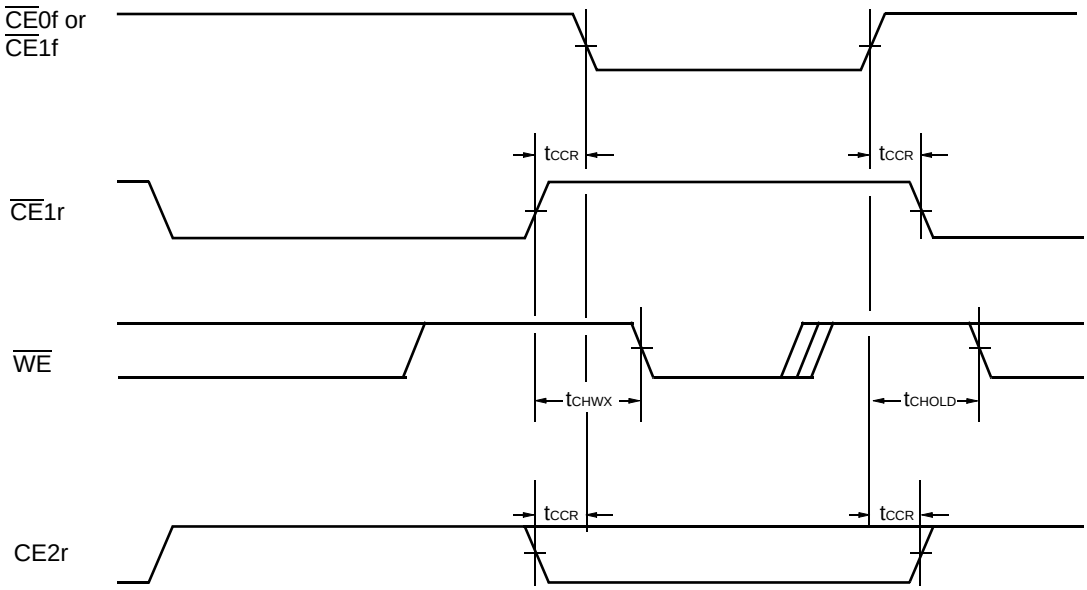
*8: I_{OUT} depends on the output load conditions.

■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min	Max	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	—	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	—	ns
$\overline{CE}$1r High to $\overline{WE}$ Invalid time for Standby Entry	—	t_{CHWX}	—	10	—	ns

- **Timing Diagram for alternating RAM to Flash**



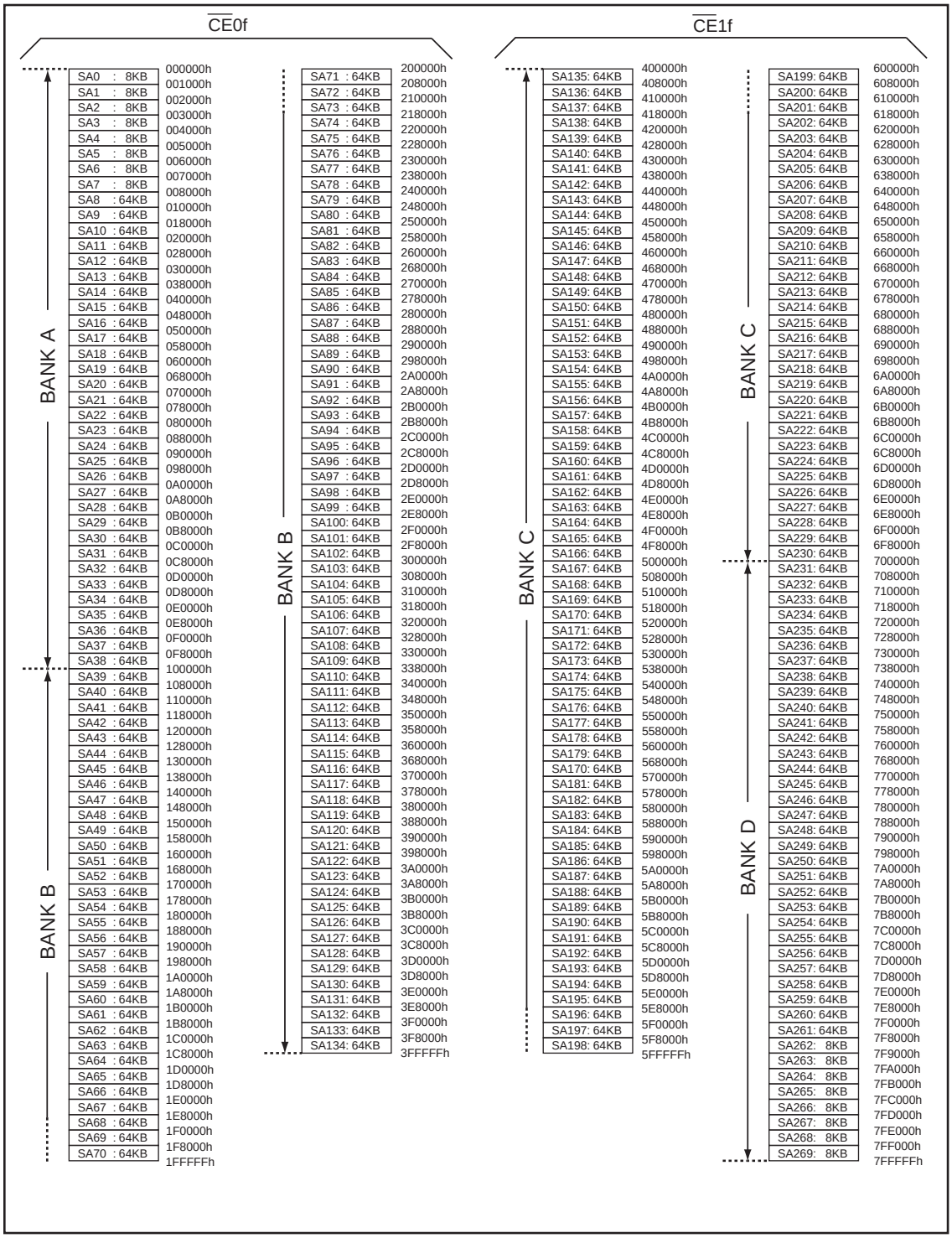
- **Flash Characteristics**
  Please refer to “■128 M PAEG FLASH MEMORY CHARACTERISTICS for MCP”.

- **FCRAM Characteristics**
  Please refer to “■32 M FCRAM CHARACTERISTICS for MCP”.

■ 128 M PAGE FLASH MEMORY CHARACTERISTICS for MCP

1. Flexible Sector-erase Architecture on FLASH MEMORY (128M Page Flash)

- Sixteen 4K words, and two hundred fifty-four 32K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



• **FlexBank™ Architecture (128M Page Flash)**

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	16 Mbit	Bank A	112 Mbit	Remainder (Bank B, C, D)
2	48 Mbit	Bank B	80 Mbit	Remainder (Bank A, C, D)
3	48 Mbit	Bank C	80 Mbit	Remainder (Bank A, B, D)
4	16 Mbit	Bank D	112 Mbit	Remainder (Bank A, B, C)

• **Example of Virtual Banks Combination (128M Page Flash)**

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	16 Mbit	Bank A	8 × 4 Kword + 31 x 32 Kword	112 Mbit	Bank B + Bank C + Bank D	8 x 4 Kword + 223 x 32 Kword
2	32 Mbit	Bank A + Bank D	16 x 4 Kword + 62 x 32 Kword	96 Mbit	Bank B + Bank C	192 x 32 Kword
3	48 Mbit	Bank B	96 x 32 Kword	80 Mbit	Bank A + Bank C + Bank D	16 x 4 Kword + 158 x 32 Kword
4	64 Mbit	Bank A + Bank B	8 x 4 Kword + 127 x 32 Kword	64 Mbit	Bank C + Bank D	8 x 4 Kword + 127 x 32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

• **Simultaneous Operation (Dual $\overline{CE}$) (128M Page Flash)**

The device features functions that enable reading of data from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation) , in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank can be selected by bank address (A_{21}, A_{20}) with zero latency. The device consists of the following four banks :
$\overline{CE}$0f control: Bank A : 8 x 4 KW and 31 x 32 KW; Bank B : 96 x 32 KW
$\overline{CE}$1f control: Bank C : 96 x 32 KW; Bank D : 8 x 4 KW and 31 x 32 KW.
The possible combinations for simultaneous operation is show as following table. ((Refer to Figure 11 Bank-to-Bank Read/Write Timing Diagram.)

• **Simultaneous Operation for Dual CE (128M Page Flash)**

Case	Bank 1 ($\overline{CE}$0f) Status 16 Mbit	Bank 2 ($\overline{CE}$0f) Status 48 Mbit	Bank 1 ($\overline{CE}$1f) Status 48 Mbit	Bank 2 ($\overline{CE}$1f) Status 16 Mbit
1	Read mode	Read mode	Read mode	Read mode
2	Autoselect mode	Read mode	Read mode	Read mode
3	Read mode	Autoselect mode	Read mode	Read mode
4	Read mode	Read mode	Autoselect mode	Read mode
5	Read mode	Read mode	Read mode	Autoselect mode
6	Program mode	Read mode	Read mode	Read mode
7	Read mode	Program mode	Read mode	Read mode
8	Read mode	Read mode	Program mode	Read mode
9	Read mode	Read mode	Read mode	Program mode
10	Erase Mode	Read mode	Read mode	Read mode
11	Read mode	Erase Mode	Read mode	Read mode
12	Read mode	Read mode	Erase Mode	Read mode
13	Read mode	Read mode	Read mode	Erase Mode
14*	Multiple Erase Mode	Multiple Erase Mode	Read mode	Read mode
15*	Multiple Erase Mode	Read mode	Multiple Erase Mode	Read mode
16*	Multiple Erase Mode	Read mode	Read mode	Multiple Erase Mode
17*	Read mode	Multiple Erase Mode	Multiple Erase Mode	Read mode
18*	Read mode	Multiple Erase Mode	Read mode	Multiple Erase Mode
19*	Read mode	Read mode	Multiple Erase Mode	Multiple Erase Mode
20*	Multiple Erase Mode	Multiple Erase Mode	Multiple Erase Mode	Read mode
21*	Multiple Erase Mode	Multiple Erase Mode	Read mode	Multiple Erase Mode
22*	Multiple Erase Mode	Read mode	Multiple Erase Mode	Multiple Erase Mode
23*	Read mode	Multiple Erase Mode	Multiple Erase Mode	Multiple Erase Mode

* : Multiple Erase Mode requires multiple sector erase sequence which is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}”.

2. Flexible Sector-erase Architecture

- **Sector Address Tables (Bank A) (128M Page Flash)**

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank A	SA0	0	1	0	0	0	0	0	0	0	0	0	0	4	000000h to 000FFFh
	SA1	0	1	0	0	0	0	0	0	0	0	0	1	4	001000h to 001FFFh
	SA2	0	1	0	0	0	0	0	0	0	0	1	0	4	002000h to 002FFFh
	SA3	0	1	0	0	0	0	0	0	0	0	1	1	4	003000h to 003FFFh
	SA4	0	1	0	0	0	0	0	0	0	1	0	0	4	004000h to 004FFFh
	SA5	0	1	0	0	0	0	0	0	0	1	0	1	4	005000h to 005FFFh
	SA6	0	1	0	0	0	0	0	0	0	1	1	0	4	006000h to 006FFFh
	SA7	0	1	0	0	0	0	0	0	0	1	1	1	4	007000h to 007FFFh
	SA8	0	1	0	0	0	0	0	0	1	X	X	X	32	008000h to 00FFFFh
	SA9	0	1	0	0	0	0	0	1	0	X	X	X	32	010000h to 017FFFh
	SA10	0	1	0	0	0	0	0	1	1	X	X	X	32	018000h to 01FFFFh
	SA11	0	1	0	0	0	0	1	0	0	X	X	X	32	020000h to 027FFFh
	SA12	0	1	0	0	0	0	1	0	1	X	X	X	32	028000h to 02FFFFh
	SA13	0	1	0	0	0	0	1	1	0	X	X	X	32	030000h to 037FFFh
	SA14	0	1	0	0	0	0	1	1	1	X	X	X	32	038000h to 03FFFFh
	SA15	0	1	0	0	0	1	0	0	0	X	X	X	32	040000h to 047FFFh
	SA16	0	1	0	0	0	1	0	0	1	X	X	X	32	048000h to 04FFFFh
	SA17	0	1	0	0	0	1	0	1	0	X	X	X	32	050000h to 057FFFh
	SA18	0	1	0	0	0	1	0	1	1	X	X	X	32	058000h to 05FFFFh
	SA19	0	1	0	0	0	1	1	0	0	X	X	X	32	060000h to 06FFFFh
	SA20	0	1	0	0	0	1	1	0	1	X	X	X	32	068000h to 06FFFFh
	SA21	0	1	0	0	0	1	1	1	0	X	X	X	32	070000h to 077FFFh
	SA22	0	1	0	0	0	1	1	1	1	X	X	X	32	078000h to 07FFFFh
	SA23	0	1	0	0	1	0	0	0	0	X	X	X	32	080000h to 087FFFh
	SA24	0	1	0	0	1	0	0	0	1	X	X	X	32	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	0	1	0	X	X	X	32	090000h to 097FFFh
	SA26	0	1	0	0	1	0	0	1	1	X	X	X	32	098000h to 09FFFFh
	SA27	0	1	0	0	1	0	1	0	0	X	X	X	32	0A0000h to 0A7FFFh
	SA28	0	1	0	0	1	0	1	0	1	X	X	X	32	0A8000h to 0AFFFFh
	SA29	0	1	0	0	1	0	1	1	0	X	X	X	32	0B0000h to 0B7FFFh
	SA30	0	1	0	0	1	0	1	1	1	X	X	X	32	0B8000h to 0BFFFFh
	SA31	0	1	0	0	1	1	0	0	0	X	X	X	32	0C0000h to 0C7FFFh
	SA32	0	1	0	0	1	1	0	0	1	X	X	X	32	0C8000h to 0CFFFFh
	SA33	0	1	0	0	1	1	0	1	0	X	X	X	32	0D0000h to 0D7FFFh
	SA34	0	1	0	0	1	1	0	1	1	X	X	X	32	0D8000h to 0DFFFFh
	SA35	0	1	0	0	1	1	1	0	0	X	X	X	32	0E0000h to 0E7FFFh
	SA36	0	1	0	0	1	1	1	0	1	X	X	X	32	0E8000h to 0EFFFFh
	SA37	0	1	0	0	1	1	1	1	0	X	X	X	32	0F0000h to 0F7FFFh
	SA38	0	1	0	0	1	1	1	1	1	X	X	X	32	0F8000h to 0FFFFFh

• **Sector Address Tables (Bank B) (128M Page Flash)**

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA39	0	1	0	1	0	0	0	0	0	X	X	X	32	100000h to 107FFFh
	SA40	0	1	0	1	0	0	0	0	1	X	X	X	32	108000h to 10FFFFh
	SA41	0	1	0	1	0	0	0	1	0	X	X	X	32	110000h to 117FFFh
	SA42	0	1	0	1	0	0	0	1	1	X	X	X	32	118000h to 11FFFFh
	SA43	0	1	0	1	0	0	1	0	0	X	X	X	32	120000h to 127FFFh
	SA44	0	1	0	1	0	0	1	0	1	X	X	X	32	128000h to 12FFFFh
	SA45	0	1	0	1	0	0	1	1	0	X	X	X	32	130000h to 137FFFh
	SA46	0	1	0	1	0	0	1	1	1	X	X	X	32	138000h to 13FFFFh
	SA47	0	1	0	1	0	1	0	0	0	X	X	X	32	140000h to 147FFFh
	SA48	0	1	0	1	0	1	0	0	1	X	X	X	32	148000h to 14FFFFh
	SA49	0	1	0	1	0	1	0	1	0	X	X	X	32	150000h to 157FFFh
	SA50	0	1	0	1	0	1	0	1	1	X	X	X	32	158000h to 15FFFFh
	SA51	0	1	0	1	0	1	1	0	0	X	X	X	32	160000h to 167FFFh
	SA52	0	1	0	1	0	1	1	0	1	X	X	X	32	168000h to 16FFFFh
	SA53	0	1	0	1	0	1	1	1	0	X	X	X	32	170000h to 177FFFh
	SA54	0	1	0	1	0	1	1	1	1	X	X	X	32	178000h to 17FFFFh
	SA55	0	1	0	1	1	0	0	0	0	X	X	X	32	180000h to 187FFFh
	SA56	0	1	0	1	1	0	0	0	1	X	X	X	32	188000h to 18FFFFh
	SA57	0	1	0	1	1	0	0	1	0	X	X	X	32	190000h to 197FFFh
	SA58	0	1	0	1	1	0	0	1	1	X	X	X	32	198000h to 19FFFFh
	SA59	0	1	0	1	1	0	1	0	0	X	X	X	32	1A0000h to 1A7FFFh
	SA60	0	1	0	1	1	0	1	0	1	X	X	X	32	1A8000h to 1AFFFFh
	SA61	0	1	0	1	1	0	1	1	0	X	X	X	32	1B0000h to 1B7FFFh
	SA62	0	1	0	1	1	0	1	1	1	X	X	X	32	1B8000h to 1BFFFFh
	SA63	0	1	0	1	1	1	0	0	0	X	X	X	32	1C0000h to 1C7FFFh
	SA64	0	1	0	1	1	1	0	0	1	X	X	X	32	1C8000h to 1CFFFFh
	SA65	0	1	0	1	1	1	0	1	0	X	X	X	32	1D0000h to 1D7FFFh
	SA66	0	1	0	1	1	1	0	1	1	X	X	X	32	1D8000h to 1DFFFFh
	SA67	0	1	0	1	1	1	1	0	0	X	X	X	32	1E0000h to 1E7FFFh
	SA68	0	1	0	1	1	1	1	0	1	X	X	X	32	1E8000h to 1EFFFFh
	SA69	0	1	0	1	1	1	1	1	0	X	X	X	32	1F0000h to 1F7FFFh
	SA70	0	1	0	1	1	1	1	1	1	X	X	X	32	1F8000h to 1FFFFFh
	SA71	0	1	1	0	0	0	0	0	0	X	X	X	32	200000h to 207FFFh
	SA72	0	1	1	0	0	0	0	0	1	X	X	X	32	208000h to 20FFFFh
	SA73	0	1	1	0	0	0	0	1	0	X	X	X	32	210000h to 217FFFh
	SA74	0	1	1	0	0	0	0	1	1	X	X	X	32	218000h to 21FFFFh
	SA75	0	1	1	0	0	0	1	0	0	X	X	X	32	220000h to 227FFFh
	SA76	0	1	1	0	0	0	1	0	1	X	X	X	32	228000h to 22FFFFh
	SA77	0	1	1	0	0	0	1	1	0	X	X	X	32	230000h to 237FFFh

(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA78	0	1	1	0	0	0	1	1	1	X	X	X	32	238000h to 23FFFFh
	SA79	0	1	1	0	0	1	0	0	0	X	X	X	32	240000h to 247FFFh
	SA80	0	1	1	0	0	1	0	0	1	X	X	X	32	248000h to 24FFFFh
	SA81	0	1	1	0	0	1	0	1	0	X	X	X	32	250000h to 257FFFh
	SA82	0	1	1	0	0	1	0	1	1	X	X	X	32	258000h to 25FFFFh
	SA83	0	1	1	0	0	1	1	0	0	X	X	X	32	260000h to 267FFFh
	SA84	0	1	1	0	0	1	1	0	1	X	X	X	32	268000h to 26FFFFh
	SA85	0	1	1	0	0	1	1	1	0	X	X	X	32	270000h to 277FFFh
	SA86	0	1	1	0	0	1	1	1	1	X	X	X	32	278000h to 27FFFFh
	SA87	0	1	1	0	1	0	0	0	0	X	X	X	32	280000h to 287FFFh
	SA88	0	1	1	0	1	0	0	0	1	X	X	X	32	288000h to 28FFFFh
	SA89	0	1	1	0	1	0	0	1	0	X	X	X	32	290000h to 297FFFh
	SA90	0	1	1	0	1	0	0	1	1	X	X	X	32	298000h to 29FFFFh
	SA91	0	1	1	0	1	0	1	0	0	X	X	X	32	2A0000h to 2A7FFFh
	SA92	0	1	1	0	1	0	1	0	1	X	X	X	32	2A8000h to 2AFFFFh
	SA93	0	1	1	0	1	0	1	1	0	X	X	X	32	2B0000h to 2B7FFFh
	SA94	0	1	1	0	1	0	1	1	1	X	X	X	32	2B8000h to 2BFFFFh
	SA95	0	1	1	0	1	1	0	0	0	X	X	X	32	2C0000h to 2C7FFFh
	SA96	0	1	1	0	1	1	0	0	1	X	X	X	32	2C8000h to 2CFFFFh
	SA97	0	1	1	0	1	1	0	1	0	X	X	X	32	2D0000h to 2D7FFFh
	SA98	0	1	1	0	1	1	0	1	1	X	X	X	32	2D8000h to 2DFFFFh
	SA99	0	1	1	0	1	1	1	0	0	X	X	X	32	2E0000h to 2E7FFFh
	SA100	0	1	1	0	1	1	1	0	1	X	X	X	32	2E8000h to 2EFFFFh
	SA101	0	1	1	0	1	1	1	1	0	X	X	X	32	2F0000h to 2F7FFFh
	SA102	0	1	1	0	1	1	1	1	1	X	X	X	32	2F8000h to 2FFFFFh
	SA103	0	1	1	1	0	0	0	0	0	X	X	X	32	300000h to 307FFFh
	SA104	0	1	1	1	0	0	0	0	1	X	X	X	32	308000h to 30FFFFh
	SA105	0	1	1	1	0	0	0	1	0	X	X	X	32	310000h to 317FFFh
	SA106	0	1	1	1	0	0	0	1	1	X	X	X	32	318000h to 31FFFFh
	SA107	0	1	1	1	0	0	1	0	0	X	X	X	32	320000h to 327FFFh
	SA108	0	1	1	1	0	0	1	0	1	X	X	X	32	328000h to 32FFFFh
	SA109	0	1	1	1	0	0	1	1	0	X	X	X	32	330000h to 337FFFh
	SA110	0	1	1	1	0	0	1	1	1	X	X	X	32	338000h to 33FFFFh
	SA111	0	1	1	1	0	1	0	0	0	X	X	X	32	340000h to 347FFFh
	SA112	0	1	1	1	0	1	0	0	1	X	X	X	32	348000h to 34FFFFh
	SA113	0	1	1	1	0	1	0	1	0	X	X	X	32	350000h to 357FFFh
	SA114	0	1	1	1	0	1	0	1	1	X	X	X	32	358000h to 35FFFFh
	SA115	0	1	1	1	0	1	1	0	0	X	X	X	32	360000h to 367FFFh
	SA116	0	1	1	1	0	1	1	0	1	X	X	X	32	368000h to 36FFFFh

(Continued)

(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA117	0	1	1	1	0	1	1	1	0	X	X	X	32	370000h to 377FFFh
	SA118	0	1	1	1	0	1	1	1	1	X	X	X	32	378000h to 37FFFFh
	SA119	0	1	1	1	1	0	0	0	0	X	X	X	32	380000h to 387FFFh
	SA120	0	1	1	1	1	0	0	0	1	X	X	X	32	388000h to 38FFFFh
	SA121	0	1	1	1	1	0	0	1	0	X	X	X	32	390000h to 397FFFh
	SA122	0	1	1	1	1	0	0	1	1	X	X	X	32	398000h to 39FFFFh
	SA123	0	1	1	1	1	0	1	0	0	X	X	X	32	3A0000h to 3A7FFFh
	SA124	0	1	1	1	1	0	1	0	1	X	X	X	32	3A8000h to 3AFFFFh
	SA125	0	1	1	1	1	0	1	1	0	X	X	X	32	3B0000h to 3B7FFFh
	SA126	0	1	1	1	1	0	1	1	1	X	X	X	32	3B8000h to 3BFFFFh
	SA127	0	1	1	1	1	1	0	0	0	X	X	X	32	3C0000h to 3C7FFFh
	SA128	0	1	1	1	1	1	0	0	1	X	X	X	32	3C8000h to 3CFFFFh
	SA129	0	1	1	1	1	1	0	1	0	X	X	X	32	3D0000h to 3D7FFFh
	SA130	0	1	1	1	1	1	0	1	1	X	X	X	32	3D8000h to 3DFFFFh
	SA131	0	1	1	1	1	1	1	0	0	X	X	X	32	3E0000h to 3E7FFFh
	SA132	0	1	1	1	1	1	1	0	1	X	X	X	32	3E8000h to 3EFFFFh
	SA133	0	1	1	1	1	1	1	1	0	X	X	X	32	3F0000h to 3F7FFFh
	SA134	0	1	1	1	1	1	1	1	1	X	X	X	32	3F8000h to 3FFFFFh

- **Sector Address Tables (Bank C) (128M Page Flash)**

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA135	1	0	0	0	0	0	0	0	0	X	X	X	32	400000h to 407FFFh
	SA136	1	0	0	0	0	0	0	0	1	X	X	X	32	408000h to 40FFFFh
	SA137	1	0	0	0	0	0	0	1	0	X	X	X	32	410000h to 417FFFh
	SA138	1	0	0	0	0	0	0	1	1	X	X	X	32	418000h to 41FFFFh
	SA139	1	0	0	0	0	0	1	0	0	X	X	X	32	420000h to 427FFFh
	SA140	1	0	0	0	0	0	1	0	1	X	X	X	32	428000h to 42FFFFh
	SA141	1	0	0	0	0	0	1	1	0	X	X	X	32	430000h to 437FFFh
	SA142	1	0	0	0	0	0	1	1	1	X	X	X	32	438000h to 43FFFFh
	SA143	1	0	0	0	0	1	0	0	0	X	X	X	32	440000h to 447FFFh
	SA144	1	0	0	0	0	1	0	0	1	X	X	X	32	448000h to 44FFFFh
	SA145	1	0	0	0	0	1	0	1	0	X	X	X	32	450000h to 457FFFh
	SA146	1	0	0	0	0	1	0	1	1	X	X	X	32	458000h to 45FFFFh
	SA147	1	0	0	0	0	1	1	0	0	X	X	X	32	460000h to 467FFFh
	SA148	1	0	0	0	0	1	1	0	1	X	X	X	32	468000h to 46FFFFh
	SA149	1	0	0	0	0	1	1	1	0	X	X	X	32	470000h to 477FFFh
	SA150	1	0	0	0	0	1	1	1	1	X	X	X	32	478000h to 47FFFFh
	SA151	1	0	0	0	1	0	0	0	0	X	X	X	32	480000h to 487FFFh
	SA152	1	0	0	0	1	0	0	0	1	X	X	X	32	488000h to 48FFFFh
	SA153	1	0	0	0	1	0	0	1	0	X	X	X	32	490000h to 497FFFh
	SA154	1	0	0	0	1	0	0	1	1	X	X	X	32	498000h to 49FFFFh
	SA155	1	0	0	0	1	0	1	0	0	X	X	X	32	4A0000h to 4A7FFFh
	SA156	1	0	0	0	1	0	1	0	1	X	X	X	32	4A8000h to 4AFFFFh
	SA157	1	0	0	0	1	0	1	1	0	X	X	X	32	4B0000h to 4B7FFFh
	SA158	1	0	0	0	1	0	1	1	1	X	X	X	32	4B8000h to 4BFFFFh
	SA159	1	0	0	0	1	1	0	0	0	X	X	X	32	4C0000h to 4C7FFFh
	SA160	1	0	0	0	1	1	0	0	1	X	X	X	32	4C8000h to 4CFFFFh
	SA161	1	0	0	0	1	1	0	1	0	X	X	X	32	4D0000h to 4D7FFFh
	SA162	1	0	0	0	1	1	0	1	1	X	X	X	32	4D8000h to 4DFFFFh
	SA163	1	0	0	0	1	1	1	0	0	X	X	X	32	4E0000h to 4E7FFFh
	SA164	1	0	0	0	1	1	1	0	1	X	X	X	32	4E8000h to 4EFFFFh
	SA165	1	0	0	0	1	1	1	1	0	X	X	X	32	4F0000h to 4F7FFFh
	SA166	1	0	0	0	1	1	1	1	1	X	X	X	32	4F8000h to 4FFFFFh
	SA167	1	0	0	1	0	0	0	0	0	X	X	X	32	500000h to 507FFFh
	SA168	1	0	0	1	0	0	0	0	1	X	X	X	32	508000h to 50FFFFh
	SA169	1	0	0	1	0	0	0	1	0	X	X	X	32	510000h to 517FFFh
	SA170	1	0	0	1	0	0	0	1	1	X	X	X	32	518000h to 51FFFFh
	SA171	1	0	0	1	0	0	1	0	0	X	X	X	32	520000h to 527FFFh
	SA172	1	0	0	1	0	0	1	0	1	X	X	X	32	528000h to 52FFFFh
	SA173	1	0	0	1	0	0	1	1	0	X	X	X	32	530000h to 537FFFh

(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA174	1	0	0	1	0	0	1	1	1	X	X	X	32	538000h to 53FFFFh
	SA175	1	0	0	1	0	1	0	0	0	X	X	X	32	540000h to 547FFFh
	SA176	1	0	0	1	0	1	0	0	1	X	X	X	32	548000h to 54FFFFh
	SA177	1	0	0	1	0	1	0	1	0	X	X	X	32	550000h to 557FFFh
	SA178	1	0	0	1	0	1	0	1	1	X	X	X	32	558000h to 55FFFFh
	SA179	1	0	0	1	0	1	1	0	0	X	X	X	32	560000h to 567FFFh
	SA180	1	0	0	1	0	1	1	0	1	X	X	X	32	568000h to 56FFFFh
	SA181	1	0	0	1	0	1	1	1	0	X	X	X	32	570000h to 577FFFh
	SA182	1	0	0	1	0	1	1	1	1	X	X	X	32	578000h to 57FFFFh
	SA183	1	0	0	1	1	0	0	0	0	X	X	X	32	580000h to 587FFFh
	SA184	1	0	0	1	1	0	0	0	1	X	X	X	32	588000h to 58FFFFh
	SA185	1	0	0	1	1	0	0	1	0	X	X	X	32	590000h to 597FFFh
	SA186	1	0	0	1	1	0	0	1	1	X	X	X	32	598000h to 59FFFFh
	SA187	1	0	0	1	1	0	1	0	0	X	X	X	32	5A0000h to 5A7FFFh
	SA188	1	0	0	1	1	0	1	0	1	X	X	X	32	5A8000h to 5AFFFFh
	SA189	1	0	0	1	1	0	1	1	0	X	X	X	32	5B0000h to 5B7FFFh
	SA190	1	0	0	1	1	0	1	1	1	X	X	X	32	5B8000h to 5BFFFFh
	SA191	1	0	0	1	1	1	0	0	0	X	X	X	32	5C0000h to 5C7FFFh
	SA192	1	0	0	1	1	1	0	0	1	X	X	X	32	5C8000h to 5CFFFFh
	SA193	1	0	0	1	1	1	0	1	0	X	X	X	32	6D0000h to 5D7FFFh
	SA194	1	0	0	1	1	1	0	1	1	X	X	X	32	6D8000h to 5DFFFFh
	SA195	1	0	0	1	1	1	1	0	0	X	X	X	32	5E0000h to 5E7FFFh
	SA196	1	0	0	1	1	1	1	0	1	X	X	X	32	5E8000h to 5EFFFFh
	SA197	1	0	0	1	1	1	1	1	0	X	X	X	32	5F0000h to 5F7FFFh
	SA198	1	0	0	1	1	1	1	1	1	X	X	X	32	5F8000h to 5FFFFFh
	SA199	1	0	1	0	0	0	0	0	0	X	X	X	32	600000h to 607FFFh
	SA200	1	0	1	0	0	0	0	0	1	X	X	X	32	608000h to 60FFFFh
	SA201	1	0	1	0	0	0	0	1	0	X	X	X	32	610000h to 617FFFh
	SA202	1	0	1	0	0	0	0	1	1	X	X	X	32	618000h to 61FFFFh
	SA203	1	0	1	0	0	0	1	0	0	X	X	X	32	620000h to 627FFFh
	SA204	1	0	1	0	0	0	1	0	1	X	X	X	32	628000h to 62FFFFh
	SA205	1	0	1	0	0	0	1	1	0	X	X	X	32	630000h to 637FFFh
	SA206	1	0	1	0	0	0	1	1	1	X	X	X	32	638000h to 63FFFFh
	SA207	1	0	1	0	0	1	0	0	0	X	X	X	32	640000h to 647FFFh
	SA208	1	0	1	0	0	1	0	0	1	X	X	X	32	648000h to 64FFFFh
	SA209	1	0	1	0	0	1	0	1	0	X	X	X	32	650000h to 657FFFh
	SA210	1	0	1	0	0	1	0	1	1	X	X	X	32	658000h to 65FFFFh
	SA211	1	0	1	0	0	1	1	0	0	X	X	X	32	660000h to 667FFFh
	SA212	1	0	1	0	0	1	1	0	1	X	X	X	32	668000h to 66FFFFh

(Continued)

(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA213	1	0	1	0	0	1	1	1	0	X	X	X	32	670000h to 677FFFh
	SA214	1	0	1	0	0	1	1	1	1	X	X	X	32	678000h to 67FFFFh
	SA215	1	0	1	0	1	0	0	0	0	X	X	X	32	680000h to 687FFFh
	SA216	1	0	1	0	1	0	0	0	1	X	X	X	32	688000h to 68FFFFh
	SA217	1	0	1	0	1	0	0	1	0	X	X	X	32	690000h to 697FFFh
	SA218	1	0	1	0	1	0	0	1	1	X	X	X	32	698000h to 69FFFFh
	SA219	1	0	1	0	1	0	1	0	0	X	X	X	32	6A0000h to 6A7FFFh
	SA220	1	0	1	0	1	0	1	0	1	X	X	X	32	6A8000h to 6AFFFFh
	SA221	1	0	1	0	1	0	1	1	0	X	X	X	32	6B0000h to 6B7FFFh
	SA222	1	0	1	0	1	0	1	1	1	X	X	X	32	8B8000h to 6BFFFFh
	SA223	1	0	1	0	1	1	0	0	0	X	X	X	32	6C0000h to 6C7FFFh
	SA224	1	0	1	0	1	1	0	0	1	X	X	X	32	6C8000h to 6CFFFFh
	SA225	1	0	1	0	1	1	0	1	0	X	X	X	32	6D0000h to 6D7FFFh
	SA226	1	0	1	0	1	1	0	1	1	X	X	X	32	6D8000h to 6DFFFFh
	SA227	1	0	1	0	1	1	1	0	0	X	X	X	32	6E0000h to 6E7FFFh
	SA228	1	0	1	0	1	1	1	0	1	X	X	X	32	6E8000h to 6EFFFFh
	SA229	1	0	1	0	1	1	1	1	0	X	X	X	32	6F0000h to 6F7FFFh
	SA230	1	0	1	0	1	1	1	1	1	X	X	X	32	6F8000h to 6FFFFFh

- **Sector Address Tables (Bank D) (128M Page Flash)**

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kword)	(× 16) Address Range
				Bank Address											
		$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank D	SA231	1	0	1	1	0	0	0	0	0	X	X	X	32	700000h to 707FFFh
	SA232	1	0	1	1	0	0	0	0	1	X	X	X	32	708000h to 70FFFFh
	SA233	1	0	1	1	0	0	0	1	0	X	X	X	32	710000h to 717FFFh
	SA234	1	0	1	1	0	0	0	1	1	X	X	X	32	718000h to 71FFFFh
	SA235	1	0	1	1	0	0	1	0	0	X	X	X	32	720000h to 727FFFh
	SA236	1	0	1	1	0	0	1	0	1	X	X	X	32	728000h to 72FFFFh
	SA237	1	0	1	1	0	0	1	1	0	X	X	X	32	730000h to 737FFFh
	SA238	1	0	1	1	0	0	1	1	1	X	X	X	32	738000h to 73FFFFh
	SA239	1	0	1	1	0	1	0	0	0	X	X	X	32	740000h to 747FFFh
	SA240	1	0	1	1	0	1	0	0	1	X	X	X	32	748000h to 74FFFFh
	SA241	1	0	1	1	0	1	0	1	0	X	X	X	32	750000h to 757FFFh
	SA242	1	0	1	1	0	1	0	1	1	X	X	X	32	758000h to 75FFFFh
	SA243	1	0	1	1	0	1	1	0	0	X	X	X	32	760000h to 767FFFh
	SA244	1	0	1	1	0	1	1	0	1	X	X	X	32	768000h to 76FFFFh
	SA245	1	0	1	1	0	1	1	1	0	X	X	X	32	770000h to 777FFFh
	SA246	1	0	1	1	0	1	1	1	1	X	X	X	32	778000h to 77FFFFh
	SA247	1	0	1	1	1	0	0	0	0	X	X	X	32	780000h to 787FFFh
	SA248	1	0	1	1	1	0	0	0	1	X	X	X	32	788000h to 78FFFFh
	SA249	1	0	1	1	1	0	0	1	0	X	X	X	32	790000h to 797FFFh
	SA250	1	0	1	1	1	0	0	1	1	X	X	X	32	798000h to 79FFFFh
	SA251	1	0	1	1	1	0	1	0	0	X	X	X	32	7A0000h to 7A7FFFh
	SA252	1	0	1	1	1	0	1	0	1	X	X	X	32	7A8000h to 7AFFFFh
	SA253	1	0	1	1	1	0	1	1	0	X	X	X	32	7B0000h to 7B7FFFh
	SA254	1	0	1	1	1	0	1	1	1	X	X	X	32	7B8000h to 7BFFFFh
	SA255	1	0	1	1	1	1	0	0	0	X	X	X	32	7C0000h to 7C7FFFh
	SA256	1	0	1	1	1	1	0	0	1	X	X	X	32	7C8000h to 7CFFFFh
	SA257	1	0	1	1	1	1	0	1	0	X	X	X	32	7D0000h to 7D7FFFh
	SA258	1	0	1	1	1	1	0	1	1	X	X	X	32	7D8000h to 7DFFFFh
	SA259	1	0	1	1	1	1	1	0	0	X	X	X	32	7E0000h to 7E7FFFh
	SA260	1	0	1	1	1	1	1	0	1	X	X	X	32	7E8000h to 7EFFFFh
	SA261	1	0	1	1	1	1	1	1	0	X	X	X	32	7F0000h to 7F7FFFh
	SA262	1	0	1	1	1	1	1	1	1	0	0	0	4	7F8000h to 7F8FFFh
	SA263	1	0	1	1	1	1	1	1	1	0	0	1	4	7F9000h to 7F9FFFh
	SA264	1	0	1	1	1	1	1	1	1	0	1	0	4	7FA000h to 7FAFFFh
	SA265	1	0	1	1	1	1	1	1	1	0	1	1	4	7FB000h to 7FBFFFh
	SA266	1	0	1	1	1	1	1	1	1	1	0	0	4	7FC000h to 7FCFFFh
	SA267	1	0	1	1	1	1	1	1	1	1	0	1	4	7FD000h to 7FDFFFh
	SA268	1	0	1	1	1	1	1	1	1	1	1	0	4	7FE000h to 7FEFFFh
	SA269	1	0	1	1	1	1	1	1	1	1	1	1	4	7FF000h to 7FFFFFh

- **Sector Group Address Table (128M Page Flash)**

Sector Group	$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	1	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	1	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	1	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	1	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	1	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	1	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	1	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	1	0	0	0	0	0	0	1	X	X	X	SA8
SGA9	0	1	0	0	0	0	0	1	0	X	X	X	SA9
SGA10	0	1	0	0	0	0	0	1	1	X	X	X	SA10
SGA11	0	1	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA12	0	1	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA13	0	1	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA14	0	1	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA15	0	1	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA16	0	1	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA17	0	1	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA18	0	1	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA19	0	1	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA20	0	1	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA21	0	1	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA22	0	1	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA23	0	1	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA24	0	1	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA25	0	1	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA26	0	1	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA27	0	1	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA28	0	1	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA29	0	1	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA30	0	1	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA31	0	1	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA32	0	1	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA33	0	1	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA34	0	1	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA35	0	1	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA36	0	1	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA37	0	1	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA38	0	1	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA39	0	1	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA40	0	1	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA41	0	1	1	1	1	1	1	X	X	X	X	X	SA131 to SA134

(Continued)

(Continued)

Sector Group	$\overline{CE}$0f	$\overline{CE}$1f	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA42	1	0	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA43	1	0	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA44	1	0	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA45	1	0	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA46	1	0	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA47	1	0	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA48	1	0	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA49	1	0	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA50	1	0	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA51	1	0	0	1	0	0	1	X	X	X	X	X	SA171 to SA174
SGA52	1	0	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA53	1	0	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA54	1	0	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA55	1	0	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA56	1	0	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA57	1	0	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA58	1	0	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA59	1	0	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA60	1	0	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA61	1	0	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA62	1	0	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA63	1	0	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA64	1	0	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA65	1	0	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA66	1	0	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA67	1	0	1	1	0	0	1	X	X	X	X	X	SA235 to SA238
SGA68	1	0	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA69	1	0	1	1	0	1	1	X	X	X	X	X	SA243 to SA246
SGA70	1	0	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA71	1	0	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA72	1	0	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA73	1	0	1	1	1	1	1	0	0	X	X	X	SA259
SGA74	1	0	1	1	1	1	1	0	1	X	X	X	SA260
SGA75	1	0	1	1	1	1	1	1	0	X	X	X	SA261
SGA76	1	0	1	1	1	1	1	1	1	0	0	0	SA262
SGA77	1	0	1	1	1	1	1	1	1	0	0	1	SA263
SGA78	1	0	1	1	1	1	1	1	1	0	1	0	SA264
SGA79	1	0	1	1	1	1	1	1	1	0	1	1	SA265
SGA80	1	0	1	1	1	1	1	1	1	1	0	0	SA266
SGA81	1	0	1	1	1	1	1	1	1	1	0	1	SA267
SGA82	1	0	1	1	1	1	1	1	1	1	1	0	SA268
SGA83	1	0	1	1	1	1	1	1	1	1	1	1	SA269

- **Sector Group Protection Verify Autoselect Codes (128M Page Flash)**

Type	A_{22} to A_{12}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	X	X	L	L	L	L	04h
Device Code	BA	L	L	X	X	L	L	L	H	227Eh
Extended Device Code*2	BA	L	L	X	X	H	H	H	L	2221h
		L	L	X	X	H	H	H	H	2200h
Sector Group Protection	Sector Group Addresses	L	L	L	L	L	L	H	L	01h*1

Legend: L = V_{IL}, H = V_{IH}, X= V_{IL} or V_{IH}

*1 : Sector Group can be protected by "Extended Sector Group Protection", and "New Sector Protection (PPB Protection)". Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

- **Command Definitions (128M Page Flash)**

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
Program/Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SGA+ WPH	60h	SGA+ WPH	40h	SGA+ WPH	SD	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—	—	—
HiddenROM Program *3	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—	—	—
HiddenROM Exit *3	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—	—	—
HiddenROM Protect *3	6	555h	AAh	2AAh	55h	555h	60h	OPBP	68h	OPBP	48h	OPBP	RD(0)	—	—
Password Program	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0	—	—	—	—	—	—
		555h	AAh	2AAh	55h	555h	38h	XX1h	PD1						
		555h	AAh	2AAh	55h	555h	38h	XX2h	PD2						
		555h	AAh	2AAh	55h	555h	38h	XX3h	PD3						
Password Unlock	7	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0	XX1h	PD1	XX2h	PD2	XX3h	PD3
Password Verify	4	555h	AAh	2AAh	55h	555h	C8h	PWA	PWD	—	—	—	—	—	—
Password Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	PL	68h	PL	48h	XXXh	RD(0)	—	—
Persistent Protection Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	SPML	68h	SPML	48h	XXXh	RD(0)	—	—
PPB Program	6	555h	AAh	2AAh	55h	555h	60h	SGA+WP	68h	SGA+WP	48h	XXXh	RD(0)	—	—
PPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	90h	SGA+WP	RD(0)	—	—	—	—	—	—
All PPB Erase	4	555h	AAh	2AAh	55h	555h	60h	WP	60h	SGA+WP	40h	XXXh	RD(0)	—	—
PPB Lock Bit Set	3	555h	AAh	2AAh	55h	555h	78h	—	—	—	—	—	—	—	—
PPB Lock Bit Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD(1)	—	—	—	—	—	—
DPB Write	4	555h	AAh	2AAh	55h	555h	48h	SA	X1h	—	—	—	—	—	—
DPB Erase	4	555h	AAh	2AAh	55h	555h	48h	SA	X0h	—	—	—	—	—	—
DPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD(0)	—	—	—	—	—	—

(Continued)

(Continued)

Legend:

RA = Address of the memory location to be read

PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12} will uniquely select any sector.

BA = Bank Address. Address settled by A_{22}, A_{21}, A_{20}, A_{19} will select Bank A, Bank B, Bank C and Bank D.

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.

SGA = Sector group address to be protected.

WPH = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 0, 0, 1, 0)

SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

HRA = Address of the HiddenROM area Word Mode : 000000h to 00007Fh

HRBA = Bank Address of the HiddenROM area (A_{22} = A_{21} = A_{20} = V_{IL})

RD (0) = Read Data bit. If protected, DQ_0 = 1, if unprotected, DQ_0 = 0

RD (1) = Read Data bit. If protected, DQ_1 = 1, if unprotected, DQ_1 = 0

OPBP = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 1, 1, 0, 1, 0)

PWA/PWD = Password Address/Password Data

PL = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 1, 0, 1, 0)

SPML = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 1, 0, 0, 1, 0)

WP = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 0, 0, 1, 0)

*1: This command is valid during Fast Mode.

*2: This command is valid while $\overline{\text{RESET}}$ = V_{ID}.

*3: This command is valid during HiddenROM mode.

*4: The data “00h” is also acceptable.

Notes :
- Address bits A_{22} to A_{11} = X = “H” or “L” for all address commands except for PA, SA, BA, SGA, OPBP, PWA, PL, SPML, WP, WPH.
- Bus operations are defined in this document.
- The system should generate the following address patterns:
  Word Mode : 555h or 2AAh to addresses A_{10} to A_0
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

3. AC Characteristics

- **Read Only Operations Characteristics (Flash) (128M Page Flash)**

Parameter	Symbol		Test Setup	Value*		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
Page Read Cycle Time	—	t_{PRC}	—	20	—	ns
Page Address to Output Delay	—	t_{PACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	20	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	20	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	20	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	20	ns
Output Hold Time From Address, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	5	—	ns

* : Test Conditions– Output Load : 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to $V_{CC}f$
Timing measurement reference level
Input: $0.5 \times V_{CC}f$
Output: $0.5 \times V_{CC}f$

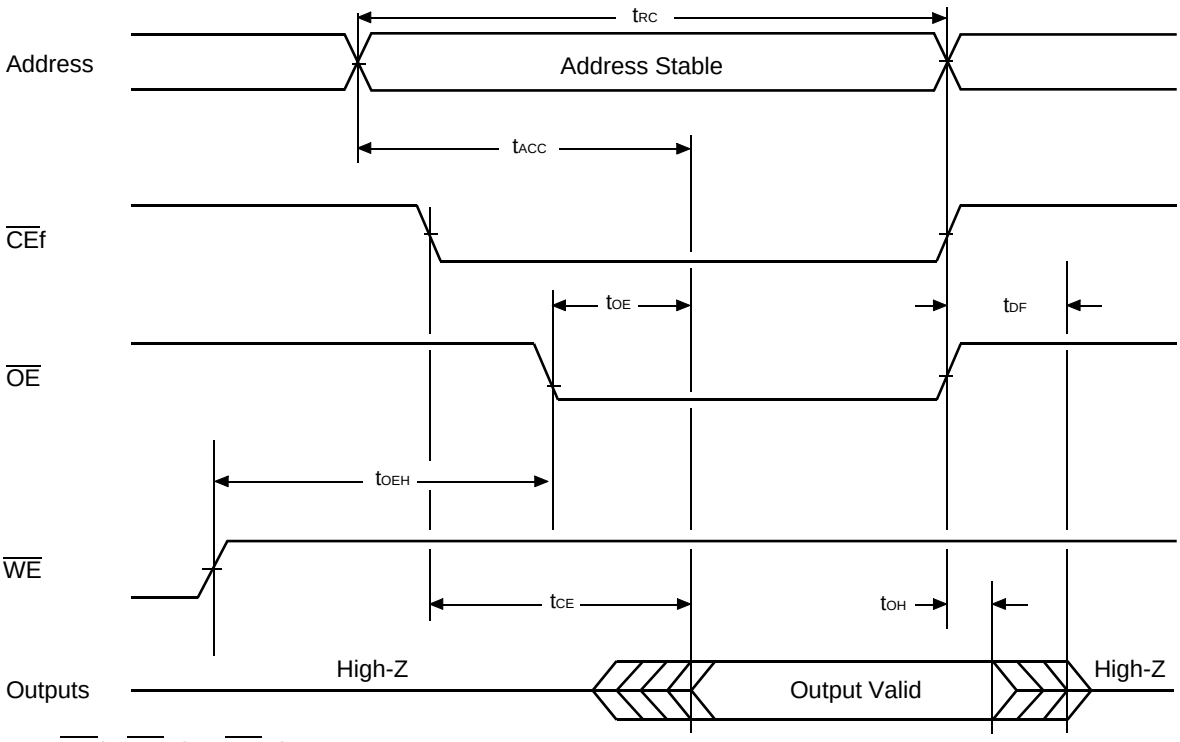
- **Write/Erase/Program Operations (Flash) (128M Page Flash)**

Parameter		Symbol		Value*1			Unit
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	70	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	15	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	35	—	—	ns
Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	30	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$f Low)		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CE}$f Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$f Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	40	—	—	ns
$\overline{CE}$f Pulse Width		t_{ELEH}	t_{CP}	40	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	25	—	—	ns
$\overline{CE}$f Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	ns
Programming Operation		t_{WHWH1}	t_{WHWH1}	—	6	—	µs
Sector Erase Operation *2		t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
V_{CC}f Setup Time		—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID} *3		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC} *4		—	t_{VACCR}	500	—	—	ns
Voltage Transition Time *3		—	t_{VLHT}	4	—	—	µs
Write Pulse Width*3		—	t_{WPP}	100	—	—	µs
Recover Time from RY/$\overline{BY}$		—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width		—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Level Period Before Read		—	t_{RH}	50	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable		—	t_{EOE}	—	—	70	ns
Erase Time-out Time		—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time		—	t_{SPD}	—	—	20	µs

*1 : Test Conditions– Output Load : 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to V_{CC}f
Timing measurement reference level
Input: 0.5×V_{CC}f
Output: 0.5×V_{CC}f

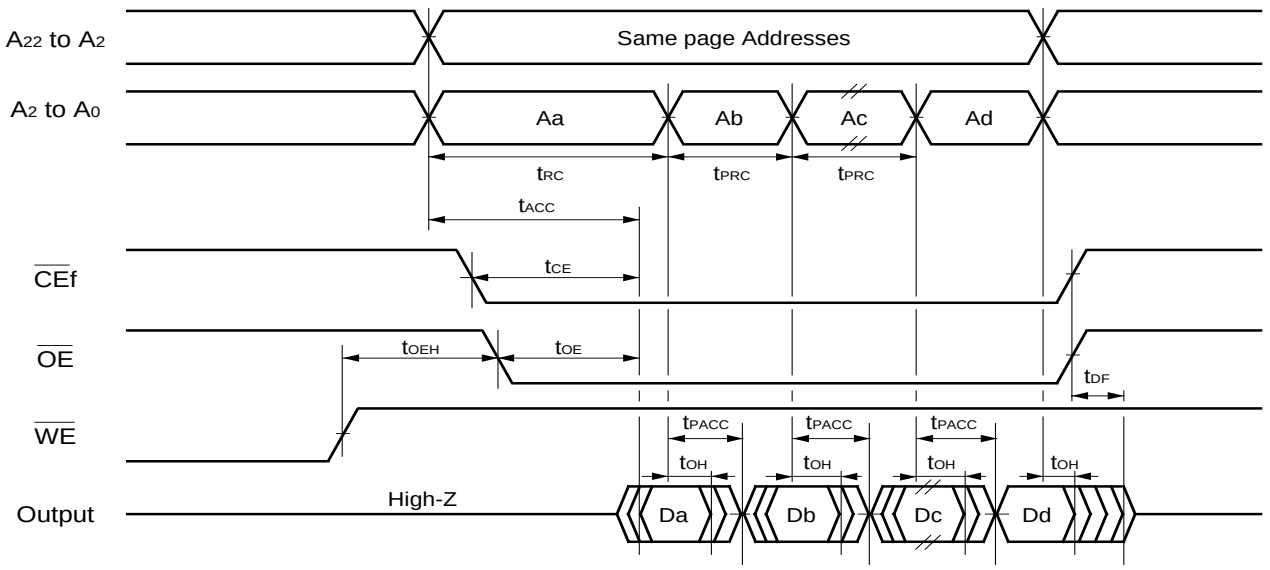
*2 : This does not include the preprogramming time.
*3 : This timing is for Sector Group Protection / Unprotection.
*4 : This timing is for Accelerated Program operation.

• Read Operation Timing Diagram (128M Page Flash)



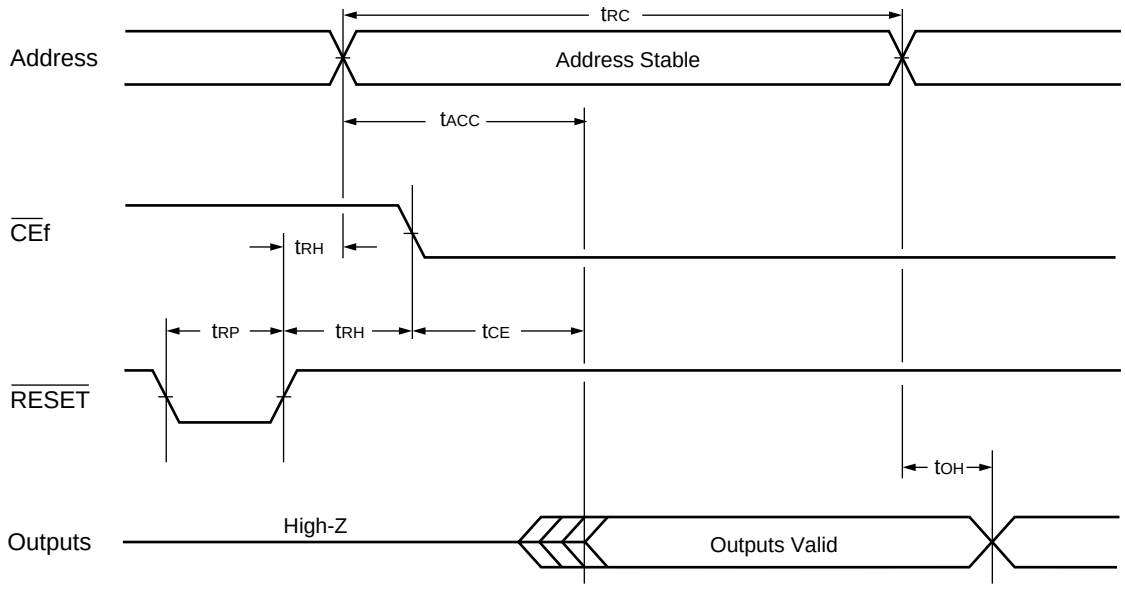
CEf : CE0f or CE1f

- **Page Read Operation Timing Diagram (128M Page Flash)**



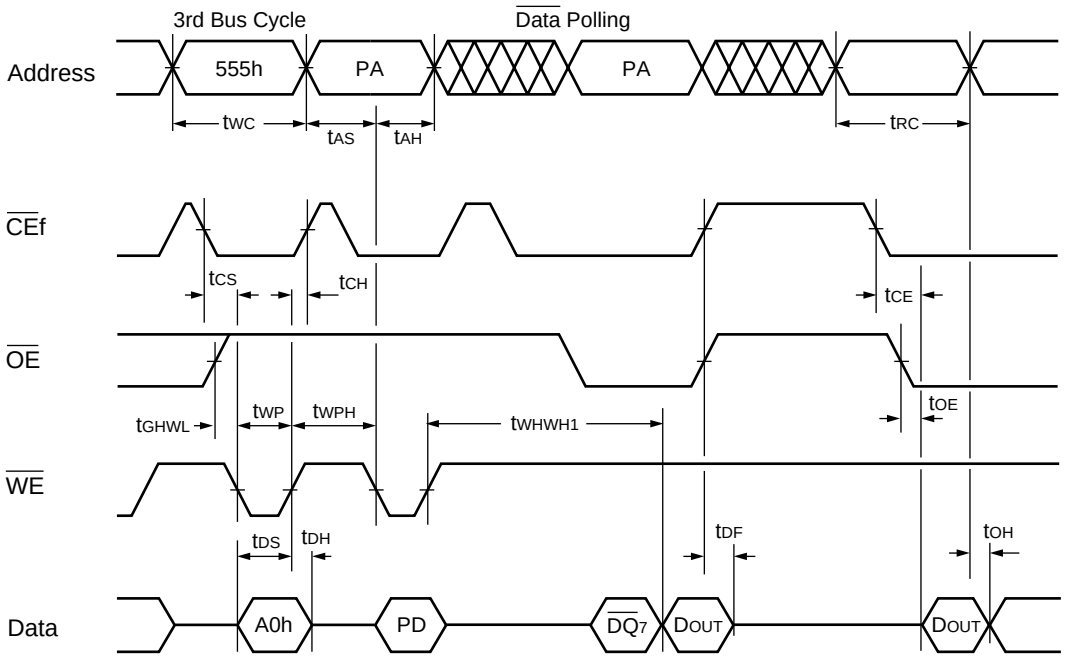
$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

- **Hardware Reset/Read Operation Timing Diagram (128M Page Flash)**



$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

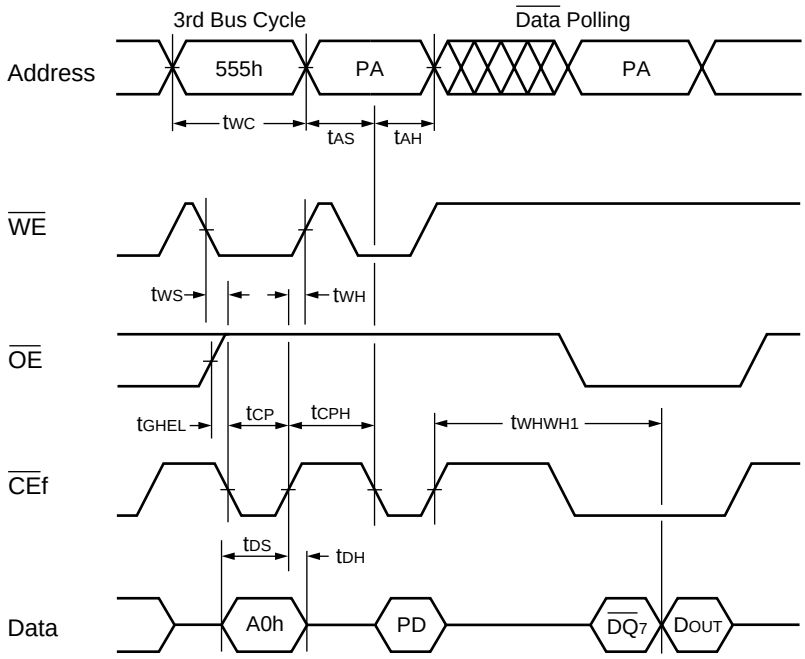
- **Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram (128M Page Flash)**



$\overline{CE}f$: $\overline{CE}0f$ or $\overline{CE}1f$

Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.

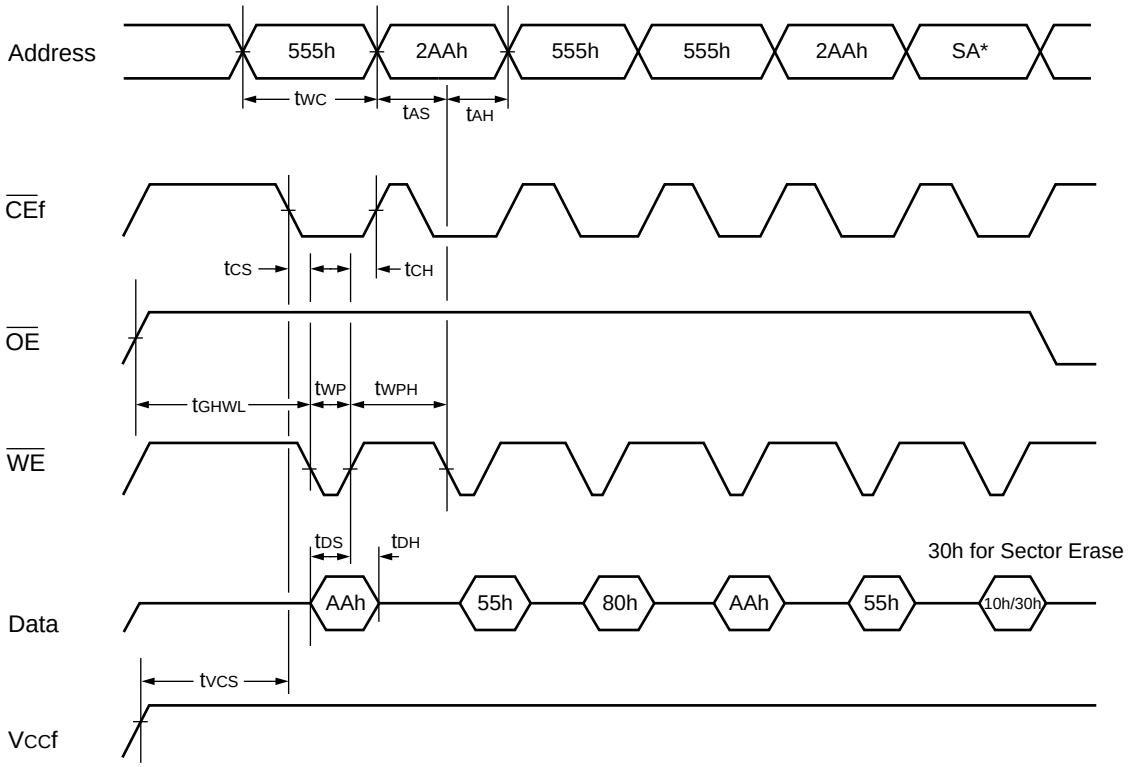
- **Alternate $\overline{CE}$f Controlled Program Operation Timing Diagram (128M Page Flash)**



$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.

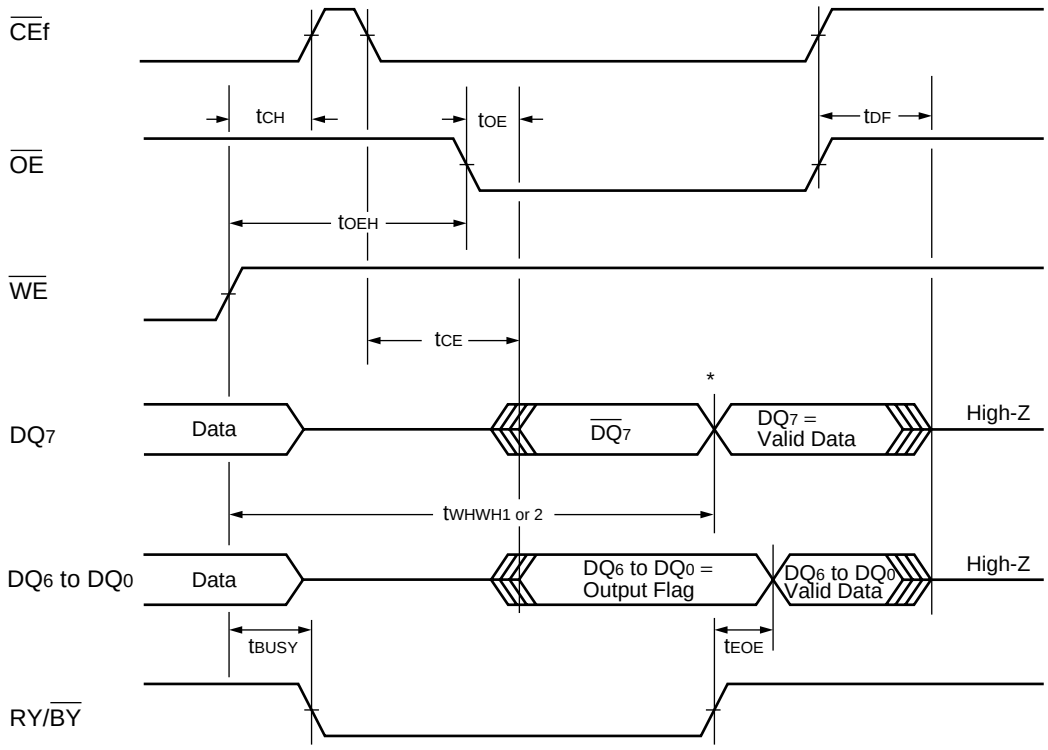
- **Chip/Sector Erase Operation Timing Diagram (128M Page Flash)**



$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

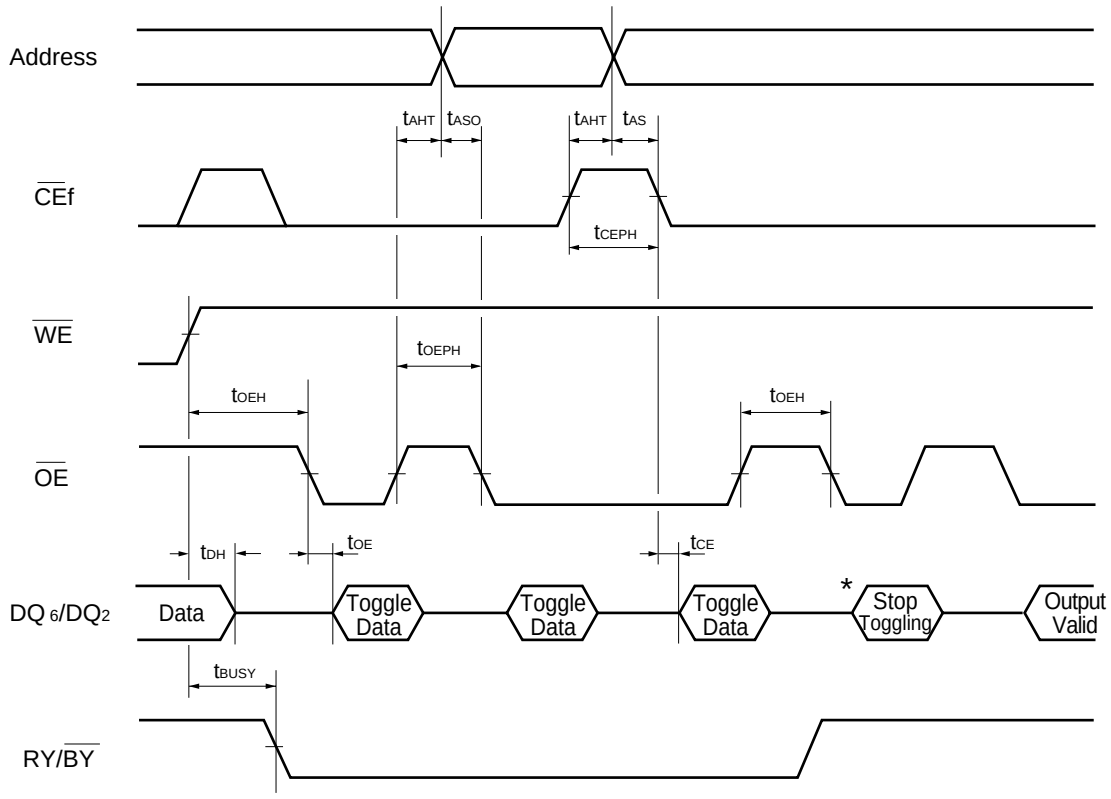
- **$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram (128M Page Flash)**



$\overline{\text{CE}}$f : $\overline{\text{CE}}$0f or $\overline{\text{CE}}$1f

* : DQ_7 = Valid Data (The device has completed the Embedded operation) .

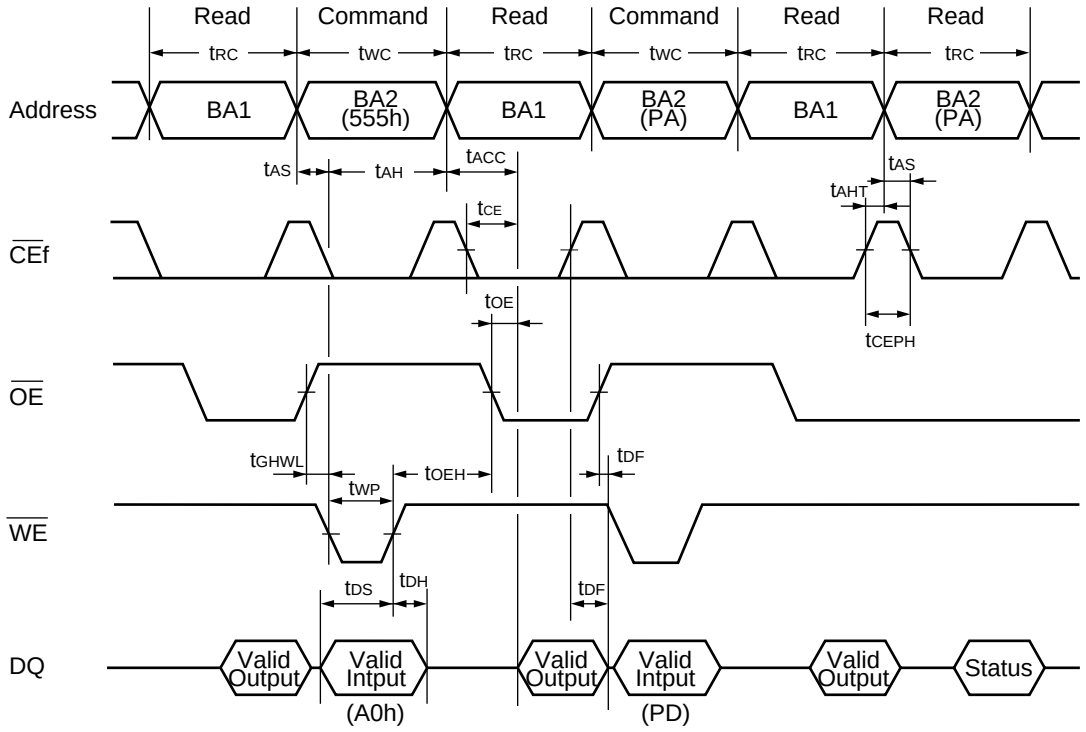
- **AC Waveforms for Toggle Bit I during Embedded Algorithm Operations (128M Page Flash)**



CEf : CE0f or CE1f

* : DQ_6 stops toggling (The device has completed the Embedded operation).

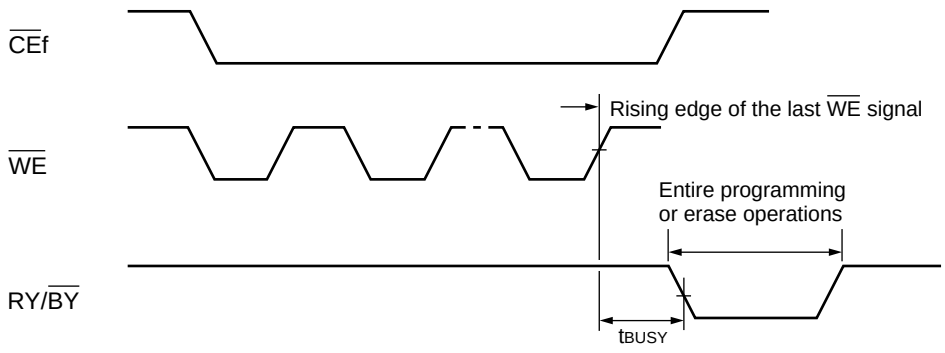
- **Bank-to-Bank Read/Write Timing Diagram (128M Page Flash)**



$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

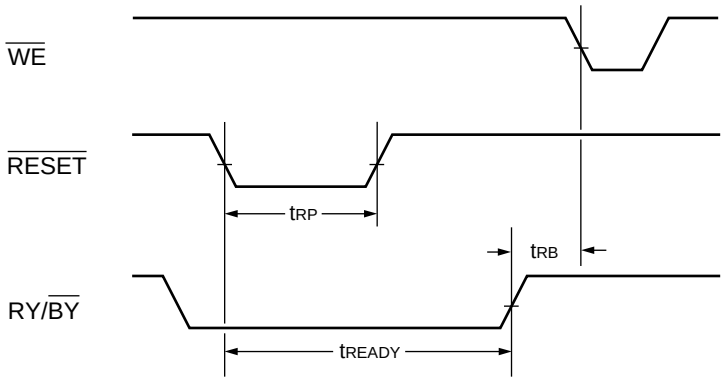
Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address corresponding to Bank 1
BA2 : Address corresponding to Bank 2

- **RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram (128M Page Flash)**

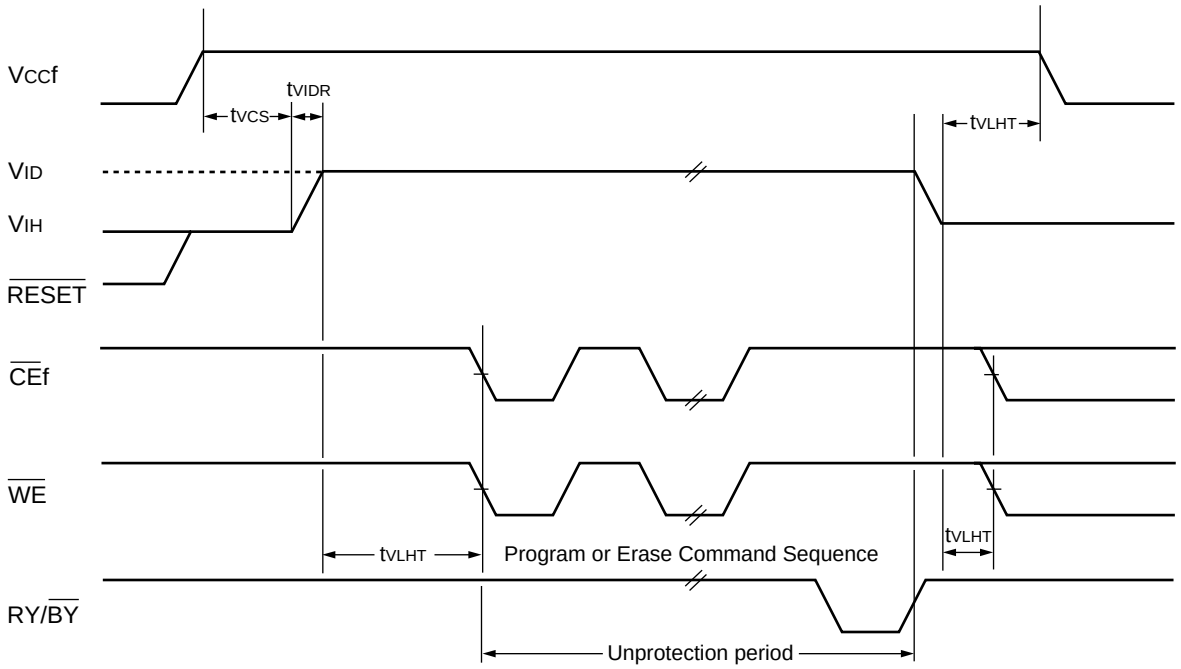


$\overline{CE}$f : $\overline{CE}$0f or $\overline{CE}$1f

- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (128M Page Flash)**

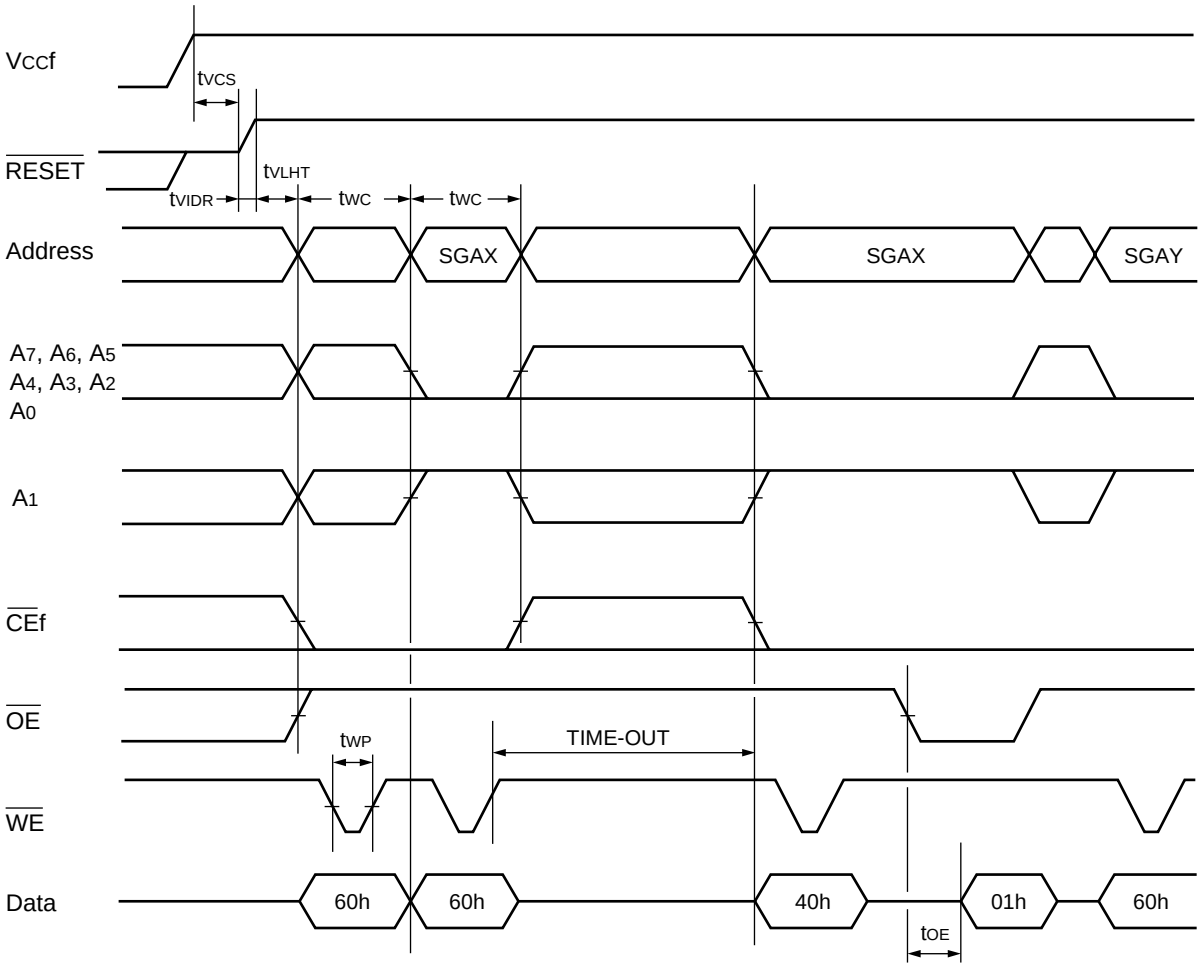


- **Temporary Sector Group Unprotection Timing Diagram (128M Page Flash)**



CEf : CE0f or CE1f

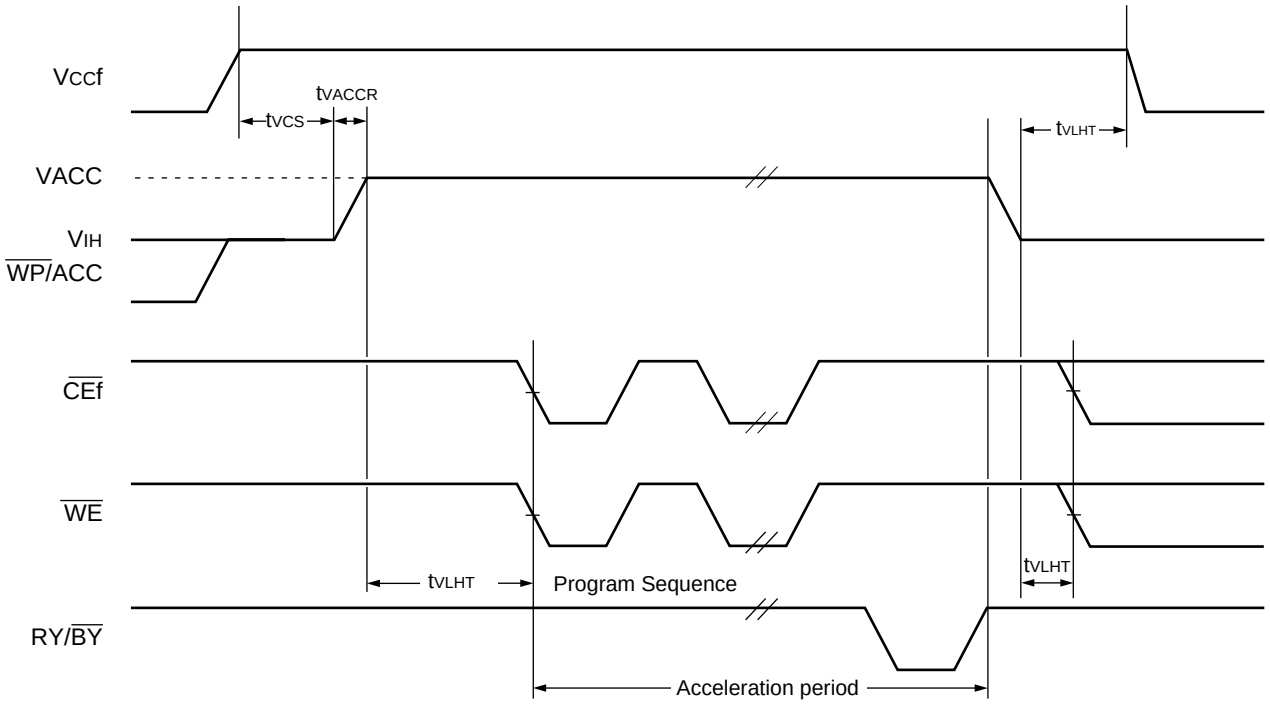
- **Extended Sector Group Protection Timing Diagram (128M Page Flash)**



$\overline{CE}f$: $\overline{CE}0f$ or $\overline{CE}1f$

SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min)

- **Accelerated Program Timing Diagram (128M Page Flash)**



CEf : CE0f or CE1f

4. Erase and Programing Performance (128M Page Flash)

Parameter	Value			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erasure
Word Programming Time	—	6.0	100	µs	Excludes system-level overhead
Chip Programming Time	—	50.3	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

Note: Typical Erase conditions T_A = + 25°C, V_{CC} = 2.9 V
Typical Program conditions T_A = + 25°C, V_{CC} = 2.9 V, Data = checker

■ 32 M FCRAM CHARACTERISTICS for MCP

1. Power Down (32M Page Mode FCRAM)

- **Power Down (32M Page mode FCRAM)**

The Power Down is to enter low power idle state when CE2r stays Low.

The 32M page mode FCRAM has four power down mode, Sleep, 4M Partial, 8M Partial, and 16M Partial. These can be programmed by series of read/write operation. Each mode has follwoing features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
4M Partial	4M bit	00000h to 3FFFFh
8M Partial	8M bit	00000h to 7FFFFh
16M Partial	16M bit	00000h to FFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2r is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

- **Power Down Program Sequence (32M Page mode FCRAM)**

The program requires total 6 read/write operation with unique address and data. Between each read/write operation requires that device be in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	0000h
5th	Write	1FFFFFh	Data Key
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significient address (MSB).
The second and third cycle are to write back the data (RDa) read by first cycle. If the third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation.
The forth and fifth cycle is to write the data key for program. The data of forth cycle must be all 0's and data of fifth cycle is a data key for mode selection. If the forth cycle is written into different address, the program is also cancelled.
The last cycle is to read from specific address key for mode selection. The both data key written by fifth cycle and address key must be the same mode for proper programming.

Once this program sequence is performed from a Partial mode to other Partial mode, the write data may be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

- **Address Key (32M Page mode FCRAM)**

The address key has following format.

Mode	Address			
	A_{20}	A_{19}	A_{18} to A_0	Binary
Sleep (default)	1	1	1	1FFFFFh
4M Partial	0	1	1	0FFFFFh
8M Partial	1	0	1	17FFFFh
16M Partial	0	0	1	07FFFFh

- **Data Key (32M Page mode FCRAM)**

The data key has following format.

Mode	Data			
	DQ_{15} to DQ_8	DQ_7 to DQ_2	DQ_1	DQ_0
Sleep (default)	0	0	1	1
4M Partial	0	0	1	0
8M Partial	0	0	0	1
16M Partial	0	0	0	0

The upper byte of data code may be ignored and it is just for recommendation to write 0's to upper byte for future compatibility.

2. AC Characteristics

- **READ OPERATION (32M Page mode FCRAM)**

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}$1r Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{LB}$ / $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	18	ns	*3, *6
Page Read Cycle Time	t_{PRC}	25	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1r Low to Output Low-Z	t_{CLZ}	3	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}$ / $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1r High to Output High-Z	t_{CHZ}	—	20	ns	*4
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*4
$\overline{LB}$ / $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*4
Address Setup Time to $\overline{CE}$1r Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *8
Page Address Invalid Time	t_{AXP}	—	10	ns	*6, *8
Address Hold Time from $\overline{CE}$1r High	t_{CHAH}	–5	—	ns	*9
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{CE}$1r High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1r is kept at Low without change of address input of A_{20} to A_3.
If needed by system operation, please contact local FUJITSU representative for the relaxation of 1 µs limitation.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 30 pF.

*4 : The output load 5 pF without any other load.

*5 : Applicable to A_{20} to A_3 when $\overline{CE}$1r is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE}$1r is kept at Low for the page address access.

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}$1r stays Low, $\overline{CE}$1r must be brought to High within 4 µs.
In other words, Page Read Cycle must be closed within 4 µs.

*8 : Applicable when at least two of address inputs among applicable are switched from previous state.

*9 : t_{RC}(Min) and t_{PRC}(Min) must be satisfied.

- **WRITE OPERATION (32M Page mode FCRAM)**

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*2
$\overline{CE}$1r Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$ / $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{CE}$1r Write Recovery Time	t_{WRC}	15	—	ns	*4
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*4
$\overline{LB}$ / $\overline{UB}$ Write Recovery Time	t_{BR}	15	1000	ns	*4
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
Address Invalid Time after Write	t_{AXW}	—	10	ns	*5
$\overline{OE}$ High to $\overline{CE}$1r Low Setup Time for Write	t_{OHCL}	–5	—	ns	*6
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*7
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	20	—	ns	
$\overline{CE}$1r High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1r is kept at Low without any address change. If the relaxation is needed by system operation, please contact local FUJITSU representative for the relaxation of 1 μs limitation.

*2 : Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).

*3 : Write pulse is defined from High to Low transition of $\overline{CE}$1r, $\overline{WE}$, or $\overline{LB}$ / $\overline{UB}$, whichever occurs last.

*4 : Write recovery is defined from Low to High transition of $\overline{CE}$1r, $\overline{WE}$, or $\overline{LB}$ / $\overline{UB}$, whichever occurs first.

*5 : Applicable to any address change when $\overline{CE}$1r stays Low.

*6 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5ns after $\overline{CE}$1r is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*7 : If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

- **POWER DOWN PARAMETERS (32M Page mode FCRAM)**

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
CE2r Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2r Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
$\overline{CE}$1r High Hold Time following CE2r High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1r High Hold Time following CE2r High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	1	—	µs	*2
$\overline{CE}$1r High Setup Time following CE2r High after Power Down Exit	t_{CHS}	0	—	ns	

*1 : Applicable also to power-up.

*2 : Applicable when 4M, 8M, and 16M Partial mode is programmed.

- **OTHER TIMING PARAMETERS (32M Page mode FCRAM)**

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{CE}$1r High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1r High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
$\overline{CE}$1r High Hold Time following CE2r High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time	t_T	1	25	ns	*2

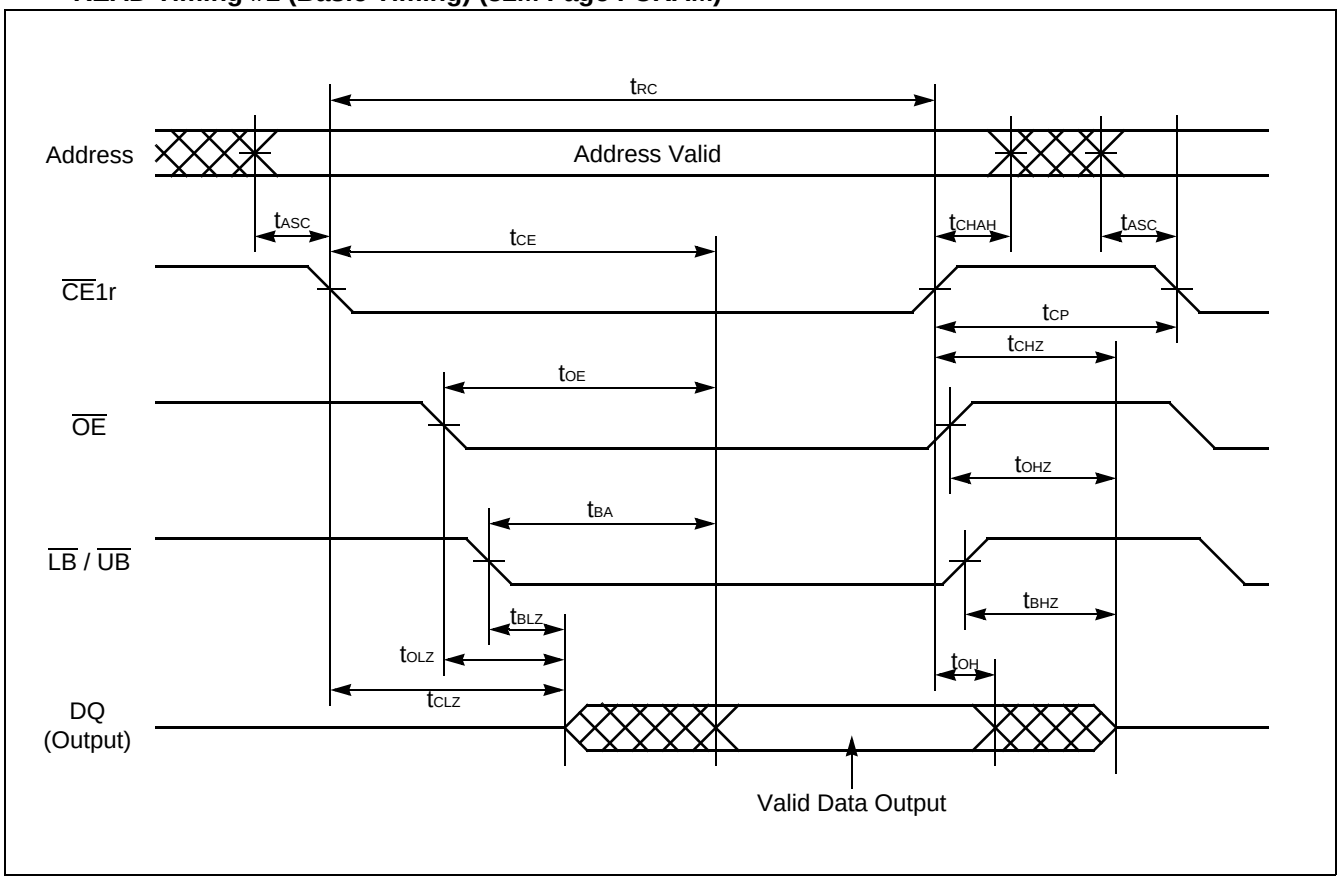
*1 : Some data might be written into any address location if t_{CHWX}(Min) is not satisfied.

*2 : The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5ns, it may violate AC specification of some timing parameters.

- **AC TEST CONDITIONS (32M Page mode FCRAM)**

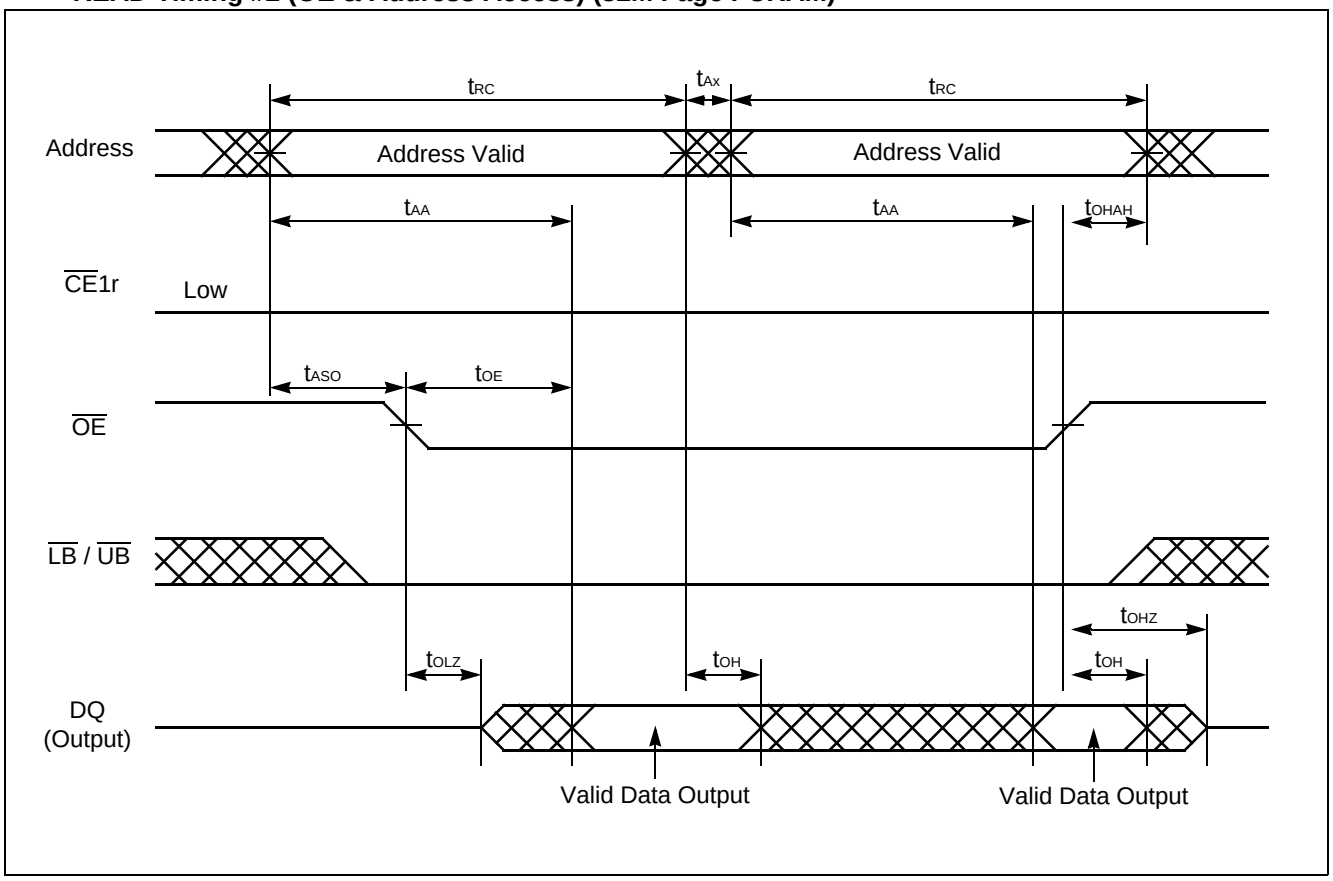
Description	Symbol	Test Setup	Value	Unit	Remarks
Input High Level	V_{IH}	—	$V_{CC}r$	V	
Input Low Level	V_{IL}	—	V_{SS}	V	
Input Timing Measurement Level	V_{REF}	—	$V_{CC}r \times 0.5$	V	
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns	

- **READ Timing #1 (Basic Timing) (32M Page FCRAM)**



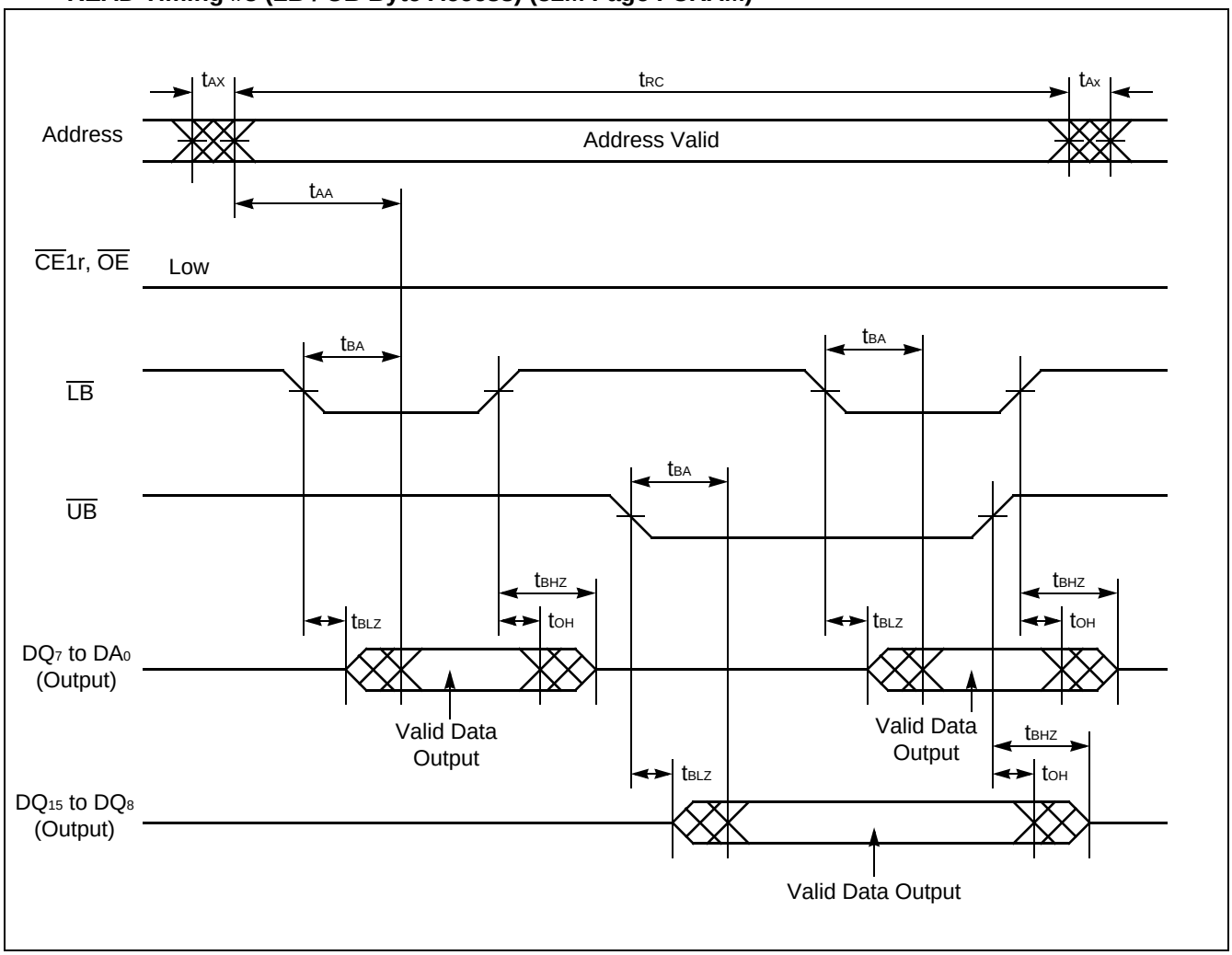
Note : CE2r and $\overline{WE}$ must be High for entire read cycle.

- **READ Timing #2 ($\overline{OE}$ & Address Access) (32M Page FCRAM)**



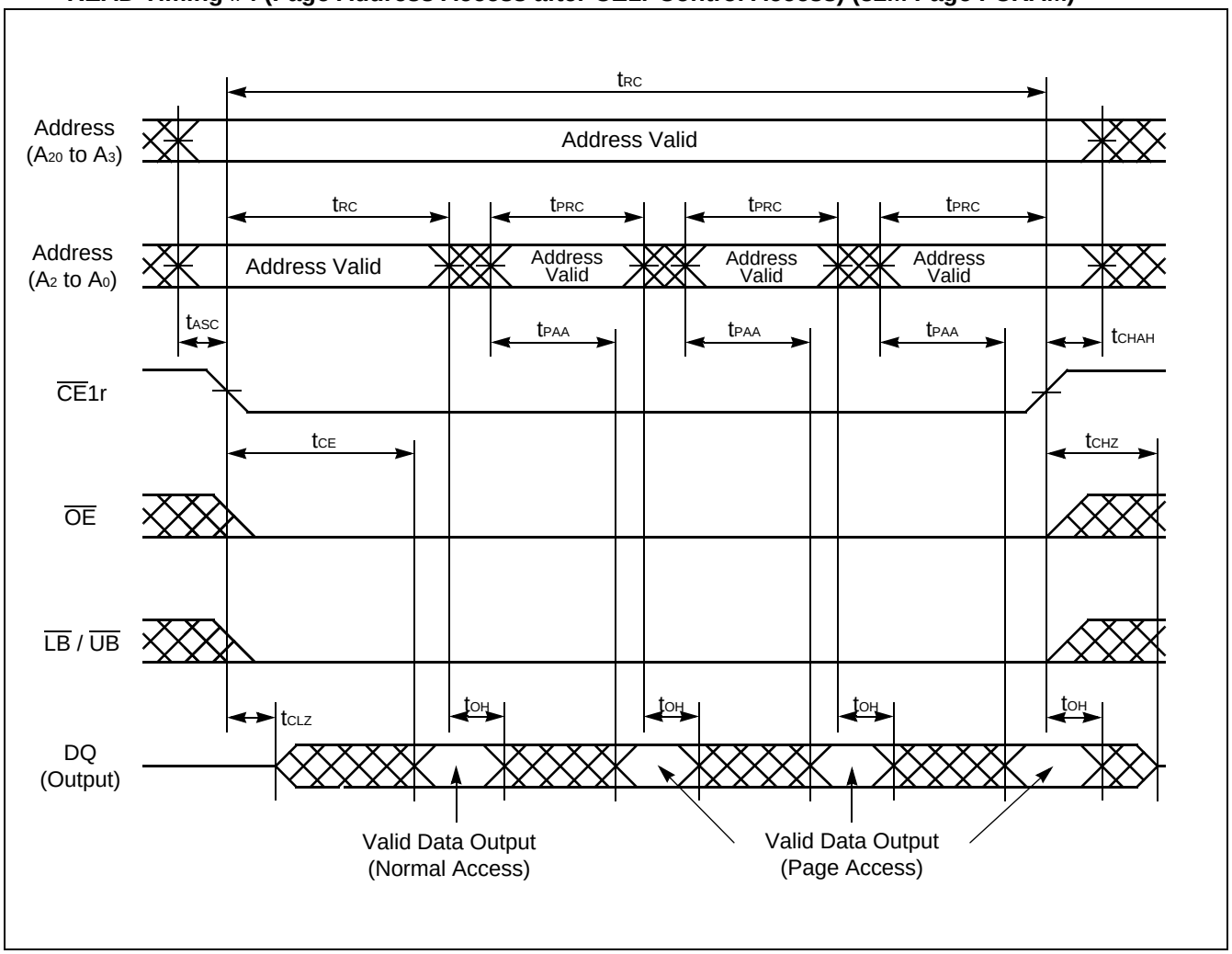
Note : CE2r and $\overline{WE}$ must be High for entire read cycle.

- **READ Timing #3 ($\overline{LB}$ / $\overline{UB}$ Byte Access) (32M Page FCRAM)**



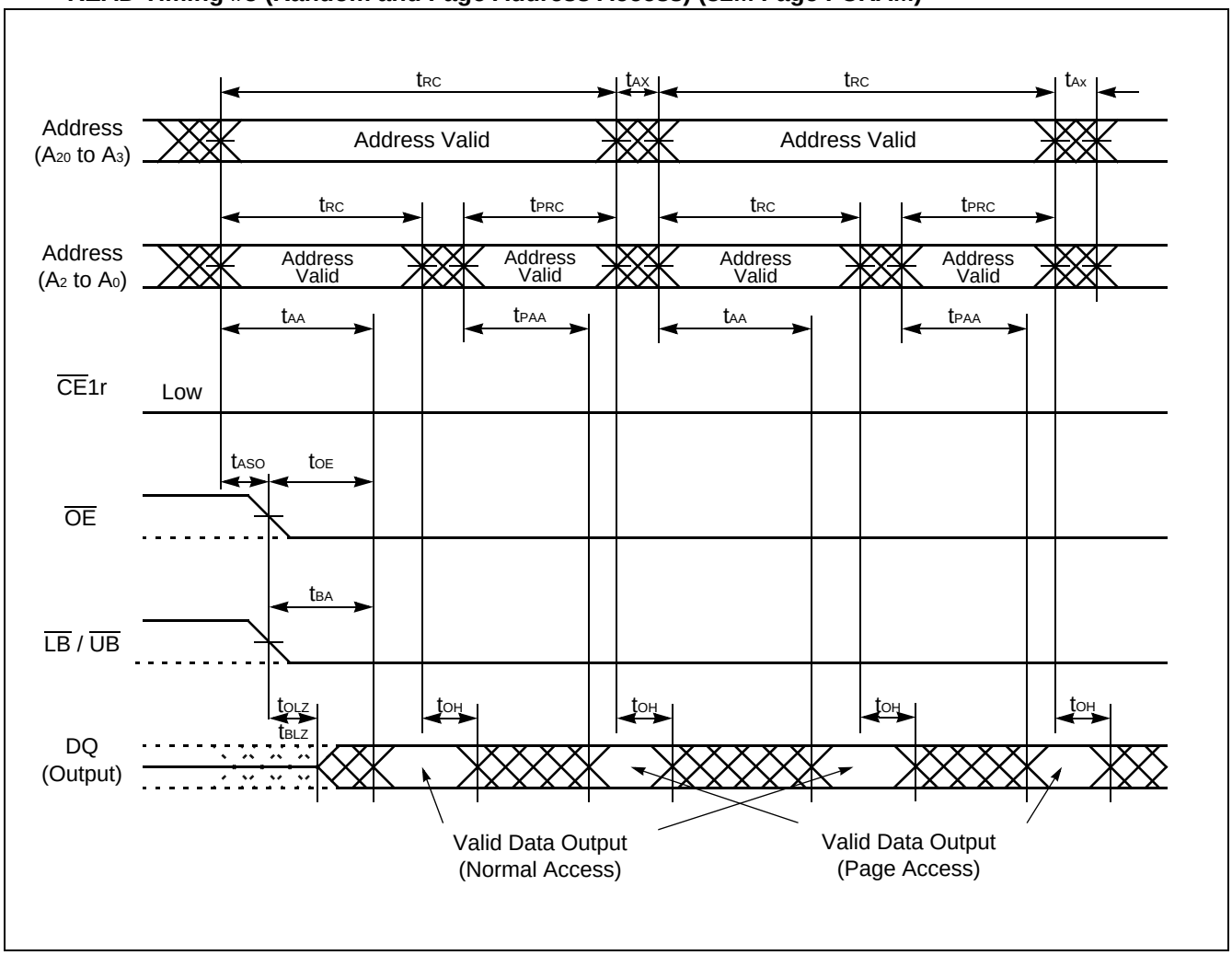
Note : CE2r and $\overline{WE}$ must be High for entire read cycle.

- **READ Timing #4 (Page Address Access after $\overline{CE}$1r Control Access) (32M Page FCRAM)**



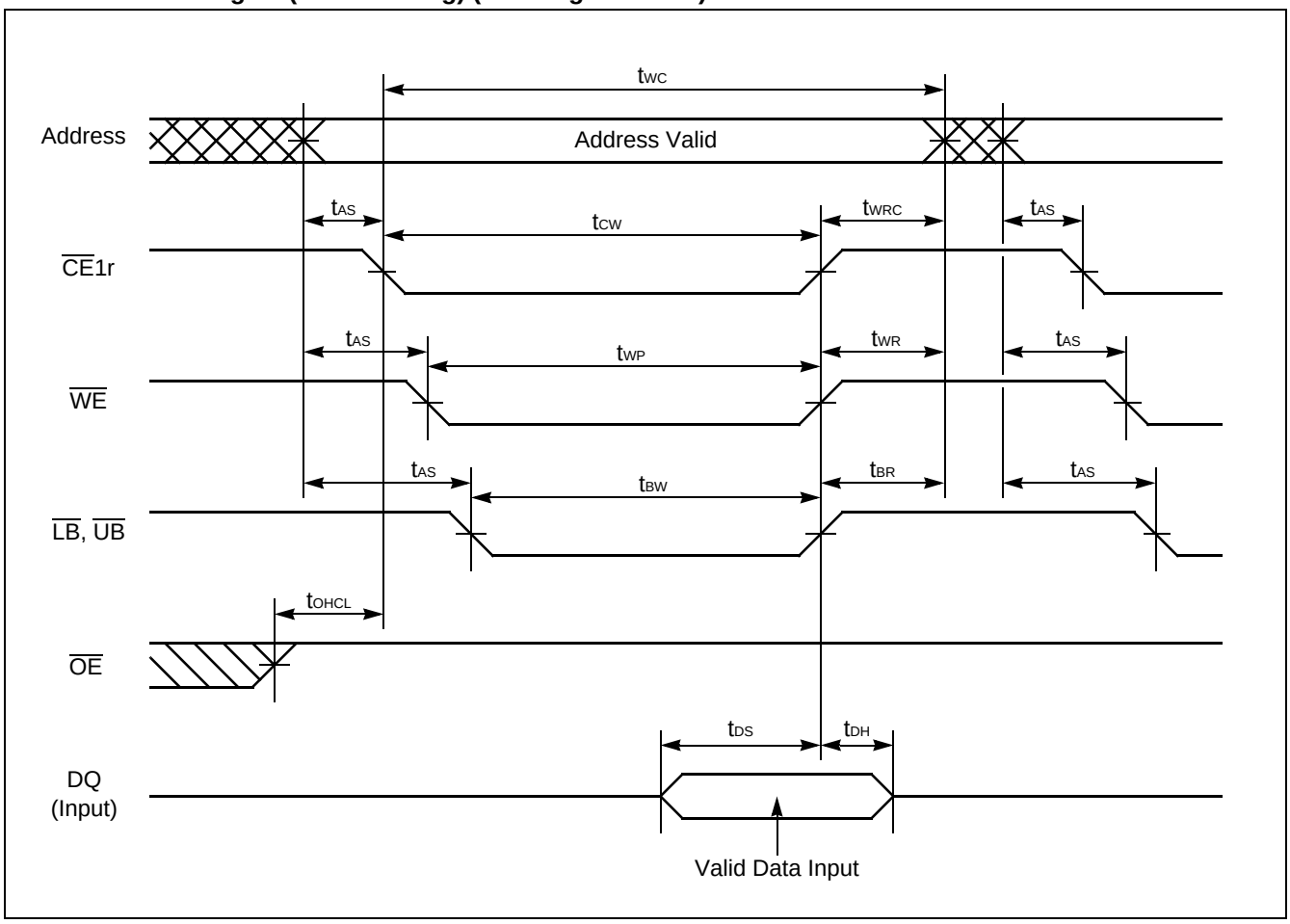
Note : CE2r and $\overline{WE}$ must be High for entire read cycle.

- **READ Timing #5 (Random and Page Address Access) (32M Page FCRAM)**



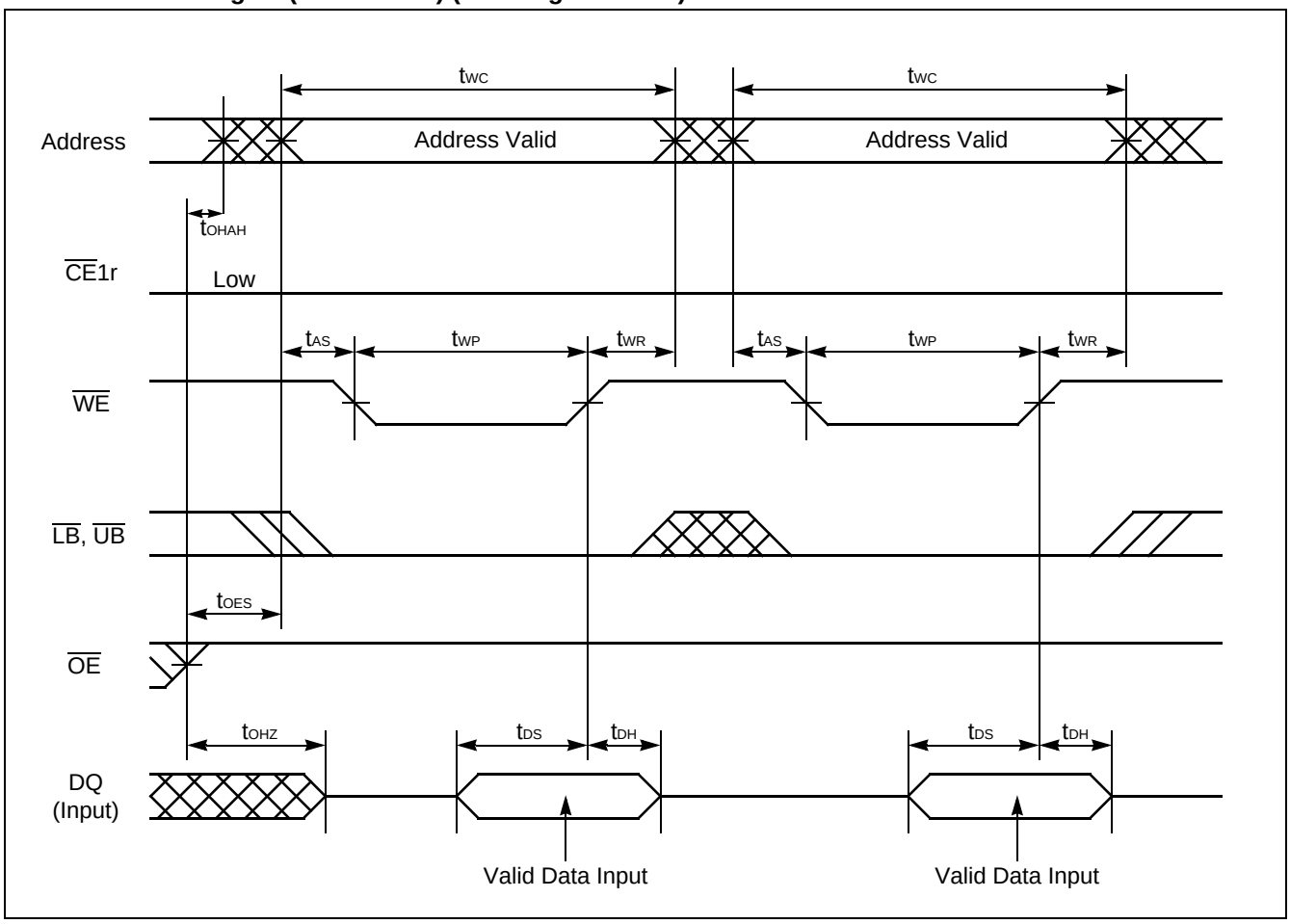
Note : CE2r and $\overline{WE}$ must be High for entire read cycle.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

- **WRITE Timing #1 (Basic Timing) (32M Page FCRAM)**



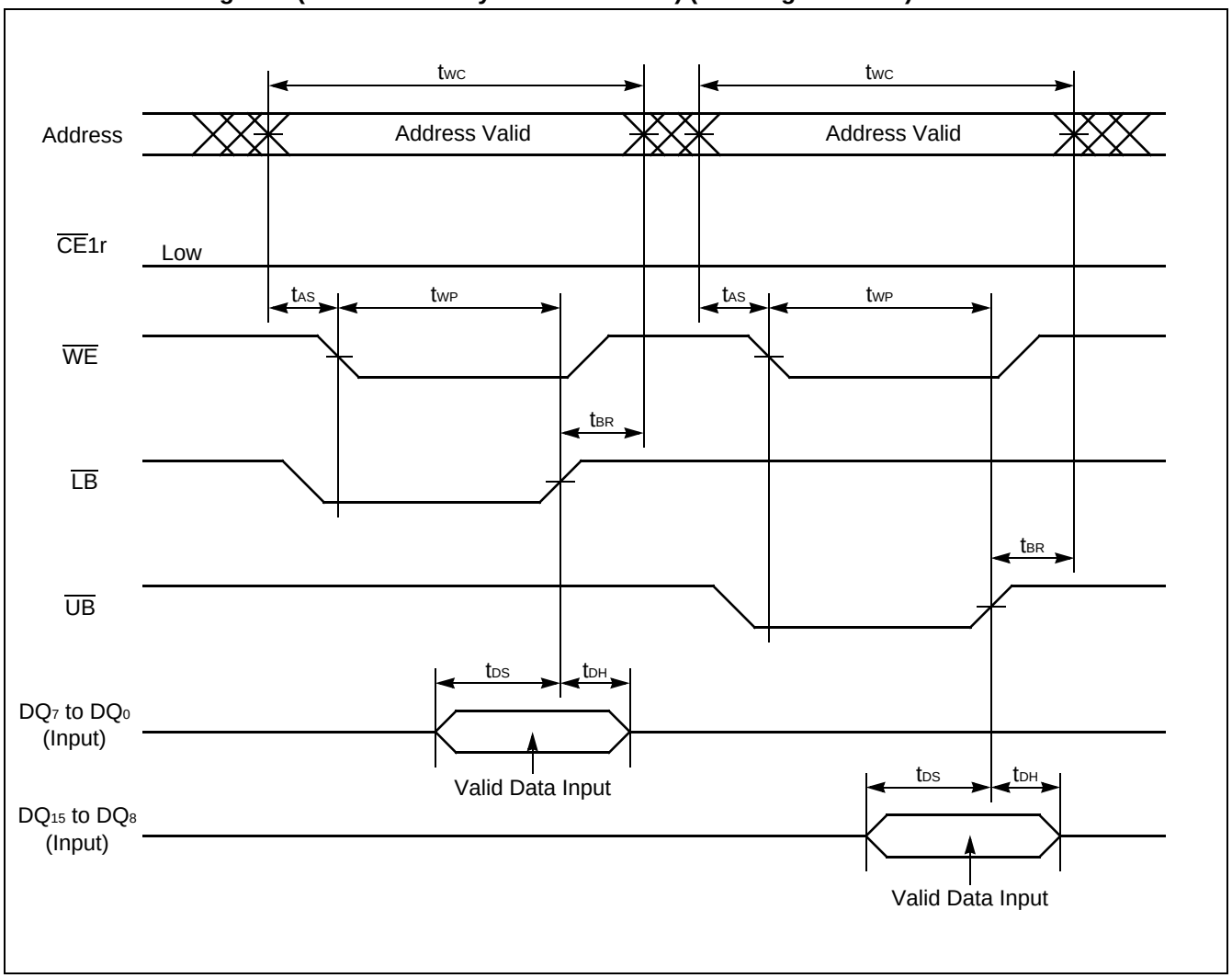
Note : CE2r must be High for write cycle.

- **WRITE Timing #2 ($\overline{WE}$ Control) (32M Page FCRAM)**



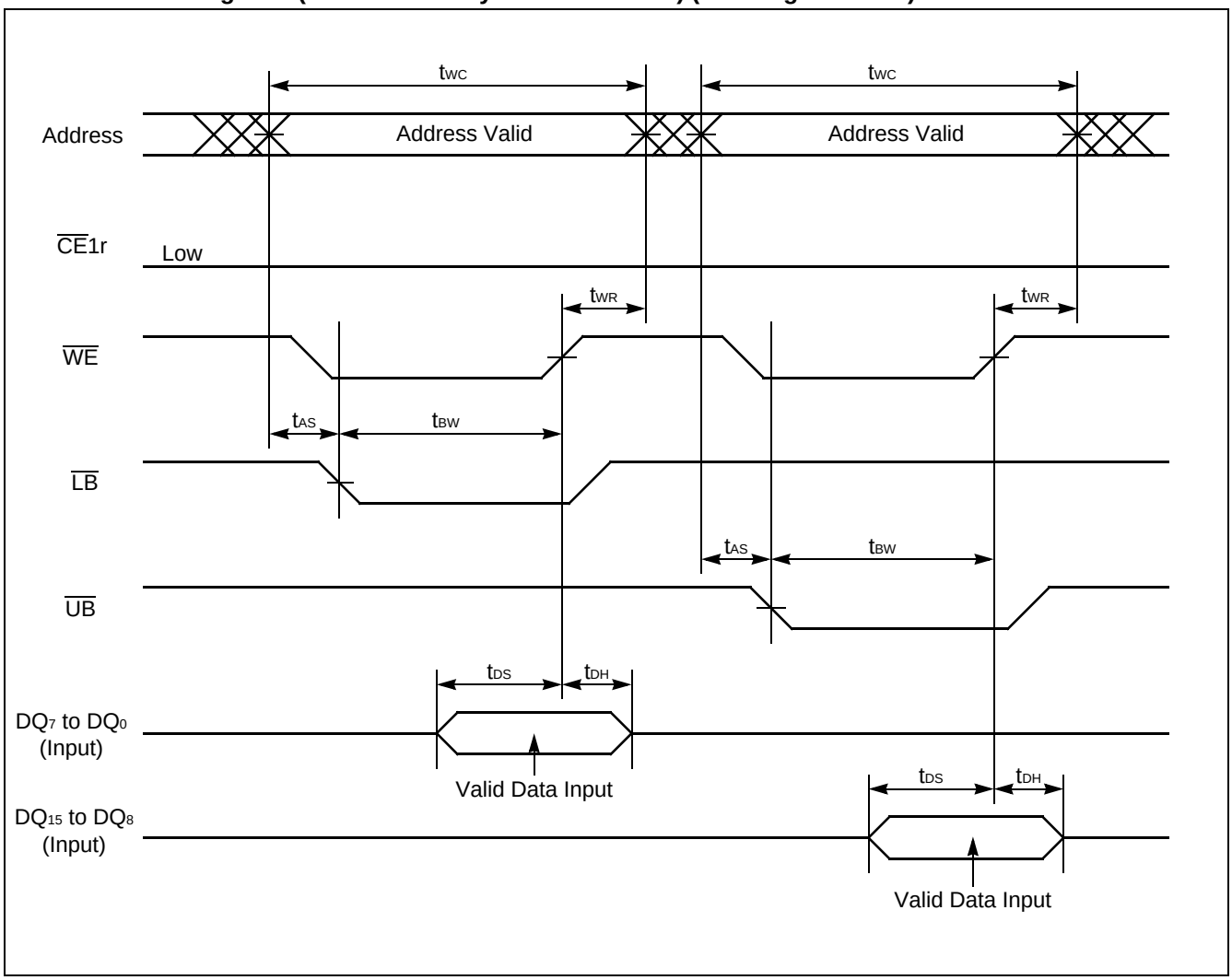
Note : CE2r must be High for write cycle.

- **WRITE Timing #3-1 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) (32M Page FCRAM)**



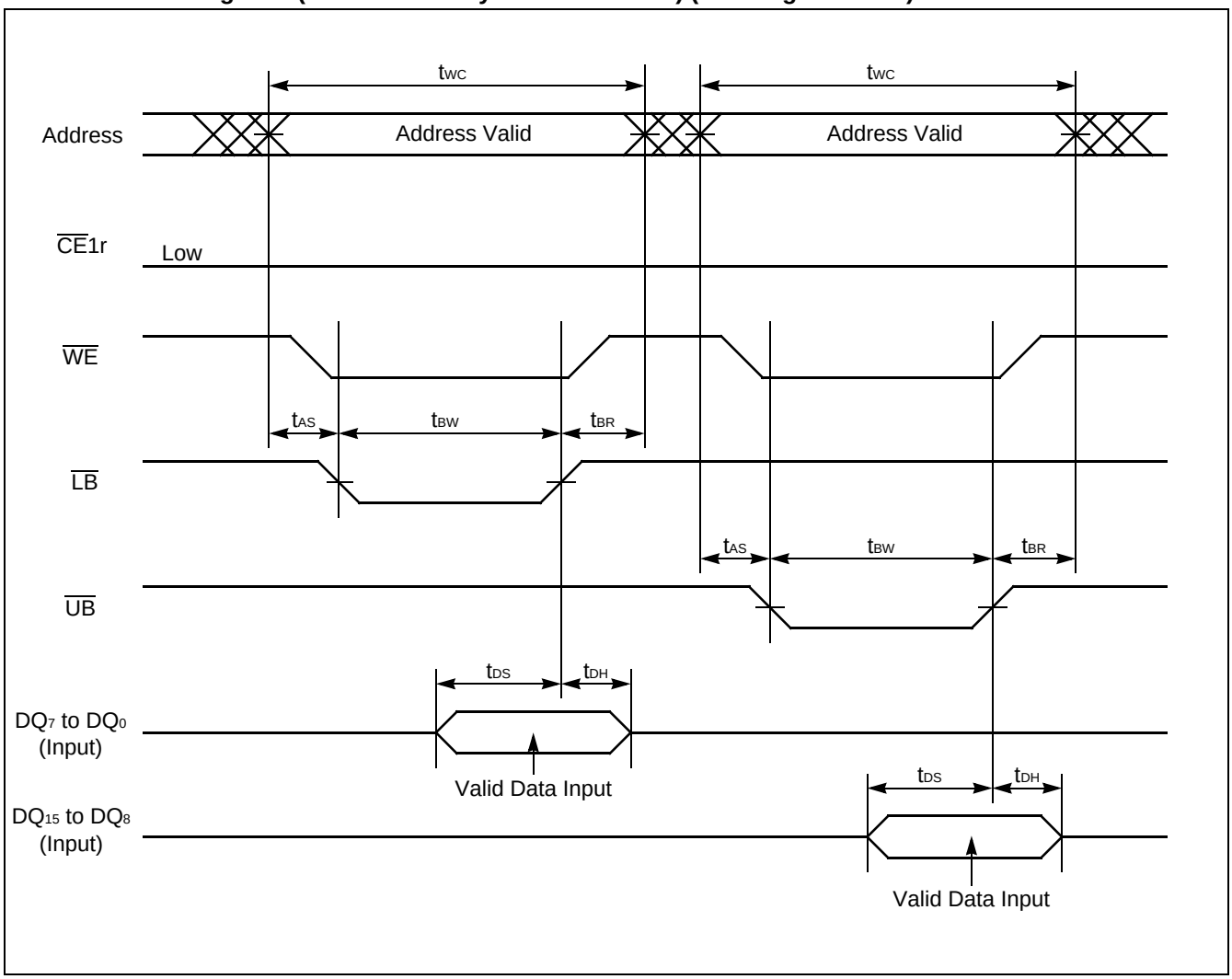
Note : CE2r must be High for write cycle.

- **WRITE Timing #3-2 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) (32M Page FCRAM)**



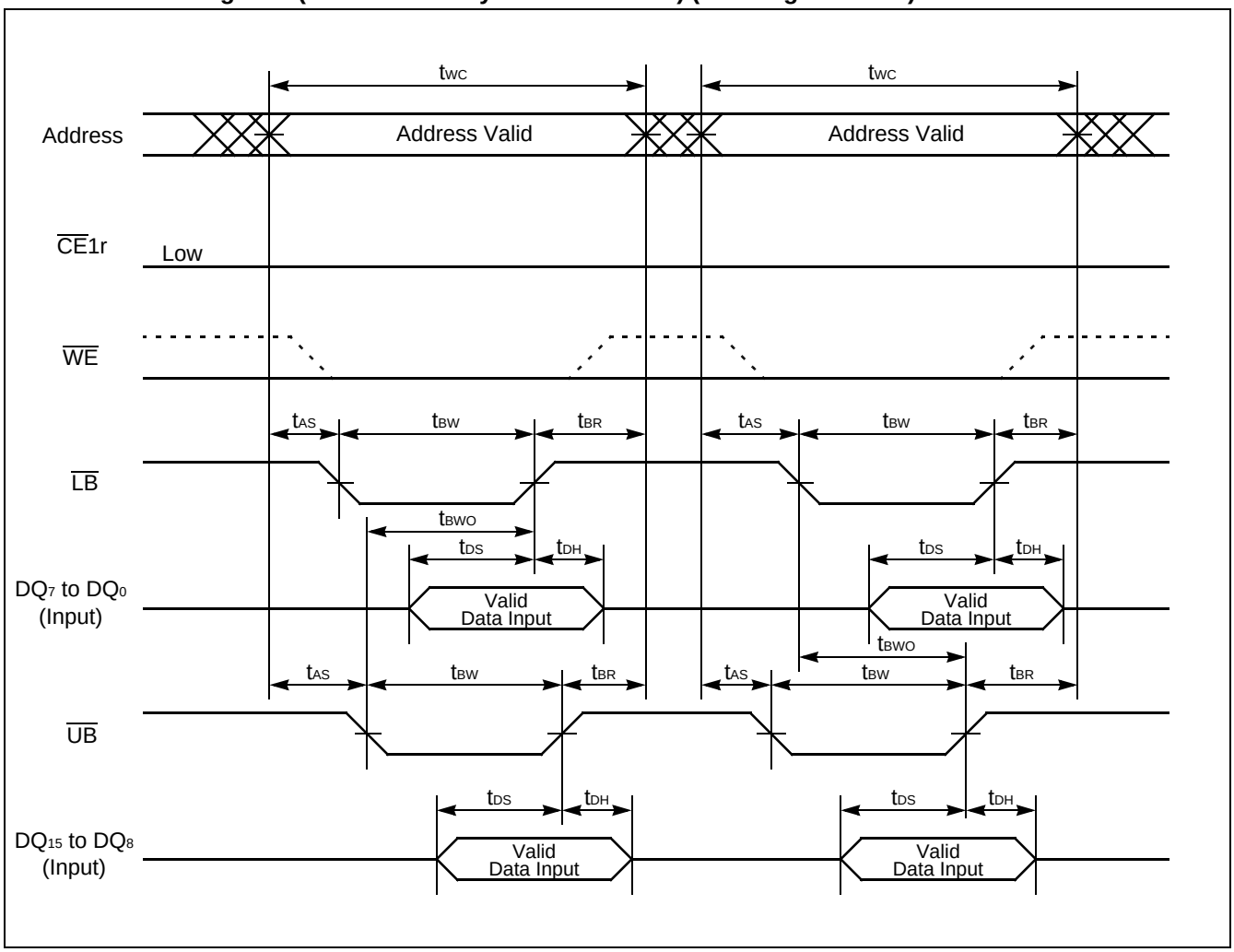
Note : CE2r must be High for write cycle.

- **WRITE Timing #3-3 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) (32M Page FCRAM)**



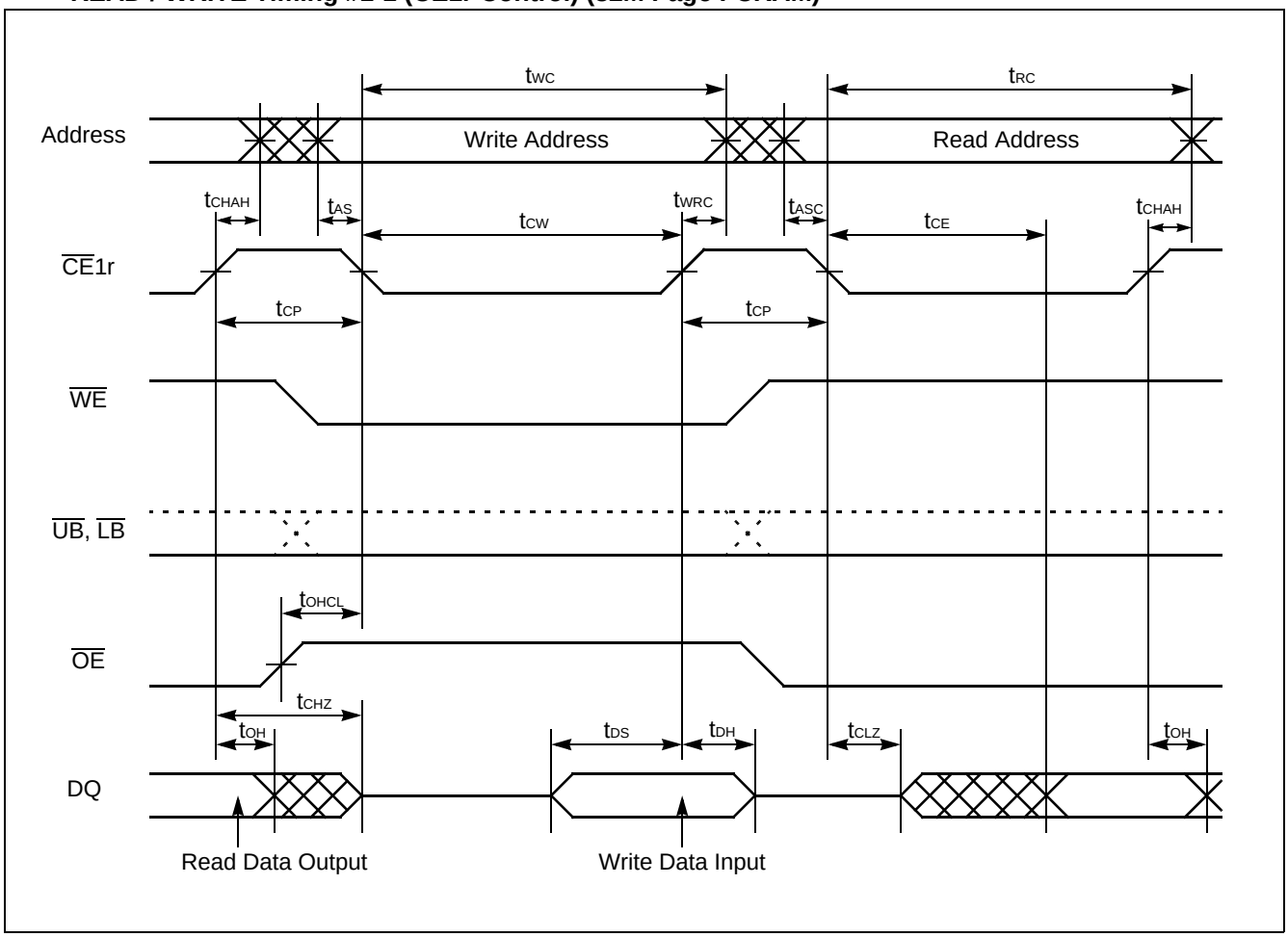
Note : CE2r must be High for write cycle.

- **WRITE Timing #3-4 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) (32M Page FCRAM)**



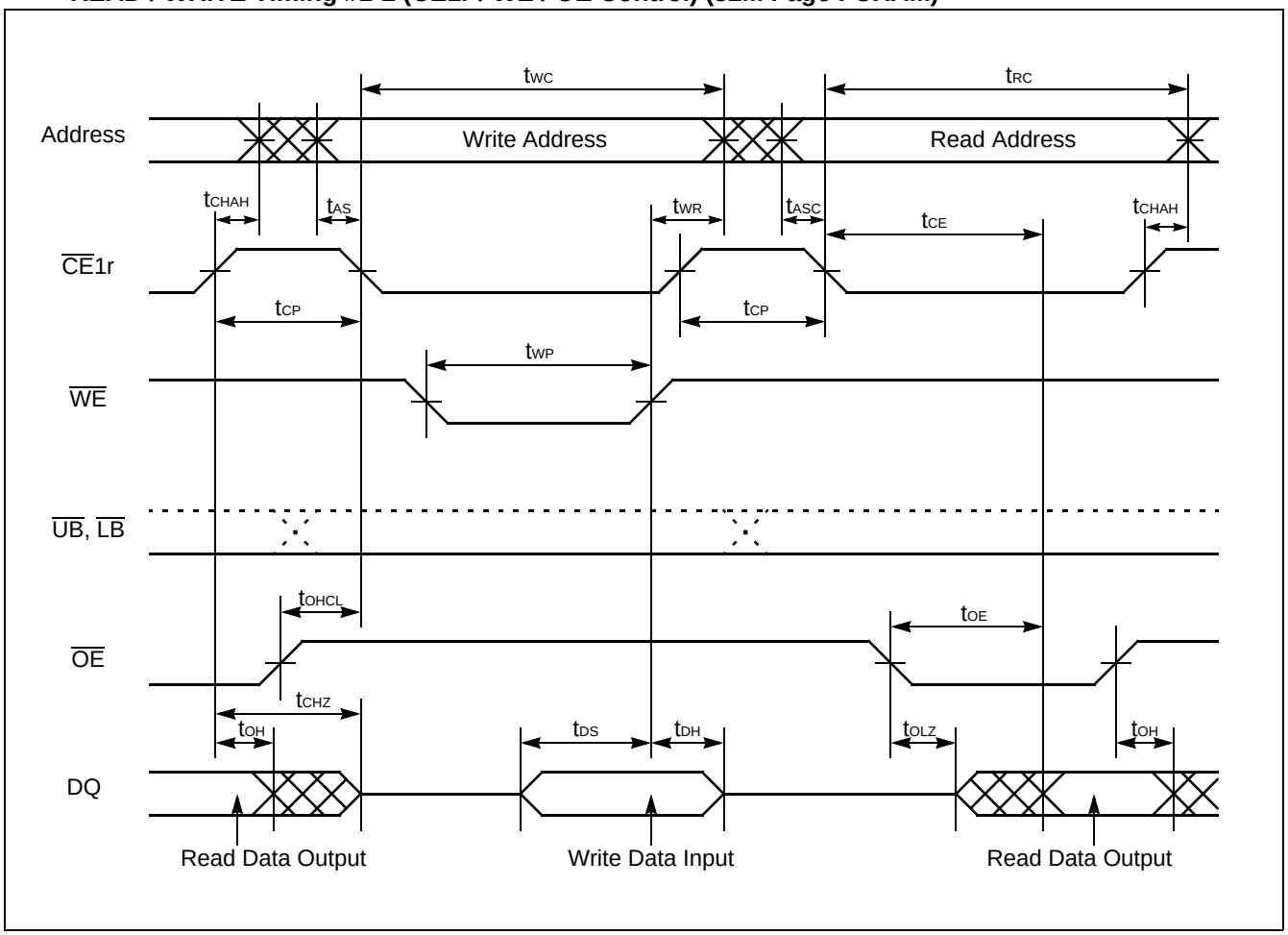
Note : CE2r must be High for write cycle.

- **READ / WRITE Timing #1-1 ($\overline{CE}$1r Control) (32M Page FCRAM)**



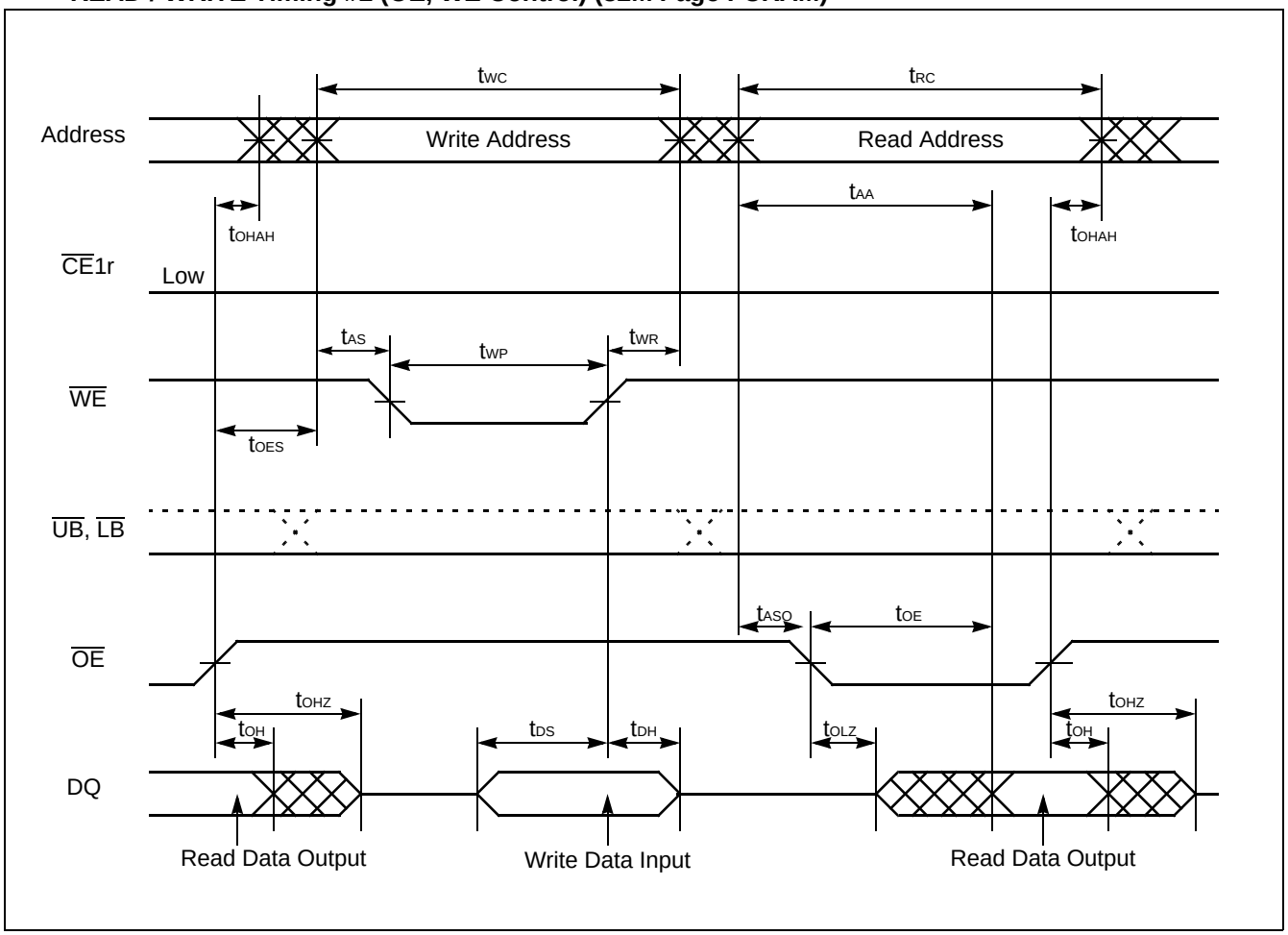
Note : Write address is valid from either $\overline{CE}$1r or $\overline{WE}$ of last falling edge.

- **READ / WRITE Timing #1-2 ($\overline{CE}$1r / $\overline{WE}$ / $\overline{OE}$ Control) (32M Page FCRAM)**



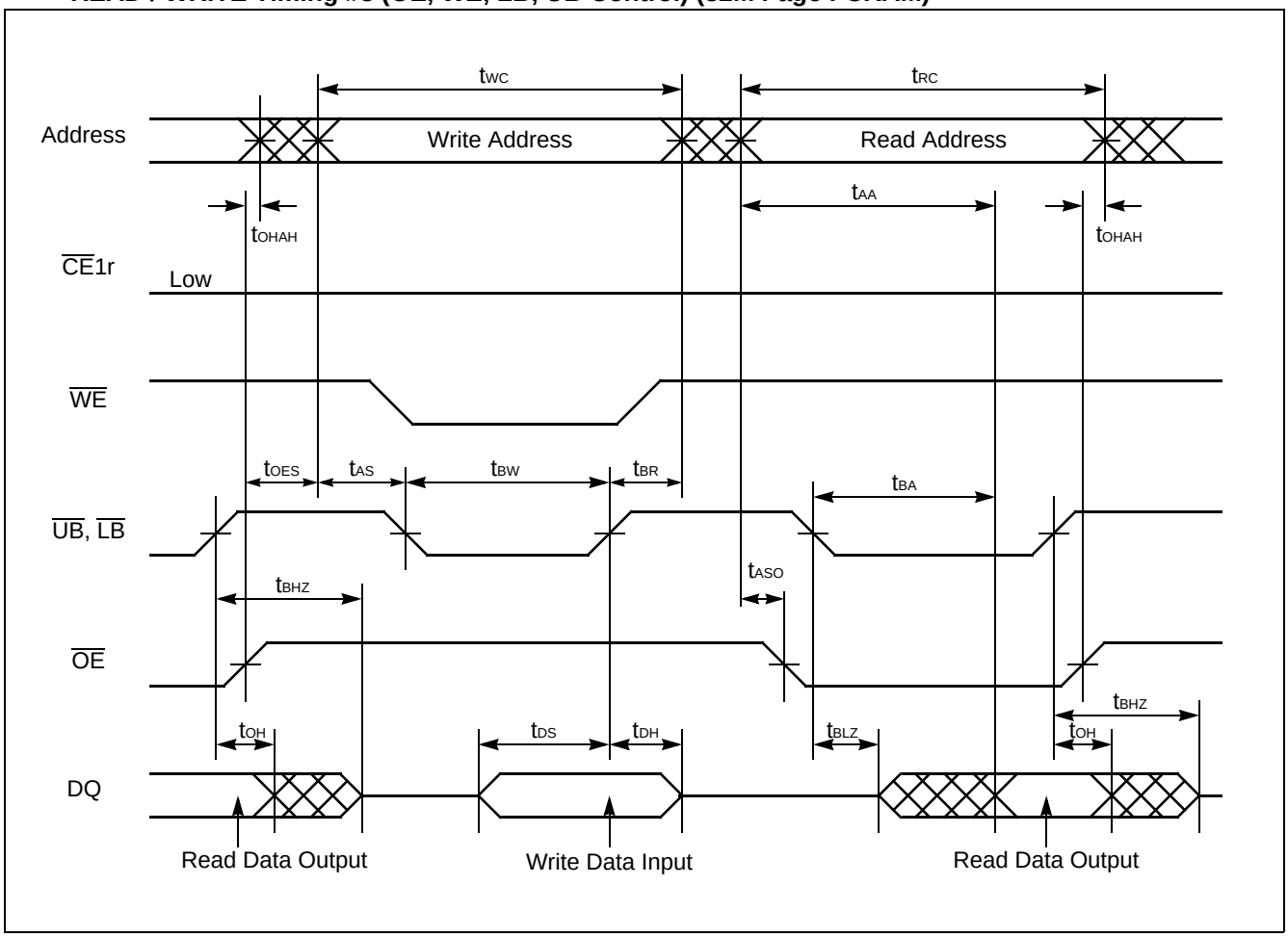
Note : $\overline{OE}$ can be Low fixed in write operation under $\overline{CE}$1r control $\overline{RD}$-$\overline{WR}$-$\overline{RD}$ operation.

- **READ / WRITE Timing #2 ($\overline{OE}$, $\overline{WE}$ Control) (32M Page FCRAM)**



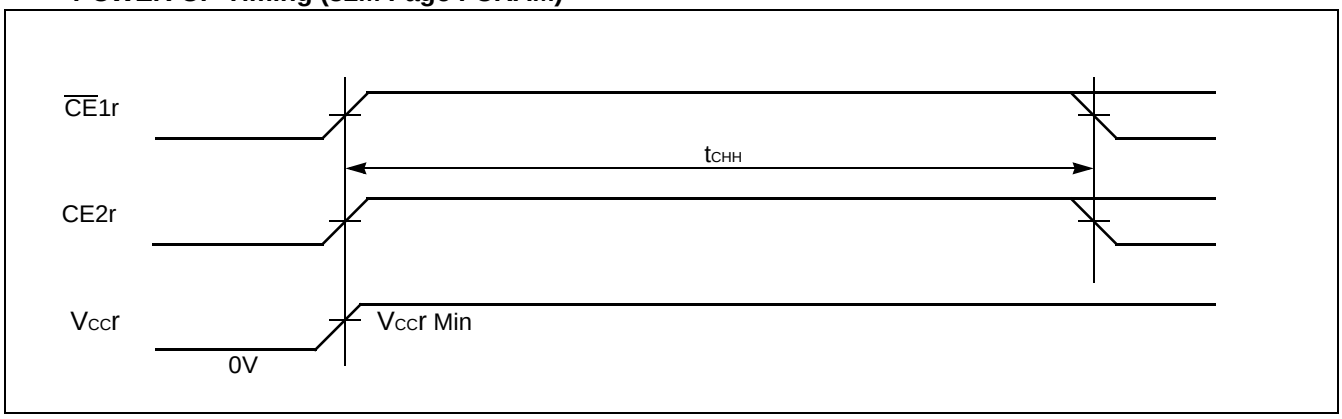
Note : $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1r is tied to Low, output is exclusively controlled by $\overline{OE}$.

- **READ / WRITE Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control) (32M Page FCRAM)**



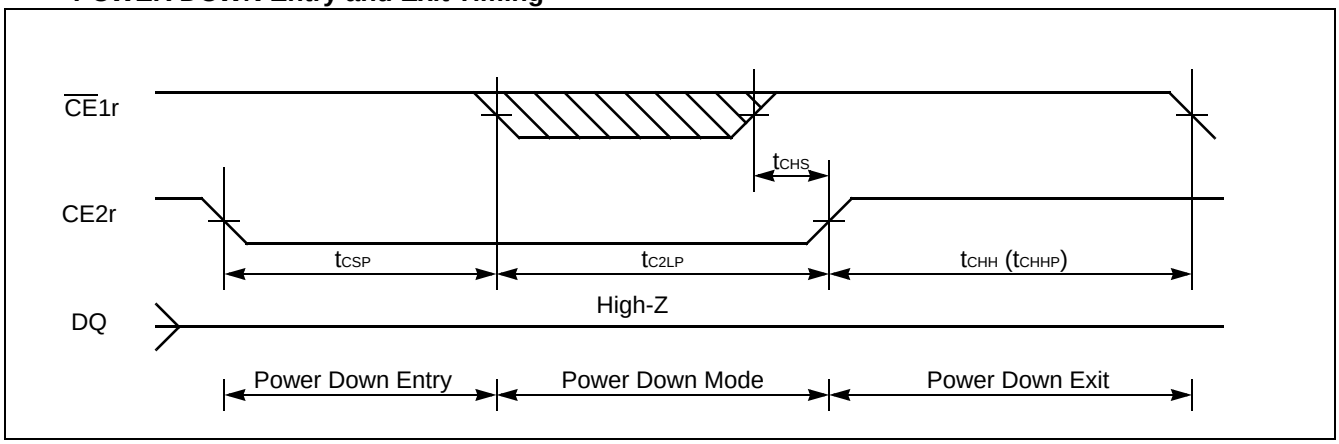
Note : $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1r is tied to Low, output is exclusively controlled by $\overline{OE}$.

- **POWER-UP Timing (32M Page FCRAM)**



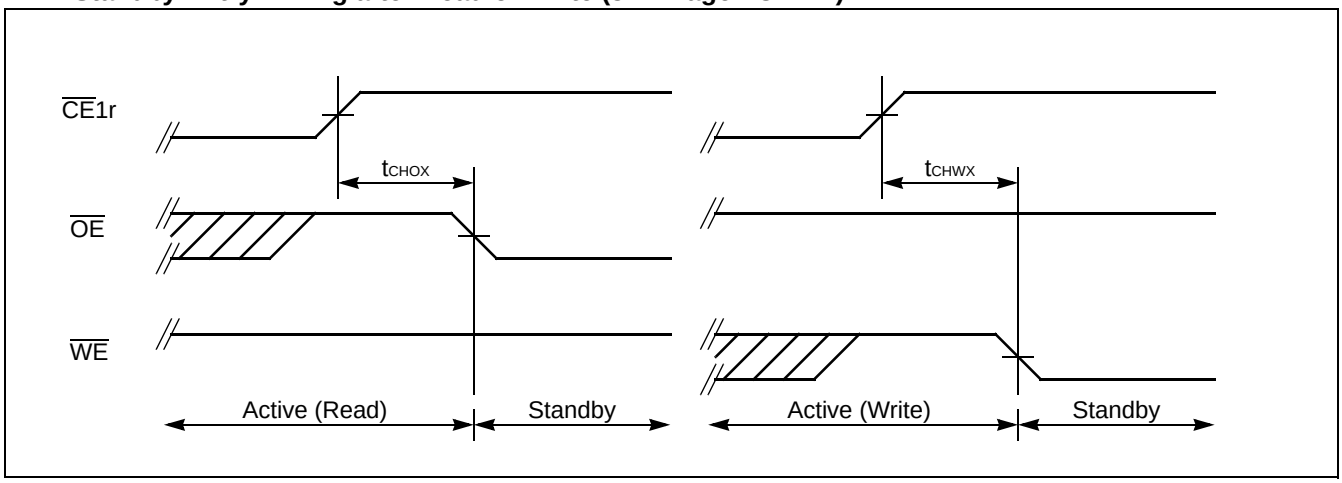
Note : The t_{CHH} specifies after $V_{CC}r$ reaches specified minimum level and applicable both $\overline{CE}1r$ and CE2r.

- **POWER DOWN Entry and Exit Timing**



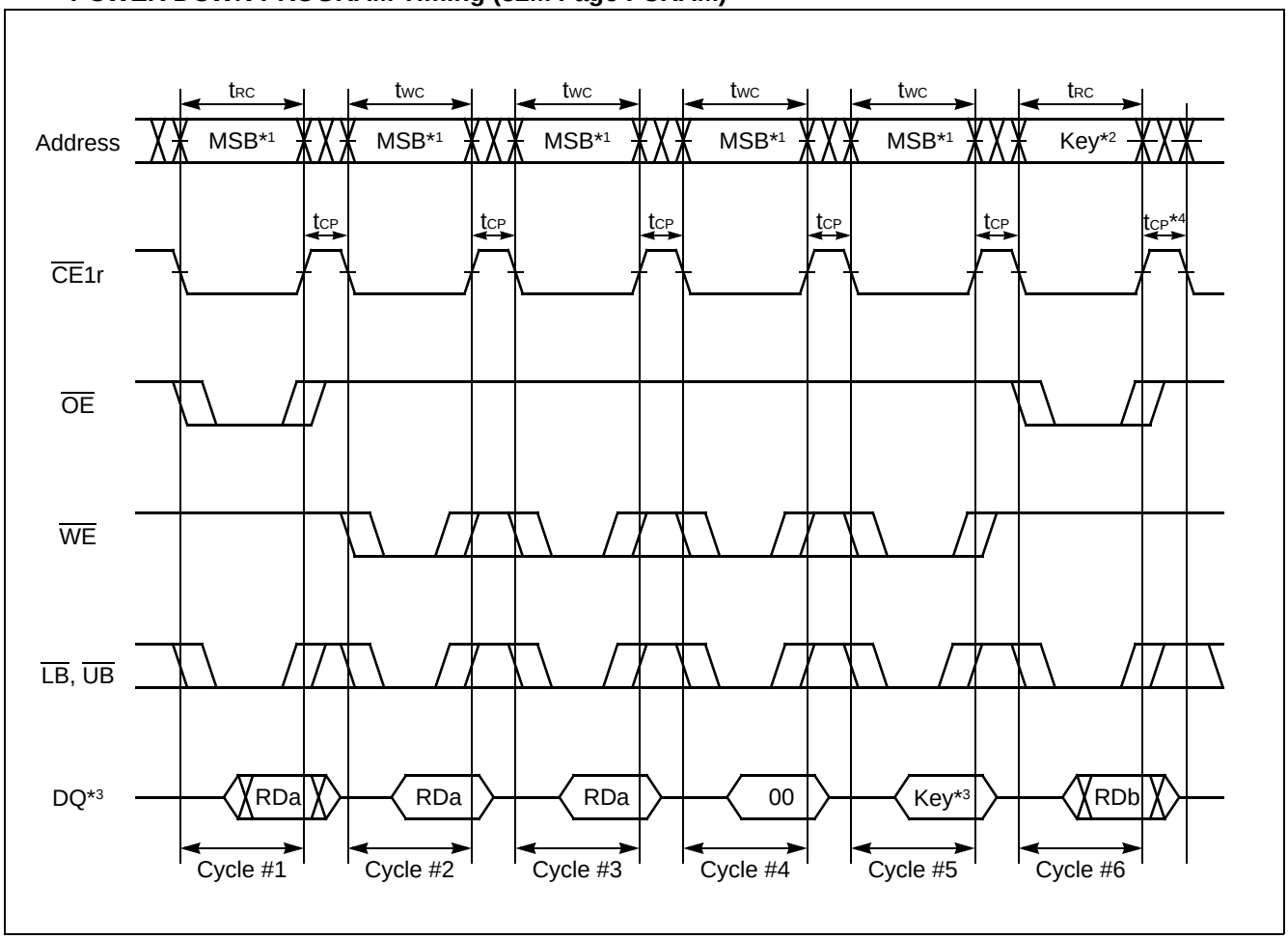
Note : This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.

- **Standby Entry Timing after Read or Write (32M Page FCRAM)**



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (Min) period for Standby mode from $\overline{CE}1r$ Low to High transition.

- **POWER DOWN PROGRAM Timing (32M Page FCRAM)**



*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■ 32 M FCRAM CHARACTERISTICS for MCP 1. Power Down Program Timing (32 M Page FCRAM) ". If not, the operation and data are not guaranteed.

*3 : The data key must confirm the format specified in "■ 32 M FCRAM CHARACTERISTICS for MCP 1. Power Down Program Timing (32 M Page FCRAM) ". If not, the operation and data are not guaranteed.

*4 : After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	—	11.0	14.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	12.0	16.0	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	—	14.0	16.0	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	—	21.5	26.0	pF

Note: Test conditions T_A = + 25°C, f = 1.0 MHz

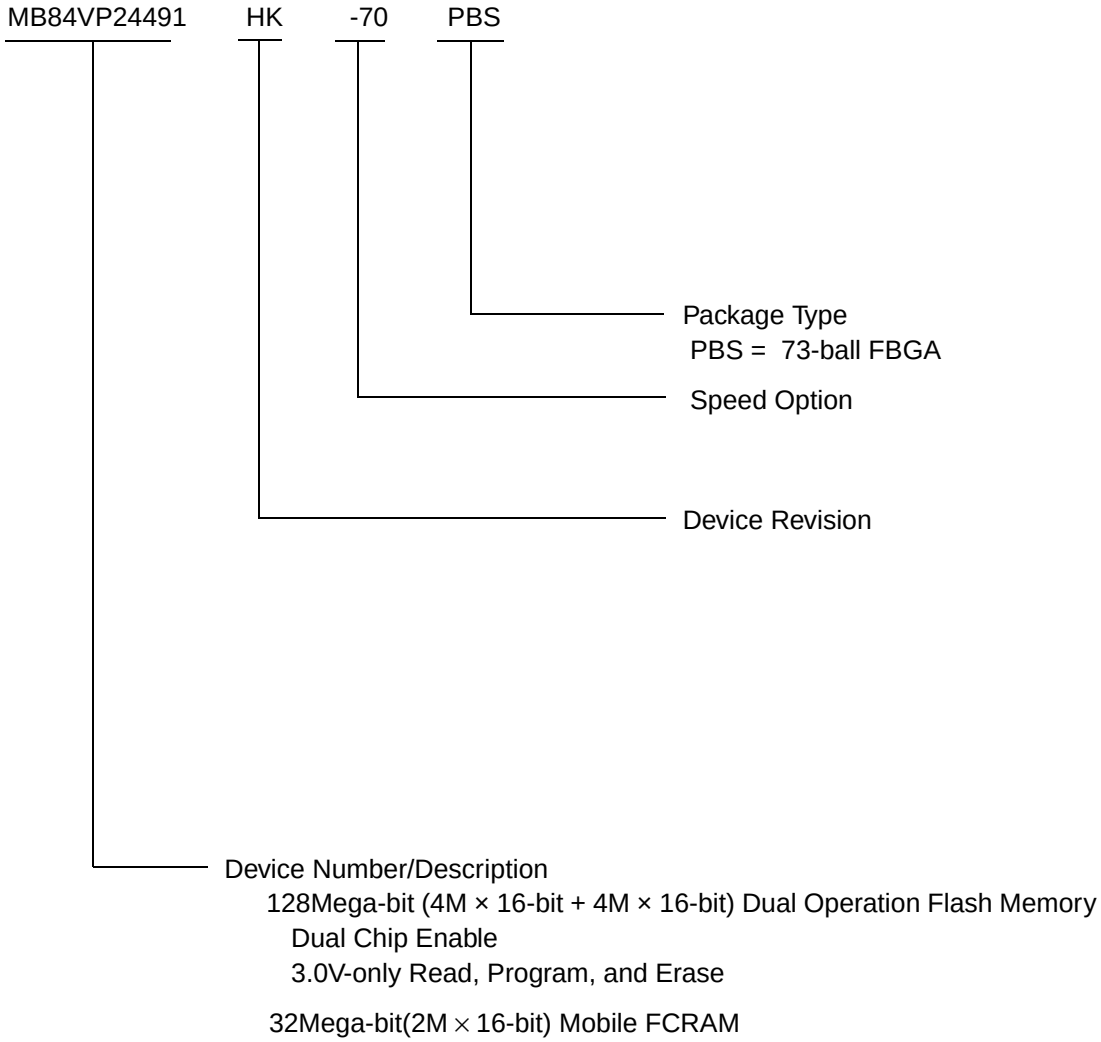
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

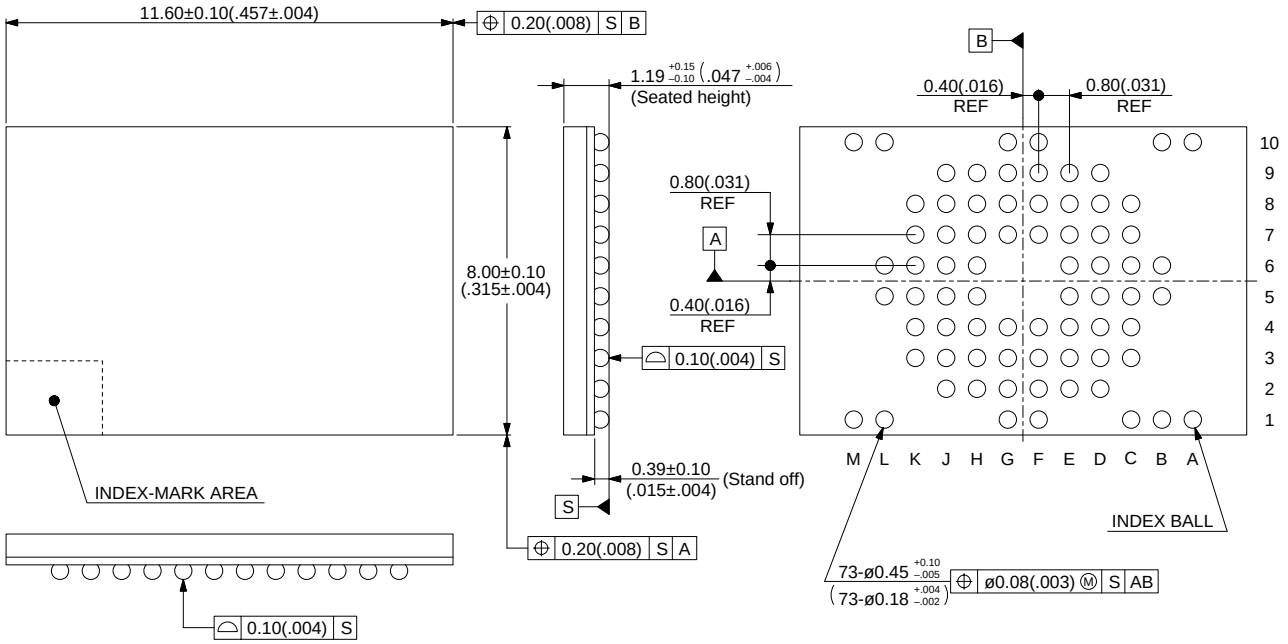
- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{RESET}$. Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.
- Without the high voltage (V_{ID}) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

73-ball plastic FBGA
(BGA-73P-M03)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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