

ASSP For Screen Display Control

CMOS

On-Screen Display Controller

MB90099

■ DESCRIPTION

The MB90099 is an on-screen display controller for displaying text and graphics on the TV screen. The three-channel output control function, compact package and low voltage operation make this device suitable for on-screen displays in portable devices including camera-integrated VTRs and digital still cameras.

The MB90099 controls a display area of 28 characters by 12 lines, and provides 1,024 different characters, each composed of 12×18 dots. All 1,024 characters in font ROM can be set by the user. The display functions include a wealth of characters with qualifying functions such as character background shading (shadow casting) and individual character size setting, with 16-color display selection for each character. Also included are the line background, screen background, and sprite character functions, providing a wide variety of screen display capabilities.

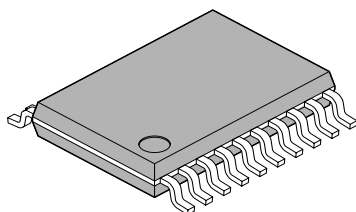
■ FEATURES

- Character screen configuration : 28 characters $\times$ 12 lines (maximum)
- Character types : 1,024 characters (integrated in ROM, user definable through the entire area)

(Continued)

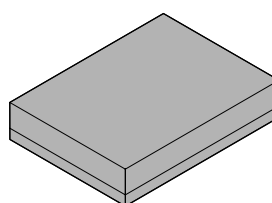
■ PACKAGE

20-pin plastic SSOP



(FPT-20P-M03)

20-pin plastic FLGA



(LGA-20P-M01)

(Continued)

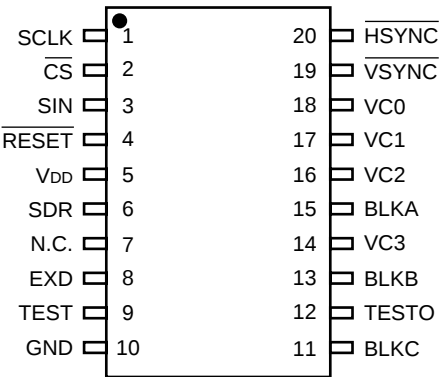
- Font configuration : 12 × 18 dots (font ROM configuration)
Horizontal/vertical character display size setting enabled.
Two horizontal width settings (S/L) per character.
S size : 6 dots
L size : 12 dots
Two vertical height settings (HA/HB) per line.
HA : 18 dots
HB : 12 dots
- Display modes : Character trimming : Enabled/Disabled (set for each line)
Character background :
None/Solid-fill/Shaded background (concave) /Shaded background (convex)
(set for each character)
Horizontal character merge/independent display with shaded background (set for each character)
Vertical line merge/independent display with shaded background (set for each line)
Character background display extended to line spacings : Enabled/Disabled (set for each line)
Line background :
None/Solid-fill/Shaded background (concave) /Shaded background (convex)
(set for each line)
(Display extends into left and right screen margins and into line spacings)
Character enlargement :
4 types : Normal, Double width, Double height, Double width × double height (set for each line)
Enlarged character dot interpolation function (set for each line)
- Character screen display position control : Horizontal display position :
Control in 2-dot units (movable through the entire screen)
Vertical display position :
Control in 2-dot units (movable through the entire screen)
Line spacing control :
Control in 1-dot units (set between 0 to 7 dots for each line, applied simultaneously to two areas above and below the line)
- Sprite character control : Sprite character display : Enable/Disabled
Sprite character types : 256 types (character codes 000_H to 0FF_H)
Sprite character trimming : Enabled/Disabled
Sprite character configuration : 2 types : 1 character/Stack of 2 characters
Sprite character horizontal display position : Control in 1-dot units (movable through the entire screen)
Sprite character vertical display position : Control in 1-dot units (movable through the entire screen)
- Screen background control : Screen background color : Enabled/Disabled

- Display colors :
 - Character color : 16 colors (set for each character)
 - Character trimming color : 16 colors (set for each line)
 - Character background color : 16 colors (set for each character) *
 - Line background color : 16 colors (set for each line)
 - Screen background color : 16 colors
 - Sprite character color : 16 colors
 - Sprite character trimming color : 16 colors
 - Shaded background frame highlight color : 16 colors
 - Shaded background frame shadow color : 16 colors
- Display signal output :
 - Color signal output : 4 bits (supports 16 colors)
 - Display period signals : 3 channels (output selector circuit provided)
- External interface :
 - 16-bit serial input :
 - Chip select
 - Serial clock
 - Serial data
- Package :
 - SSOP-20
 - FLGA-20
- Supply voltage :
 - 2.4 V to 3.6 V

* : Character background color (color code) = "0" is transparent (displays lower-layer color) .

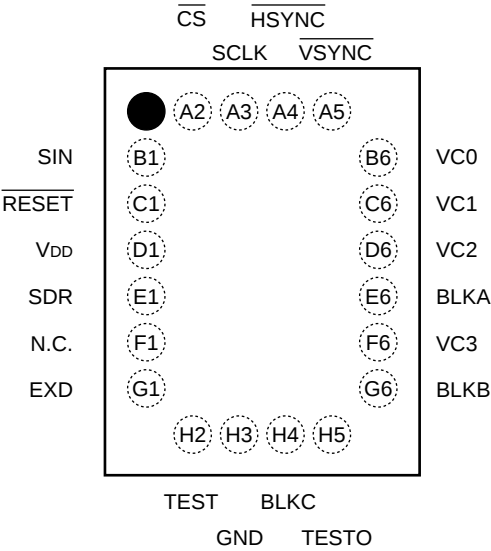
PIN ASSIGNMENTS

(TOP VIEW)



SSOP-20
(FPT-20P-M03)

(TOP VIEW)



FLGA-20
(LGA-20P-M01)

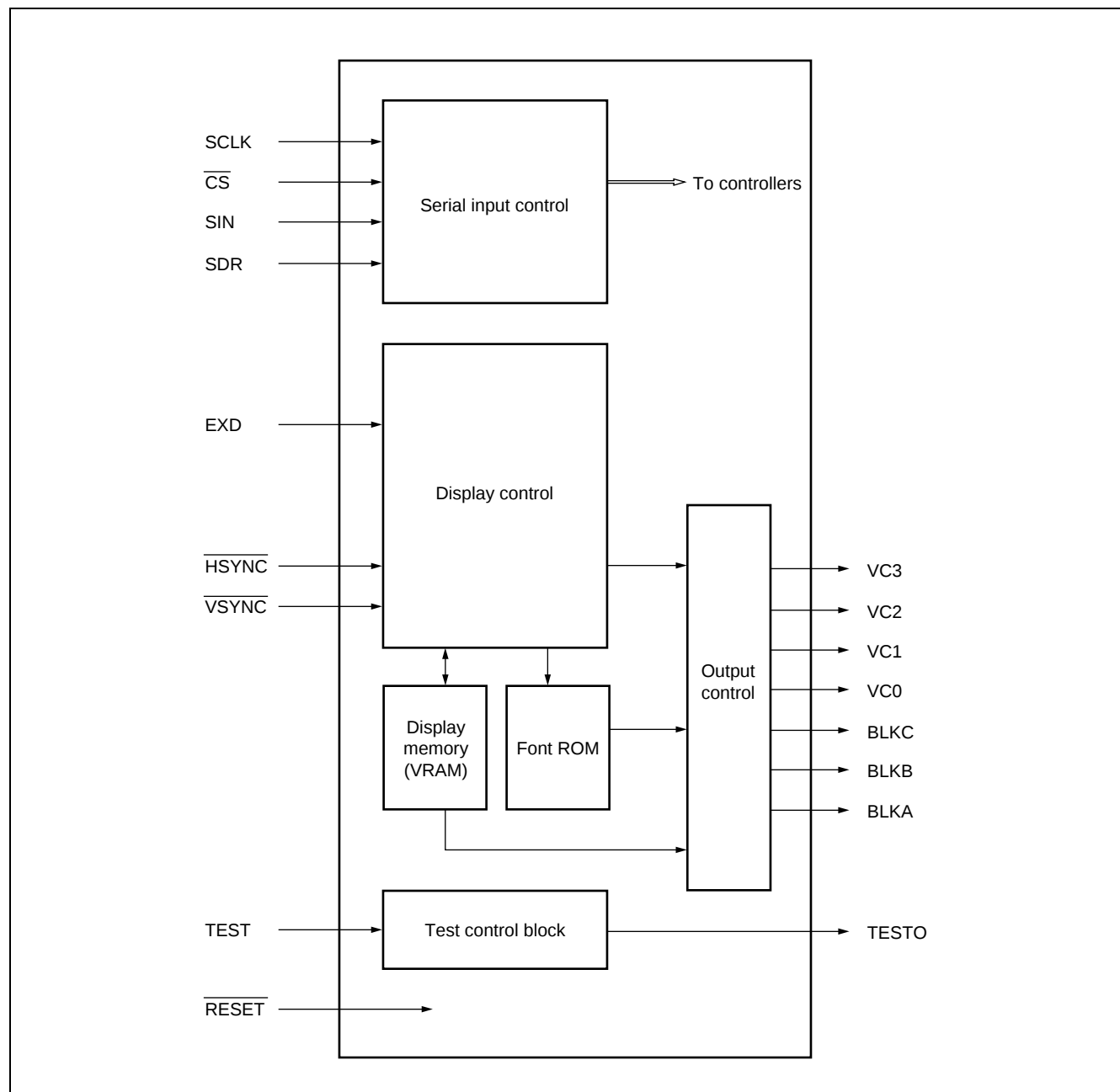
PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Circuit type	Function
SSOP	FLGA				
1	A3	SCLK	I	A	Shift clock input pin for serial transfer. This pin has an internal pull-up resistor.
2	A2	$\overline{\text{CS}}$	I	A	Chip select pin. Input a low level signal during serial transfer. This pin has an internal pull-up resistor.
3	B1	SIN	I	A	Serial data input pin. This pin has an internal pull-up resistor.
4	C1	$\overline{\text{RESET}}$	I	B	Reset input pin. Input a low level signal at power-on time.
5	D1	V _{DD}	—	—	+3 V power supply pin.
6	E1	SDR	I	C	Data input direction select pin for serial transfer. Input a low level signal at LSB-first transfer mode, or a high level signal at MSB-first transfer mode.
7	F1	N.C.	—	—	Not connected. This pin should be left open.
8	G1	EXD	I	B	Display dot clock input pin.
9	H2	TEST	I	C	LSI test input pin. Input a low level signal during normal use.
10	H3	GND	—	—	Ground pin.
11	H4	BLKC	O	D	Display period signal output pin for output channel C.
12	H5	TESTO	O	D	LSI test output pin. This pin should be left open during normal use.
13	G6	BLKB	O	D	Display period signal output pin for output channel B.
15	E6	BLKA	O	D	Display period signal output pin for output channel A.
14 16 17 18	F6 D6 C6 B6	VC3 VC2 VC1 VC0	O O O O	D	Color code signal output pins.
19	A5	$\overline{\text{VSYNC}}$	I	B	Vertical synchronization signal input pin.
20	A4	$\overline{\text{HSYNC}}$	I	B	Horizontal synchronization signal input pin.

I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		CMOS level, hysteresis input, pull-up resistance (25 kΩ to 200 kΩ) .
B		CMOS level, hysteresis input.
C		CMOS level input.
D		CMOS level output.

■ BLOCK DIAGRAM



■ COMPONENT ELEMENTS

- Serial input control block
Receives serial commands and data. Decodes commands, and allocates commands and data to the appropriate control blocks.
- Display control block
Performs display control functions synchronized with the input sync signals.
- Display memory (VRAM) block
VRAM memory for character data (24 bits × 28 characters × 12 lines) and line data (24 bits × 12 lines) .
- Font ROM block
ROM memory for display character fonts. Configured for 1,024 characters of 12 dots × 18 dots.
- Output control block
Generates output signals by applying display processing to the font data read from the font ROM.
- Test control block
Circuits for factory testing of the LSI before delivery.

■ ABSOLUTE MAXIMUM RATINGS

(V_{GND} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{DD}	V _{GND} – 0.5	V _{GND} + 4.0	V	
Input voltage	V _{IN}	V _{GND} – 0.5	V _{DD} + 0.5	V	
Output voltage	V _{OUT}	V _{GND} – 0.5	V _{DD} + 0.5	V	
Power consumption	P _d	—	100	mW	
Operating temperature	T _a	–20	+70	°C	
Storage temperature	T _{stg}	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{GND} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{DD}	2.4	3.6	V	
“H” level input voltage 1	V _{IHS}	0.8 × V _{DD}	V _{DD} + 0.3	V	*1
“L” level input voltage 1	V _{ILS}	V _{GND}	0.2 × V _{DD}	V	*1
“H” level input voltage 2	V _{IH}	0.7 × V _{DD}	V _{DD} + 0.3	V	*2
“L” level input voltage 2	V _{IL}	V _{GND}	0.3 × V _{DD}	V	*2
Operating temperature	T _a	–20	+70	°C	

*1 : Input pins excluding TEST and SDR pins.

*2 : TEST and SDR input pins.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

($V_{GND} = 0\text{ V}$, $T_a = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

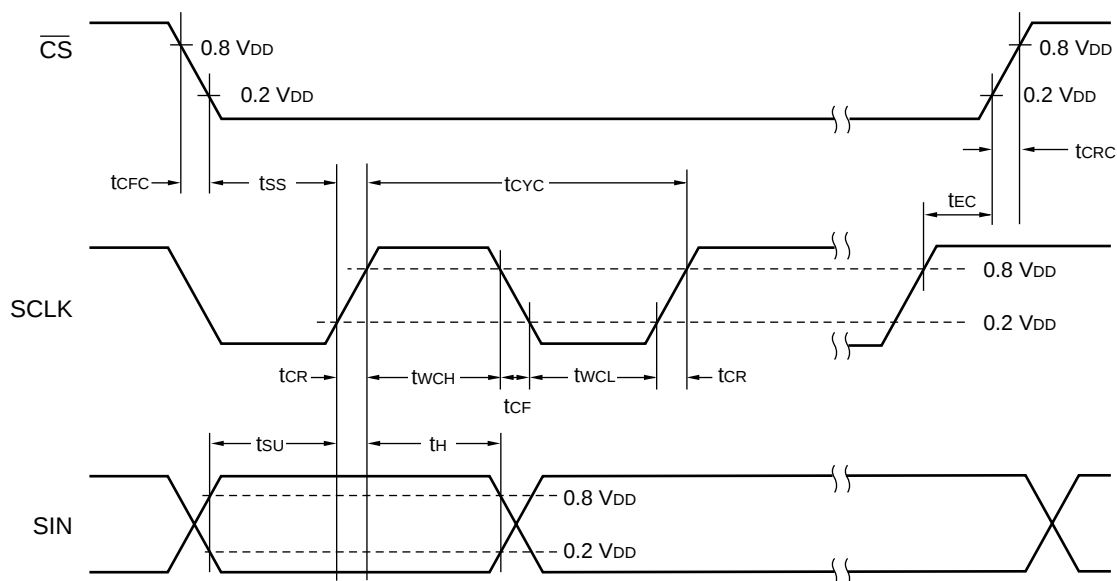
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
"H" level output voltage	V_{OH}	VC3, VC2, VC1, VC0, BLKC, BLKB, BLKA	$V_{DD} = 3.3\text{ V}$ $I_{OH} = -4\text{ mA}$	$V_{DD} - 0.5$	—	V_{DD}	V
"L" level output voltage	V_{OL}		$V_{DD} = 3.3\text{ V}$ $I_{OL} = 4\text{ mA}$	V_{GND}	—	0.4	V
"H" level input current	I_{IH}	SDR, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, EXD, TEST, $\overline{\text{RESET}}$	$V_{DD} = 3.3\text{ V}$ $V_{IH} = V_{DD}$	—	—	+10	μA
"L" level input current	I_{IL}		$V_{DD} = 3.3\text{ V}$ $V_{IL} = 0\text{ V}$	—	—	-10	μA
Pull-up resistance	R_{PULL}	SIN, SCLK, $\overline{\text{CS}}$	$V_{DD} = 3.3\text{ V}$	25	50	200	$\text{k}\Omega$
Power supply current	I_{CC}	V_{DD}	$V_{DD} = 2.4\text{ V}$ $f_{DC} = 8\text{ MHz}$	—	—	5	mA
			$V_{DD} = 3.6\text{ V}$ $f_{DC} = 8\text{ MHz}$	—	—	6	mA
Input capacitance	C	Except V_{DD} , GND	—	—	—	16	pF

2. AC Characteristics

(1) Serial input timings

($V_{DD} = 2.4 \text{ V to } 3.6 \text{ V}$, $V_{GND} = 0 \text{ V}$, $T_a = -20 \text{ }^{\circ}\text{C to } +70 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Unit
			Min.	Max.	
Shift clock cycle time	t_{CYC}	SCLK	250	—	ns
Shift clock pulse width	t_{WCH}	SCLK	100	—	ns
	t_{WCL}		100	—	ns
Shift clock signal rise/fall time	t_{CR}	SCLK	—	200	ns
	t_{CF}		—	200	ns
Shift clock start time	t_{SS}	SCLK	100	—	ns
Data setup time	t_{SU}	SIN	100	—	ns
Data hold time	t_H		50	—	ns
Chip select end time	t_{EC}	$\overline{CS}$	100	—	ns
Chip select signal rise/fall time	t_{CRC}	$\overline{CS}$	—	200	ns
	t_{CFC}		—	200	ns



(2) Vertical and horizontal sync signal input timing

($V_{DD} = 2.4 \text{ V}$ to 3.6 V , $V_{GND} = 0 \text{ V}$, $T_a = -20 \text{ }^{\circ}\text{C}$ to $+70 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Unit
			Min.	Max.	
Horizontal sync signal rise time	t_{HR}	$\overline{\text{HSYNC}}$	—	200	ns
Horizontal sync signal fall time	t_{HF}		—	200	ns
Vertical sync signal rise time	t_{VR}	$\overline{\text{VSYNC}}$	—	200	ns
Vertical sync signal fall time	t_{VF}		—	200	ns
Horizontal sync signal pulse width *1	t_{WH}	$\overline{\text{HSYNC}}$	18	—	Dot clock
			—	6	μs
Vertical sync signal setup time1 *2 (Except for $VVE = 1$, $VHE = 1$, $HE = 1$) *3	t_{VS}	$\overline{\text{VSYNC}}$	4	$1H - 4$	Dot clock
Vertical sync signal setup time2 *2 ($VVE = 1$, $VHE = 1$, $HE = 1$) *3	t_{VS}	$\overline{\text{VSYNC}}$	- 6	$1H - 14$	Dot clock
Vertical sync signal detection hold time	t_{VH}	$\overline{\text{VSYNC}}$	2	—	H
Vertical sync signal pulse width	t_{wv}	$\overline{\text{VSYNC}}$	2	20	H

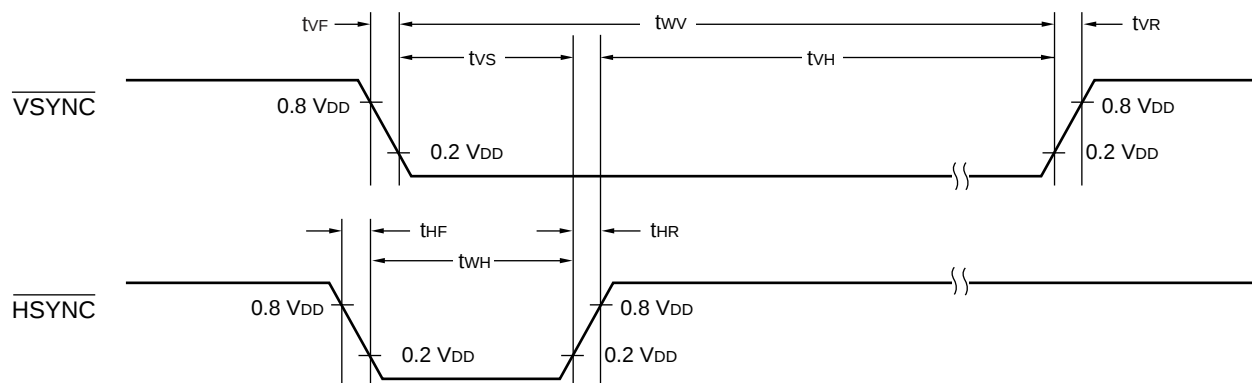
*1 : During the horizontal sync signal pulse period, the MB90099 stops its internal operation, disabling writing to the internal VRAM. Therefore, the horizontal sync signal pulse width and VRAM write cycle (command 2 or command 4 issuance cycle) should be set so that the horizontal sync signal pulse width is shorter than the VRAM write cycle.

*2 : In the vertical sync signal detection cycle, do not change the vertical sync signal (detection edge) when it is close to the horizontal sync signal edge. This may result in distortion of the display due to fluctuations in the sync signal.

*3 : VVE , VHE and HE are control bits of Command 13-0 (I/O pin control) .

$\overline{\text{VSYNC}}$: Leading-edge operation ($VVE = 0$)

$\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the trailing edge ($VHE = 1$)

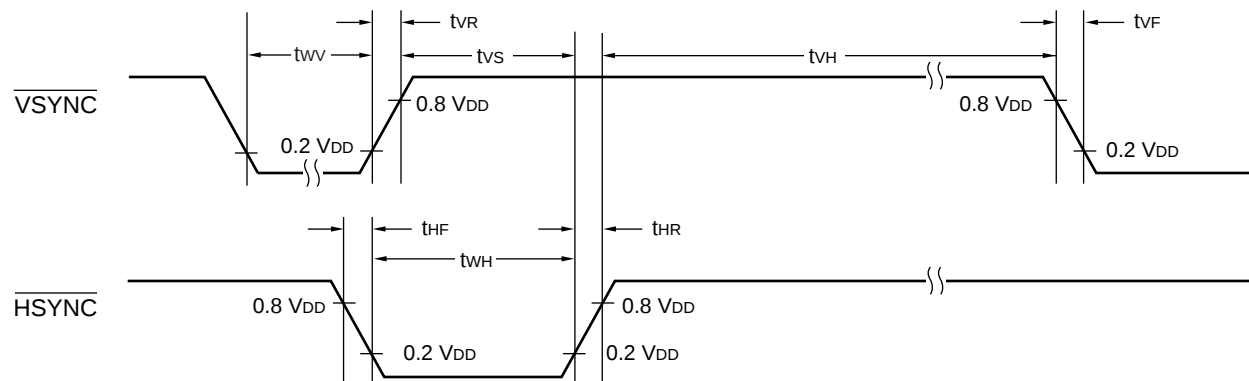


(Continued)

(Continued)

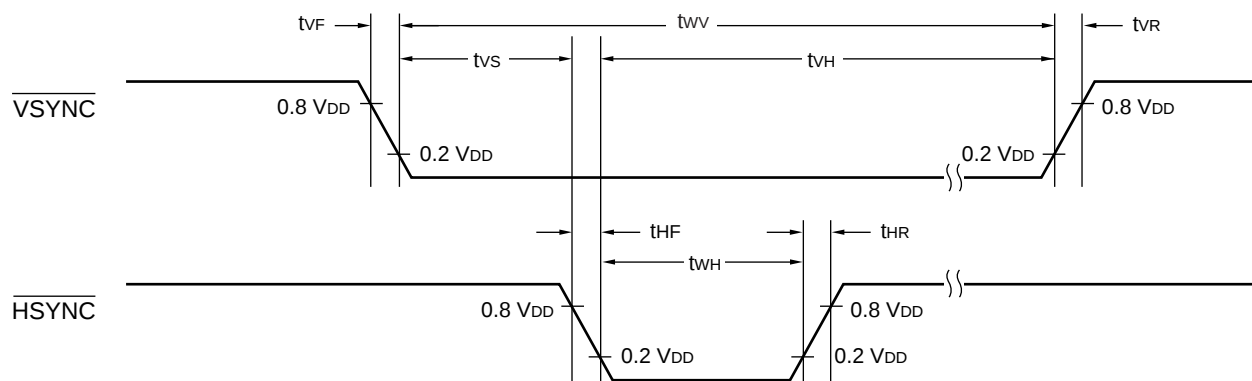
$\overline{\text{VSYNC}}$: Trailing-edge operation ($\text{VVE} = 1$)

$\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the trailing edge ($\text{VHE} = 1$ and $\text{HE} = 0$)



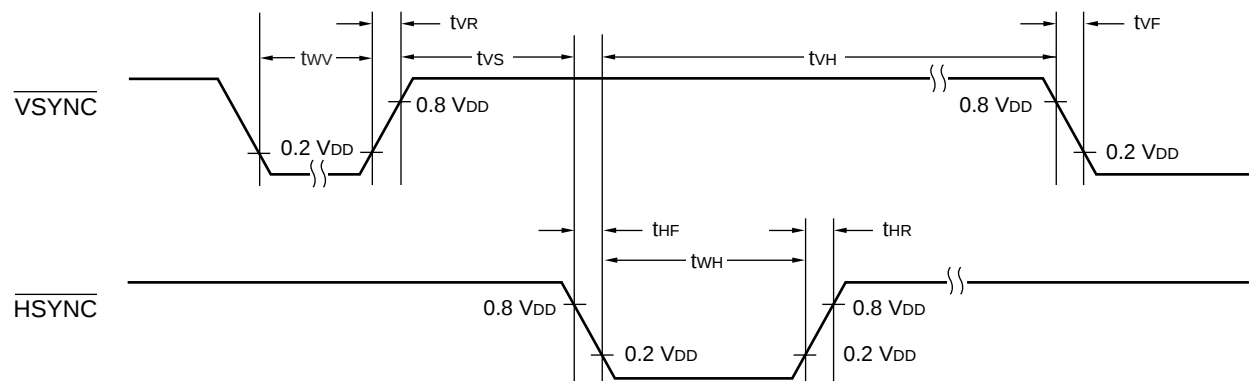
$\overline{\text{VSYNC}}$: Leading-edge operation ($\text{VVE} = 0$)

$\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the leading edge ($\text{VHE} = 0$)



$\overline{\text{VSYNC}}$: Trailing-edge operation ($\text{VVE} = 1$)

$\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the leading edge ($\text{VHE} = 0$) or ($\text{VHE} = 1$ and $\text{HE} = 1$)



Note : The above diagrams assume that I/O pin control command (command 13-0) has set the sync signal input logic control setting (SIX bit) to negative logic ("0") . However, if the positive logic setting (SIX bit = "1") is used, the H and L levels are reversed.

(3) Dot clock external input timing

($V_{DD} = 2.7 \text{ V to } 3.3 \text{ V}$, $V_{GND} = 0 \text{ V}$, $T_a = -20 \text{ }^{\circ}\text{C to } +70 \text{ }^{\circ}\text{C}$)

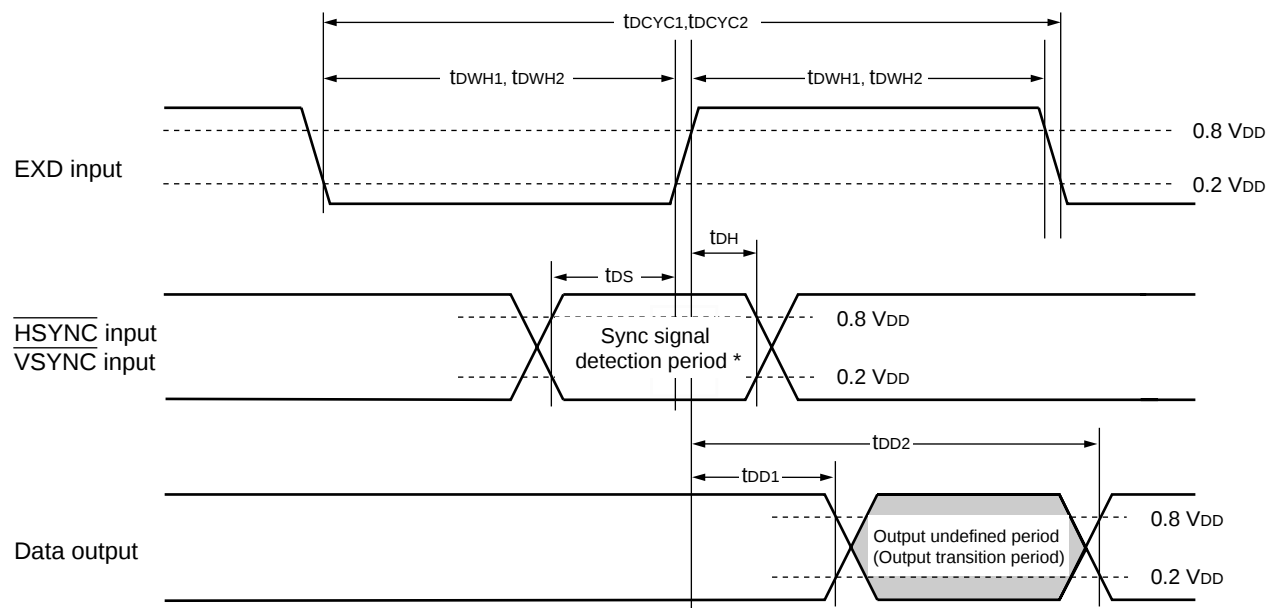
Parameter	Symbol	Pin name	Value		Unit	Note
			Min.	Max.		
Dot clock cycle time	t_{DCYC1}	EXD	112	166	ns	*1
	t_{DCYC2}	EXD	56	83	ns	*2
Dot clock pulse time	t_{DWH1}	EXD	48	—	ns	*1
	t_{DWL1}		48	—	ns	
	t_{DWH2}	EXD	24	—	ns	*2
	t_{DWL2}		24	—	ns	
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ setup time	t_{DS}	$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	13	—	ns	*3
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ hold time	t_{DH}		0	—	ns	*3
Data output delay time 1	t_{DD1}	VC3, VC2, VC1, VC0, BLKA, BLKB, BLKC	7	t_{DD2}	ns	*3
Data output delay time 2	t_{DD2}		t_{DD1}	45	ns	

Note : The above items assume a supply voltage of $V_{DD} = 2.7 \text{ V to } 3.3 \text{ V}$.

*1 : Assuming input frequency = dot clock $\times$ 1.

*2 : Assuming input frequency = dot clock $\times$ 2.

*3 : Assuming input frequency = dot clock $\times$ 1 or dot clock $\times$ 2.



AC measurement conditions

$C = 70 \text{ pF}$ $V_{OH} = 0.8 V_{DD}$
 $t_r = 5 \text{ ns}$ $V_{OL} = 0.2 V_{DD}$
 $t_f = 5 \text{ ns}$ $V_{IH} = 0.8 V_{DD}$
 $V_{IL} = 0.2 V_{DD}$

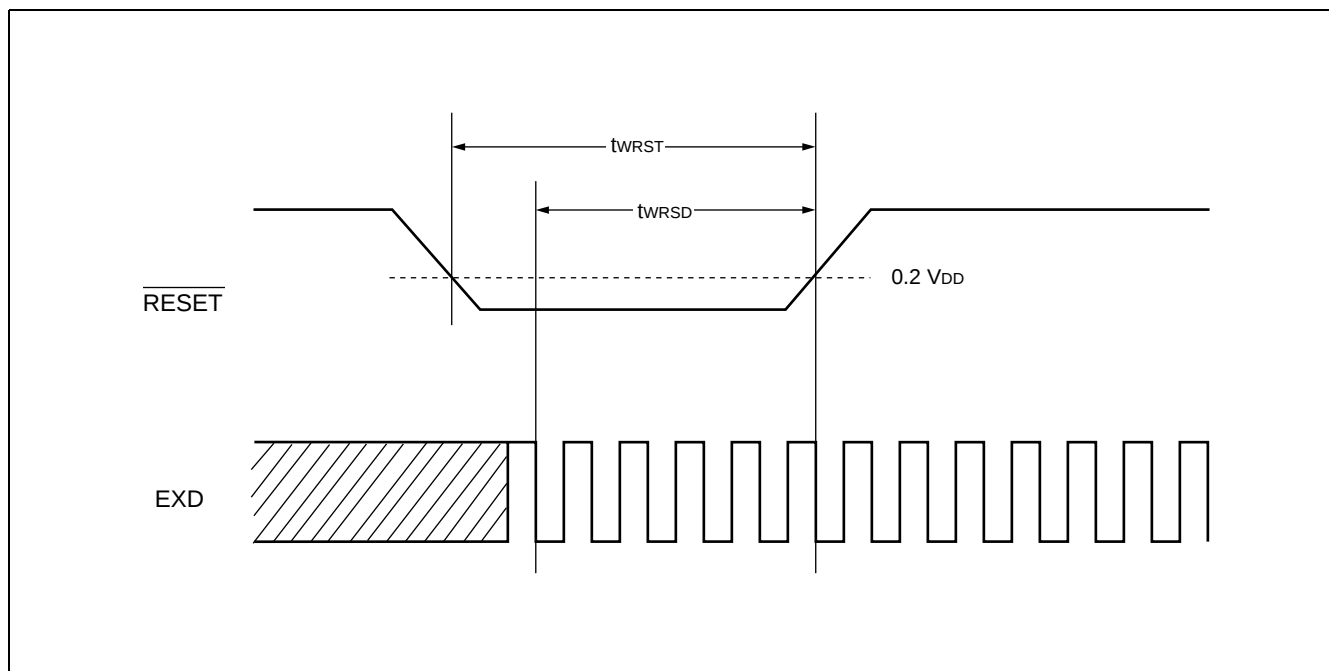
* : Do not vary the input sync signal during the sync signal detection period.
Changes in the signal during this period may cause distortion in the display.

(4) Reset input timing

($V_{DD} = 2.4 \text{ V to } 3.6 \text{ V}$, $V_{GND} = 0 \text{ V}$, $T_a = -20 \text{ }^{\circ}\text{C to } +70 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Unit	Note
			Min.	Max.		
Reset pulse width	t_{WRST}	$\overline{\text{RESET}}$	1	—	μs	
Clock input	t_{WRSD}	EXD	5	—	Dot clock	*

* : Clock input is required during reset.



■ DISPLAY CONTROL COMMANDS

1. Command list

Com- mand no.	Function	Command code/data												
		15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
0	VRAM write address setting	0 0 0 0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0
1	Character data setting 1	0 0 0 1	MO1	MO0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0
2	Character data setting 2	0 0 1 0	MR	MS	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
3	Line control data setting 1	0 0 1 1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0
4	Line control data setting 2	0 1 0 0	LDS	LGS	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0
5-00	Screen output control 1A	0 1 0 1	0	0	0	0	SDS	UDS	0	DSP	0	OA2	OA1	OA0
5-01	Screen output control 1B	0 1 0 1	0	0	0	1	SOB	BGB	BLB	0	0	OB2	OB1	OB0
5-02	Screen output control 1C	0 1 0 1	0	0	1	0	SOC	BGC	BLC	0	0	OC2	OC1	OC0
5-2	Vertical display position control	0 1 0 1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
5-3	Horizontal display position control	0 1 0 1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0
6-1	Shaded background frame color control	0 1 1 0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0
7-3	Screen background control	0 1 1 1	1	1	0	0	0	0	0	0	U3	U2	U1	U0
8-0	Sprite character control 1	1 0 0 0	0	0	SFB	SFA	SF3	SF2	SF1	SF0	SC3	SC2	SC1	SC0
8-1	Sprite character control 2	1 0 0 0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
9-0	Sprite character control 4	1 0 0 1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
9-1	Sprite character control 5	1 0 0 1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
11-0	Screen extension control	1 0 1 1	0	0	0	0	0	EG0	0	0	0	0	0	0
11-2	Dot clock control 1	1 0 1 1	1	0	0	0	0	0	0	0	0	DC2	DC1	DC0

(Continued)

(Continued)

Com- mand no.	Function	Command code/data												
		15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
13-0	I/O pin control	1 1 0 1	0	0	VVE	VHE	HE	0	SIX	0	0	0	DBX	DCX
13-1	Horizontal blanking control 1	1 1 0 1	0	1	0	0	0	0	BB5	BB4	BB3	BB2	BB1	BB0
13-2	Horizontal blanking control 2	1 1 0 1	1	0	0	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

2. Command Description

• Command 0 (VRAM write address setting)

Command 0 sets the write address in VRAM, and controls the execution of "VRAM fill". The write address is specified by row and column addresses. VRAM fill is activated by executing character data setting 2 (command 2).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0

AY3 to AY0 : Row address (0 to B_H)

AX4 to AX0 : Column address (0 to 1B_H)

FL : VRAM Fill control (0 : OFF, 1 : ON)

• Command 1 (Character data setting 1)

Command 1 specifies character data. The character data is written to VRAM and reflected on the screen by the execution of command 2 (character data setting 2).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MO1	MO0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0

MO1, MO0 : Character output control

MM1, MM0 : Character background control

(0, 0 : Off)

(0, 1 : Solid fill)

(1, 0 : Concaved shaded)

(1, 1 : Convexed shaded)

MC3 to MC0 : Character color (16 colors)

MB3 to MB0 : Background color (16 colors)

• Command 2 (Character data setting 2)

Command 2 writes additional character data to the location in VRAM spacificd by command 0 (VRAM write address setting),along with the character data set by command 1 (character data setting 1).

The VRAM write address is automatically incremented after command 2 is executed.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	MR	MS	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

MR : Shaded background succeeding character merge control

(0 : Not merged with succeeding character)

(1 : Merged with succeeding character)

MS : Character horizontal size control

(0 : S size, 6 dots)

(1 : L size, 12 dots)

M9 to M0 : Character code

• Command 3 (Line control data setting 1)

Command 3 specifies line control data. The line control data is written to VRAM and reflected on the screen by the execution of command 4 (line control data setting 2) .

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0

LHS : Line character vertical size type control

(0 : Character vertical size A)

(1 : Character vertical size B)

LW2 to LW0 : Line spacing control

(0 to 7 dots, in 1-dot units)

LF3 to LF0 : Trimming color (16 colors)

LFD, LFC : Trimming output control

(0, 0 : All Off)

(0, 1 : Trimming On for a character only, no character background)

(1, 0 : Trimming On for a solid-fill character or no character background)

(1, 1 : All On)

LFB, LFA : Trimming control

(0, 0 : Trimming Off)

(0, 1 : Reserved (setting prohibited))

(1, 0 : Reserved (setting prohibited))

(1, 1 : Eight-direction trimming)

• Command 4 (Line control data setting 2)

Command 4 specifies additional line control data and writes this data, along with the line control data set by command 3 (line control data setting 1) to the row address in VRAM specified by command 0 (VRAM write address setting) .

Executing this command will not alter the VRAM write address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	LDS	LGS	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0

LDS : Line character output control (control of a character + trimming + character background)

(0 : Off, 1 : On)

LGS : Line enlargement interpolation control

(0 : Off, 1 : On)

LG1, LG0 : Line enlargement control

(0, 0 : Normal)

(0, 1 : Double width)

(1, 0 : Double height)

(1, 1 : Double width × double height)

LE : Character background extension control

(0 : Normal, 1 : Extended)

LD : Shaded background succeeding line merge control

(0 : Independent)

(1 : Merged with succeeding line)

LM1, LM0 : Line background control

(0, 0 : Off)

(0, 1 : Solid fill)

(1, 0 : Concaved shaded)

(1, 1 : Convexed shaded)

L3 to L0 : Line background color (16 colors)

• Command 5-00 (Screen output control 1A)

Command 5-00 controls screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	SDS	UDS	0	DSP	0	OA2	OA1	OA0

SDS : Sprite character output control

(0 : Off, 1 : On) *

UDS : Screen background output control

(0 : Off, 1 : On) *

DSP : Display output control (Control of a character + trimming + character background + line background)

(0 : Off, 1 : On) *

OA2 to OA0 : Output-A character control (8 types)

* : Input of an 'L' level signal to the $\overline{\text{RESET}}$ pin will initialize SDS = 0, UDS = 0, and DSP = 0.

• Command 5-01 (Screen output control 1B)

Command 5-01 controls output-B screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1	SOB	BGB	BLB	0	0	OB2	OB1	OB0

SOB : Output-B sprite character output control

(0 : Off, 1 : On)

BGB : Output-B screen background output control

(0 : Off, 1 : On)

BLB : Output-B line background output control

(0 : Off, 1 : On)

OB2 to OB0 : Output-B character control (8 types)

• Command 5-02 (Screen output control 1C)

Command 5-02 controls output-C screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0	SOC	BGC	BLC	0	0	OC2	OC1	OC0

SOC : Output-C sprite character output control
(0 : Off, 1 : On)

BGC : Output-C screen background output control
(0 : Off, 1 : On)

BLC : Output-C line background output control
(0 : Off, 1 : On)

OC2 to OC0 : Output-C character control (8 types)

• Command 5-2 (Vertical display position control)

Command 5-2 controls the vertical display position on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y8 to Y0 : Vertical display position control (0 to 1022 in 2-dot units)

• Command 5-3 (Horizontal display position control)

Command 5-3 controls the horizontal display position on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0

X8 to X0 : Horizontal display position control (0 to 1022 in 2-dot units)

• Command 6-1 (Shaded background frame color control)

Command 6-1 controls the frame color of the shaded background.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0

BH3 to BH0 : Shaded background frame highlight color (16 colors)

BS3 to BS0 : Shaded background frame shadow color (16 colors)

• Command 7-3 (Screen background control)

Command 7-3 controls the screen background color.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	0	0	0	0	U3	U2	U1	U0

U3 to U0 : Screen background color (16 colors)

• Command 8-0 (Sprite character control 1)

Command 8-0 controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	SFB	SFA	SF3	SF2	SF1	SF0	SC3	SC2	SC1	SC0

SFB, SFA : Sprite character trimming control

(0, 0 : Trimming Off)

(0, 1 : Reserved)

(1, 0 : Reserved)

(1, 1 : Eight-direction trimming)

SF3 to SF0 : Sprite character trimming color (16 colors)

SC3 to SC0 : Sprite character color (16 colors)

• Command 8-1 (Sprite character control 2)

Command 8-1 controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SD1, SD0 : Sprite character configuration control

(0, 0 : 1 character)

(0, 1 : Reserved (setting prohibited))

(1, 0 : Stack of 2 characters)

(1, 1 : Reserved (setting prohibited))

SM7 to SM0 : Sprite character code

(000_H to 0FF_H for 256 different characters)

• Command 9-0 (Sprite character control 4)

Command 9-0 controls the vertical display position of sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0

SY9 to SY0 : Sprite character vertical display position control

(0 to 1023 in 1-dot units)

• Command 9-1 (Sprite character control 5)

Command 9-1 controls the horizontal display position of sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX9 to SX0 : Sprite character horizontal display position control

(0 to 1023 in 1-dot units)

• Command 11-0 (Screen extension control)

(Reserved)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	EG0	0	0	0	0	0	0

EG0 : (Reserved)

(0 : Normal)

(1 : Reserved (setting prohibited))

• Command 11-2 (Dot clock control 1)

Command 11-2 controls dot clock selection.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	0	0	0	0	0	0	0	DC2	DC1	DC0

DC2 to DC0 : Dot clock selection control

(0, 1, 0) : External dot clock input

(0, 1, 1) : Frequency-doubled external dot clock input

• Command 13-0 (I/O pin control)

Command 13-0 controls I/O pin functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	0	VVE	VHE	HE	0	SIX	0	0	0	DBX	DCX

VVE : Edge selection for vertical synchronization detection*1

(0 : Leading edge, 1 : Trailing edge)

VHE : HSYNC edge selection for vertical synchronization detection*1

(0 : Leading edge, 1 : Trailing edge)

HE : Edge selection for horizontal synchronization operation*1

(0 : Trailing edge, 1 : Leading edge)

SIX : Logic control for sync signal input

(0 : Negative logic, 1 : Positive logic)

DCX : Logic control for display color signal output

(0 : Positive logic, 1 : Negative logic) *2

DBX : Logic control for display output period signal

(0 : Positive logic, 1 : Negative logic) *2

*1 : When it is set up VVE = 1, VHE = 1 and HE = 1, the vertical sync detection HSYNC edge is the standard of "Leading edge".

VVE	VHE	HE	Contents of vertical sync detection	Position of vertical sync detection*
0	0	0	Detection of VSYNC Leading edge	HSYNC Leading edge
0	0	1	Detection of VSYNC Leading edge	HSYNC Leading edge
0	1	0	Detection of VSYNC Leading edge	HSYNC Trailing edge
0	1	1	Detection of VSYNC Leading edge	HSYNC Trailing edge
1	0	0	Detection of VSYNC Trailing edge	HSYNC Leading edge
1	0	1	Detection of VSYNC Trailing edge	HSYNC Leading edge
1	1	0	Detection of VSYNC Trailing edge	HSYNC Trailing edge
1	1	1	Detection of VSYNC Trailing edge	HSYNC Leading edge + 10 clock

* : If there is the change of level for direction of VSYNC pin signal detection in the vicinity of vertical sync detection, it may occur disorder in the display (deflection of vertical direction) . Input the meaningful edge of VSYNC signal without this position of vertical sync detection.

*2 : Input of an 'L' level signal to the $\overline{\text{RESET}}$ pin will initialize DCX = 0, and DBX = 0.

• Command 13-1 (Horizontal blanking control 1)

Command 13-1 controls the back porch of the horizontal blanking function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	1	0	0	0	0	BB5	BB4	BB3	BB2	BB1	BB0

BB5 to BB0 : Back porch control (0 to 126, in 2-dot units)

• Command 13-2 (Horizontal blanking control 2)

Command 13-2 controls the front porch of the horizontal blanking function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	0	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

BF8 to BF0 : Front porch control (0 to 1022, in 2-dot units)

3. Notes on Issuing Commands

(1) Initialization

When a reset signal is input ("L" level signal input to the $\overline{\text{RESET}}$ pin), the MB90099 enters display-off state(*). The contents of VRAM (the character RAM and the line RAM) are undefined.

Immediately after release of the input signal to the MB90099, issue the following commands to initialize control operation.

- Dot clock control 1 (command 11-2)
- I/O pin control (command 13-0)

This must be done before setting all command data and all RAM contents. (VRAM settings require normal dot clock input and normal sync signal input.)

* : The reset input initializes control bits as follows.

Screen output control 1A (command 5-00)

SDS = 0 Sprite Off

UDS = 0 Screen background Off

DSP = 0 Character, character background, line background Off

I/O pin control (command 13-0)

DCX = 0 VC0, VC1, VC2, VC3 pins set to positive logic output

DBX = 0 BLKA, BLKB, BLKC pins set to positive logic output

(2) Command refresh

Command data to the MB90099 and the contents of internal VRAM are stored as long as power is supplied to the MB90099. However, there may be cases in which the serial control, sync, or dot clock signals become abnormal due to causes such as external noise, preventing the internal registers and VRAM from being set properly. It is therefore recommended that all command data and VRAM data be refreshed periodically to ensure that this data is correct.

(3) Command issue timing

When any control command, including a VRAM write command such as a character data setting or line control data setting command is issued, the command is executed immediately and the result is reflected on the screen. When such a command is issued during a display period, the display in the relevant field may experience momentary distortion. To avoid this, it is recommended that commands be issued during the vertical blanking interval. However that with a command 5-00 (screen output control 1A) in which one or more of the DSP, SDS, or UDS control bits is switched from OFF to ON, the display will wait until the next vertical sync signal after the command is issued and the display will start from the top of the scanning field.

■ CONTENTS OF MB90099-001 (STANDARD PRODUCT) FONT DATA

0	1	2	3	4	5	6	7	8	9	:	:	?	!	.	.
000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F
Q	R	S	T	U	V	W	X	Y	Z	(	)	(	)	[	]
020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F
a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
q	r	s	t	u	v	w	x	y	z	+	-	*	/	=	¥
040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F
0	1	2	3	4	5	6	7	8	9	”	’	#	\$	%	&
050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F
Q	R	S	T	U	V	W	X	Y	Z	f	i	j	l	t	~
070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F
0	1	2	3	4	5	6	7	8	9	:	:	-	/	.	.
080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
Q	R	S	T	U	V	W	X	Y	Z	AM	PM	。	、	。	。
0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF
Ç	ü	é	â	ä	à	ã	ç	ê	ë	è	ï	î	ì	Å	Å
0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF
É	æ	Æ	ô	ö	ò	û	ù	ÿ	ö	ü	ç	£	£	£	£
0C0	0C1	0C2	0C3	0C4	0C5	0C6	0C7	0C8	0C9	0CA	0CB	0CC	0CD	0CE	0CF
á	í	ó	ú	ñ	Ñ	¡	¡	¡	¡	¡	¡	¡	¡	¡	¡
0D0	0D1	0D2	0D3	0D4	0D5	0D6	0D7	0D8	0D9	0DA	0DB	0DC	0DD	0DE	0DF
T															
0E0	0E1	0E2	0E3	0E4	0E5	0E6	0E7	0E8	0E9	0EA	0EB	0EC	0ED	0EE	0EF
▶	◀	▶	◀	●		☒	☒	☒	☒	○	●	▲	▼	■	■
0F0	0F1	0F2	0F3	0F4	0F5	0F6	0F7	0F8	0F9	0FA	0FB	0FC	0FD	0FE	0FF

あ	い	う	え	お	か	き	く	け	こ	さ	し	す	せ	そ	た
100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F
ち	つ	て	と	な	に	ぬ	ね	の	は	ひ	ふ	へ	ほ	ま	み
110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
む	め	も	や	ゆ	よ	ら	り	る	れ	ろ	わ	を	ん	。	”
120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F
ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ	タ
130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
チ	ツ	テ	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ	マ	ミ
140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F
ム	メ	モ	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ヲ	ン	。	”
150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
あ	い	う	え	お	や	ゆ	よ	ア	イ	ウ	エ	オ	ヤ	ユ	ヨ
160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F
抗	張	機	能	ノ	ハ	ク	ケ	コ	サ	シ	ス	セ	ソ	タ	チ
170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
日	月	火	水	木	金	土	年	曜	時	分	秒	録	画	再	生
180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F
早	送	巻	戻	停	止	毎	週	予	約	開	始	終	了	設	定
190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
標	準	倍	入	力	音	声	主	副	左	右	実	行	確	認	自
1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF
動	選	択	運	会	祝	学	卒	業	式	芸	富	士	通	文	字
1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
行	面	背	景	凹	凸	平	垂	直	表	示	位	置	間	隔	色
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF
縦	横	単	影	付	種	系	統	出	制	御	棒	信	号	補	刻
1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
午	前	後	中	切	大	前	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU
1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF
TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU	TSU
1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF

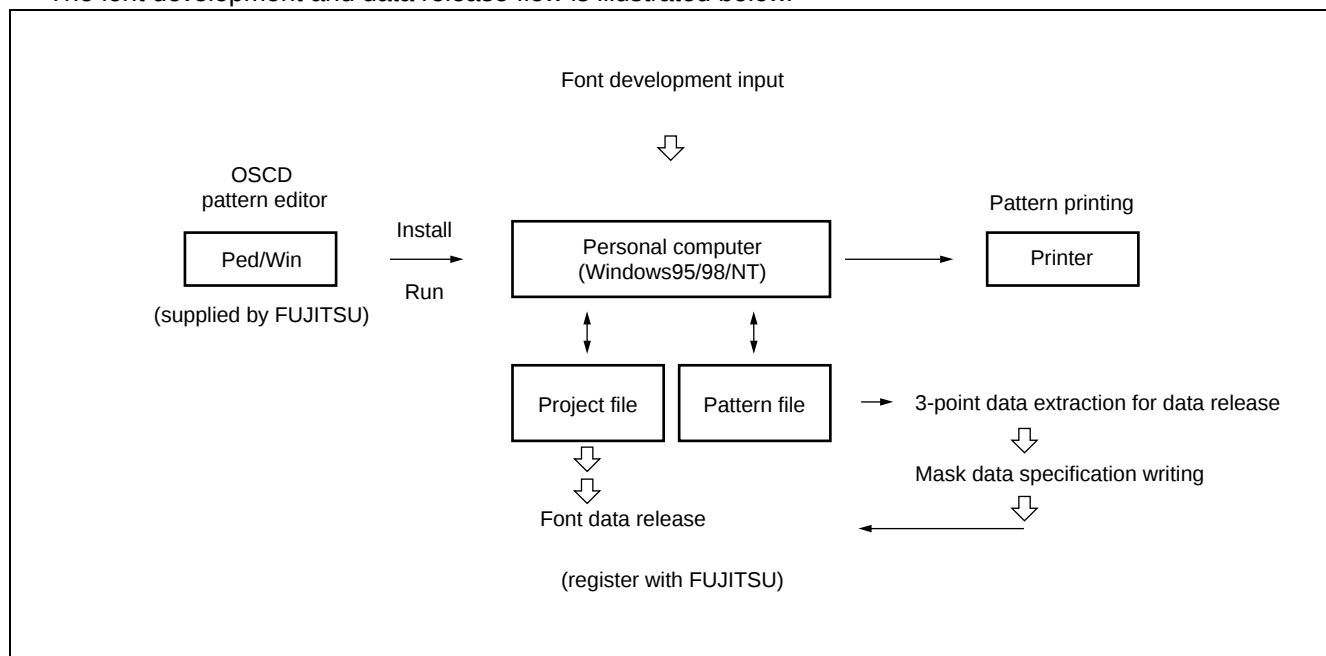
02 00	02 01	02 02	02 03	02 04	02 05	02 06	02 07	02 08	02 09	02 0A	02 0B	02 0C	02 0D	02 0E	02 0F
200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F
02 10	02 11	02 12	02 13	02 14	02 15	02 16	02 17	02 18	02 19	02 1A	02 1B	02 1C	02 1D	02 1E	02 1F
210	211	212	213	214	215	216	217	218	219	21A	21B	21C	21D	21E	21F
02 20	02 21	02 22	02 23	02 24	02 25	02 26	02 27	02 28	02 29	02 2A	02 2B	02 2C	02 2D	02 2E	02 2F
220	221	222	223	224	225	226	227	228	229	22A	22B	22C	22D	22E	22F
02 30	02 31	02 32	02 33	02 34	02 35	02 36	02 37	02 38	02 39	02 3A	02 3B	02 3C	02 3D	02 3E	02 3F
230	231	232	233	234	235	236	237	238	239	23A	23B	23C	23D	23E	23F
02 40	02 41	02 42	02 43	02 44	02 45	02 46	02 47	02 48	02 49	02 4A	02 4B	02 4C	02 4D	02 4E	02 4F
240	241	242	243	244	245	246	247	248	249	24A	24B	24C	24D	24E	24F
02 50	02 51	02 52	02 53	02 54	02 55	02 56	02 57	02 58	02 59	02 5A	02 5B	02 5C	02 5D	02 5E	02 5F
250	251	252	253	254	255	256	257	258	259	25A	25B	25C	25D	25E	25F
02 60	02 61	02 62	02 63	02 64	02 65	02 66	02 67	02 68	02 69	02 6A	02 6B	02 6C	02 6D	02 6E	02 6F
260	261	262	263	264	265	266	267	268	269	26A	26B	26C	26D	26E	26F
02 70	02 71	02 72	02 73	02 74	02 75	02 76	02 77	02 78	02 79	02 7A	02 7B	02 7C	02 7D	02 7E	02 7F
270	271	272	273	274	275	276	277	278	279	27A	27B	27C	27D	27E	27F
02 80	02 81	02 82	02 83	02 84	02 85	02 86	02 87	02 88	02 89	02 8A	02 8B	02 8C	02 8D	02 8E	02 8F
280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F
02 90	02 91	02 92	02 93	02 94	02 95	02 96	02 97	02 98	02 99	02 9A	02 9B	02 9C	02 9D	02 9E	02 9F
290	291	292	293	294	295	296	297	298	299	29A	29B	29C	29D	29E	29F
02 A0	02 A1	02 A2	02 A3	02 A4	02 A5	02 A6	02 A7	02 A8	02 A9	02 AA	02 AB	02 AC	02 AD	02 AE	02 AF
2A0	2A1	2A2	2A3	2A4	2A5	2A6	2A7	2A8	2A9	2AA	2AB	2AC	2AD	2AE	2AF
02 B0	02 B1	02 B2	02 B3	02 B4	02 B5	02 B6	02 B7	02 B8	02 B9	02 BA	02 BB	02 BC	02 BD	02 BE	02 BF
2B0	2B1	2B2	2B3	2B4	2B5	2B6	2B7	2B8	2B9	2BA	2BB	2BC	2BD	2BE	2BF
02 C0	02 C1	02 C2	02 C3	02 C4	02 C5	02 C6	02 C7	02 C8	02 C9	02 CA	02 CB	02 CC	02 CD	02 CE	02 CF
2C0	2C1	2C2	2C3	2C4	2C5	2C6	2C7	2C8	2C9	2CA	2CB	2CC	2CD	2CE	2CF
02 D0	02 D1	02 D2	02 D3	02 D4	02 D5	02 D6	02 D7	02 D8	02 D9	02 DA	02 DB	02 DC	02 DD	02 DE	02 DF
2D0	2D1	2D2	2D3	2D4	2D5	2D6	2D7	2D8	2D9	2DA	2DB	2DC	2DD	2DE	2DF
02 E0	02 E1	02 E2	02 E3	02 E4	02 E5	02 E6	02 E7	02 E8	02 E9	02 EA	02 EB	02 EC	02 ED	02 EE	02 EF
2E0	2E1	2E2	2E3	2E4	2E5	2E6	2E7	2E8	2E9	2EA	2EB	2EC	2ED	2EE	2EF
02 F0	02 F1	02 F2	02 F3	02 F4	02 F5	02 F6	02 F7	02 F8	02 F9	02 FA	02 FB	02 FC	02 FD	02 FE	02 FF
2F0	2F1	2F2	2F3	2F4	2F5	2F6	2F7	2F8	2F9	2FA	2FB	2FC	2FD	2FE	2FF

0300	0301	0302	0303	0304	0305	0306	0307	0308	0309	030A	030B	030C	030D	030E	030F
0310	0311	0312	0313	0314	0315	0316	0317	0318	0319	031A	031B	031C	031D	031E	031F
0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	032A	032B	032C	032D	032E	032F
0330	0331	0332	0333	0334	0335	0336	0337	0338	0339	033A	033B	033C	033D	033E	033F
0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	034A	034B	034C	034D	034E	034F
0350	0351	0352	0353	0354	0355	0356	0357	0358	0359	035A	035B	035C	035D	035E	035F
0360	0361	0362	0363	0364	0365	0366	0367	0368	0369	036A	036B	036C	036D	036E	036F
0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	037A	037B	037C	037D	037E	037F
0380	0381	0382	0383	0384	0385	0386	0387	0388	0389	038A	038B	038C	038D	038E	038F
0390	0391	0392	0393	0394	0395	0396	0397	0398	0399	039A	039B	039C	039D	039E	039F
03A0	03A1	03A2	03A3	03A4	03A5	03A6	03A7	03A8	03A9	03AA	03AB	03AC	03AD	03AE	03AF
03B0	03B1	03B2	03B3	03B4	03B5	03B6	03B7	03B8	03B9	03BA	03BB	03BC	03BD	03BE	03BF
03C0	03C1	03C2	03C3	03C4	03C5	03C6	03C7	03C8	03C9	03CA	03CB	03CC	03CD	03CE	03CF
03D0	03D1	03D2	03D3	03D4	03D5	03D6	03D7	03D8	03D9	03DA	03DB	03DC	03DD	03DE	03DF
03E0	03E1	03E2	03E3	03E4	03E5	03E6	03E7	03E8	03E9	03EA	03EB	03EC	03ED	03EE	03EF
03F0	03F1	03F2	03F3	03F4	03F5	03F6	03F7	03F8	03F9	03FA	03FB	03FC	03FD	03FE	03FF

■ FONT DEVELOPMENT AND DATA RELEASE

The MB90099 features the font ROM in which all 1024 characters are user-definable. For font data development, use the OSDC pattern editor Ped/Win. Ped/Win is an OSDC proprietary pattern editor for use on personal computers operating Windows95/98/NT4.0 (Japanese language) environments.

The font development and data release flow is illustrated below.



(1) Font data release

Font data is released in project files only. Pattern files should not be released. A portion of the pattern file data will be used for data matching in order to verify registration of release data by FUJITSU. For this reason, users are requested to write a portion of the pattern data content in mask data specifications.

Note : Pattern data output should not be generated until after the completion of font creation and project creation. Also, the project file should not be updated after pattern file generation is completed. If the project contents are updated after pattern file generation, pattern files should be generated again.

(2) Project files

After font data and other supplementary data is created, it is stored in a project file. Normally one project file is created for each model.

- **Project file names**

Project file names should be in the format "MB90099-XXX" where "XXX" is a ROM number assigned by FUJITSU. Users should contact their FUJITSU sales representative. If no ROM number has been assigned, any number preceded by an alphabetic character may be used. Project files which are developed solely for test purposes and not intended for font release may be assigned any file name.

- **Comments related to new project files**

Comment lines in the form of any desired character strings may be added at the time a project file is created. Comments will be printed when the font is printed, and can be modified as needed whenever that Ped/Win is operating.

(3) Pattern files

Font data may be placed in pattern files. Because pattern data is saved in the project file, normally it is only necessary to create a pattern file at the time of font release for the purpose of extracting verification data (writing to mask data specifications) . Pattern files should not be released.

- **Pattern file loading**

Pattern files can be loaded for some OSD models other than the MB90099.

- **Pattern file output generation**

Do not create more than one pattern file for the same project. This may cause errors . In such cases, the project name should be altered to create another project.

- **Extracting verification data**

Three data points, the first and last addresses and one other random address, should be extracted from pattern file data and written into the mask data specifications. The random address should not include the data values "00" or "FF."

Note : Ped/Win display functions are based on OSD specifications, however some display specifications may not be identical to actual OSD specifications. Users should consult specification documents for details.

(Data comparison)

After data release, once ROM mask processing is completed FUJITSU will extract the ROM data used in this process. Users should verify that the extracted data is identical to the pattern file data that was submitted, and return a written statement of data comparison indicating whether that data is identical or not . If the data is not identical, contact FUJITSU's sales representative immediately. Data errors may cause errors in ES production.

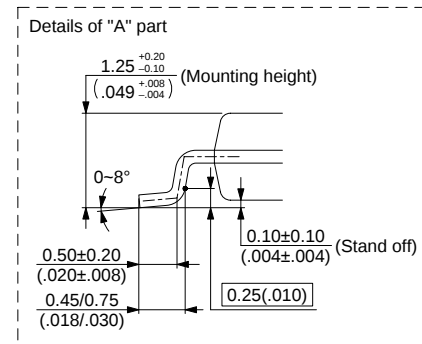
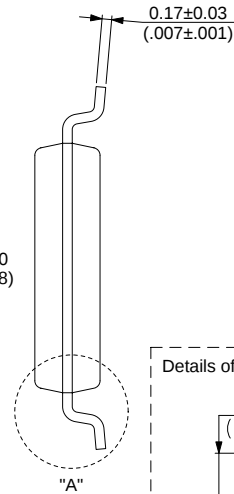
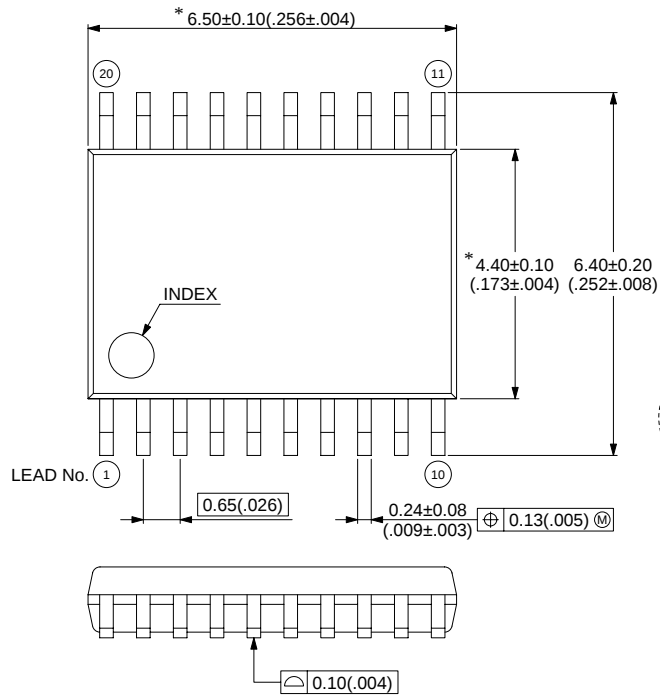
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB90099PFV	20-pin Plastic SSOP (FPT-20P-M03)	
MB90099LGA	20-pin Plastic FLGA (LGA-20P-M01)	

■ PACKAGE DIMENSION

20-pin Plastic SSOP
(FPT-20P-M03)

* : These dimensions do not include resin protrusion.



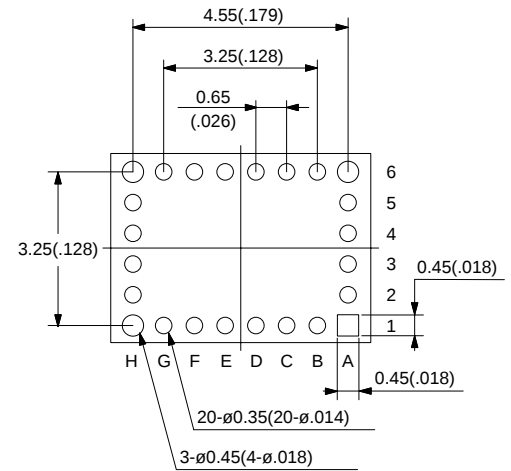
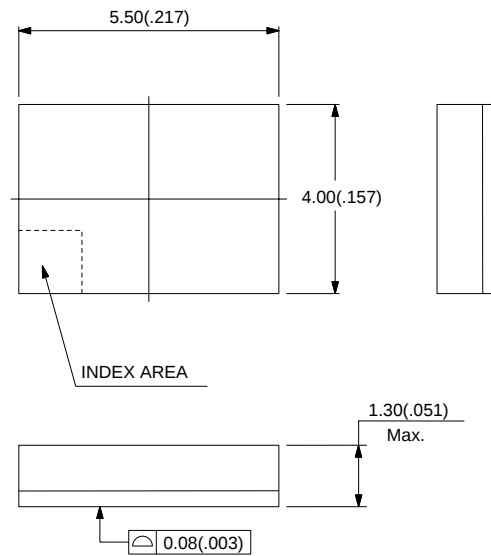
© 1999 FUJITSU LIMITED F20012S-3C-5

Dimensions in mm (inches)

(Continued)

(Continued)

20-pin plastic FLGA (LGA-20P-M02)



© 2001 FUJITSU LIMITED L20001S-c-1-1

Dimensions in mm (inches)

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.