Integrated
Circuit
Systems, Inc.

ICS9159C-14

Frequency Generator and Integrated Buffer for PENTIUM™

General Description

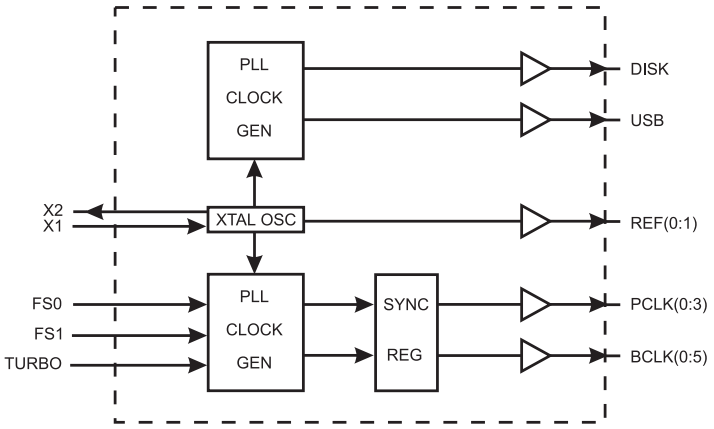
The **ICS9159C-14** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiply-ing factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. It has a TURBO pin that can speed up the 60 and 66.6 MHz clocks by 2.5%.

High drive BCLK outputs provide typically greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide typically better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle.

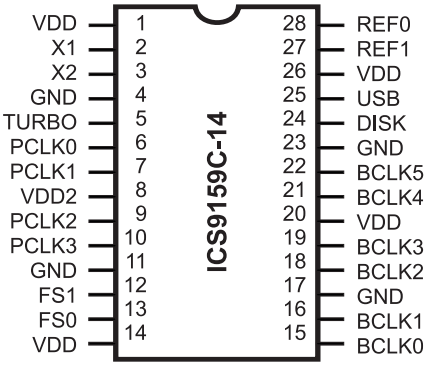
Features

- Generates up to four processor and six bus clocks, plus disk, USB and reference clocks
- Synchronous clocks skew matched to 250ps window on PCLKs and 500ps window on BCLKs
- TURBO input pin that can speed up the 60 and 66.6 MHz PCLKs by 2.5%.
- 2.5V or 3.3V output: PCLK (0:3)
- 3.0V - 5.5V supply range
- 28-pin SOIC package

Block Diagram



Pin Cnfiguration



28-Pin SOIC

Functionality

TURBO	FS1	FS0	X1, REF (MHz)	PCLK (MHz)
1	0	0	14.318	50
1	0	1	14.318	66.8
1	1	0	14.318	60
1	1	1	14.318	55
0	0	0	14.318	83.3
0	0	1	14.318	68.4
0	1	0	14.318	61.6
0	1	1	14.318	75

PCLK(0:3)	BCLK(0:5)	USB	DISK
VCO/2	PCLK/2	48 MHz	24 MHz

All frequencies in MHz, assuming 14.318 MHz input.

Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of Motorola Corporation.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 26	V_{DD}	PWR	Power for logic and fixed frequency output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4, 11, 17, 23	V_{SS}	PWR	Ground
5	TURBO	IN	Speeds up the 60 and 66.6 MHz by 2.5% (see functionality table). It has an internal pull-up resistor.
6, 7, 9, 10	PCLK(0:3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
8	V_{DD2}	PWR	Power for PCLK output buffers only. This V_{DD} supply can be reduced to 2.5V for PCLK (0:3) outputs.
13, 12	FS(0:1)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.
14, 20	V_{DD}	PWR	Power for BCLK output buffers.
15, 16, 18 19, 21, 22	BCLK(0:5)	OUT	Busclock outputs are fixed at one half the PCLK frequency.
24	DISK	OUT	The DISK controller clock is fixed at 24 MHz (with 14.318 MHZ input)
25	USB	OUT	The USB clock is fixed at 48 MHz (with 14.318 MHz input).
28, 27	REF(0:1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-28.0	-10.5	-	mA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for PCLKs & BCLKs	30.0	47.0	-	Ma
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for PCLKs & BCLKs	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for PCLKs & BCLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA; for PCLKs & BCLKs	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.5 MHz; all outputs unloaded	-	55	110	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.1 – 3.7 V, T_A = 0 – 70° C

AC Characteristics						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @ V_{OUT}=1.4V	48	50	58	%
Jitter, One Sigma[1]	T_{j1s1}	PCLK & BCLK; Load=20pF.	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK; Load=20pF.	-250	-	250	ps
Jitter, One Sigma[1]	T_{j1s2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 66.5 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0V

V_{DD} = 4.5 – 5.5 V, T_A = 0 – 70° C

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.4	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-45	-15	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for PCLKs & BCLKs	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for PCLKs & BCLKs	-	-152	-90.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	30.0	50.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-110.0	-65.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=20mA; for PCLKs & BCLKs	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-70mA; for PCLKs & BCLKs	2.4	4.0	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for fixed CLKs	-	0.2	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-50mA; for fixed CLKs	2.4	4.7	-	V
Supply Current	I_{DD}	@66.5 MHz; all outputs unloaded	-	80.0	160.0	mA

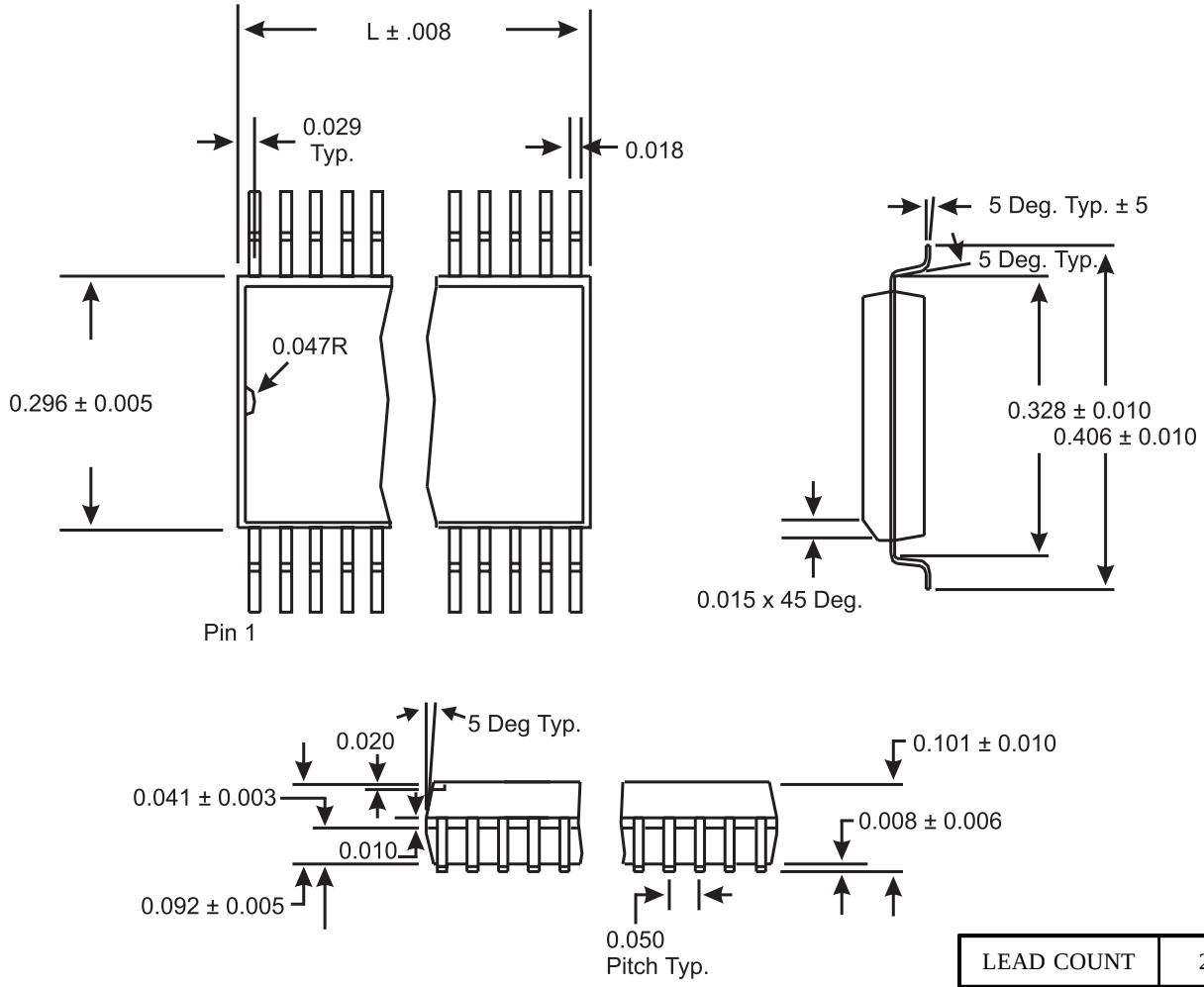
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.5V

V_{DD} = 4.5 – 5.5 V, T_A = 0 – 70° C

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.55	0.95	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.52	0.90	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.2	2.1	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.1	2.0	ns
Duty Cycle[1]	D_{t1}	20pF load @ V_{OUT}=1.4V	50	57	60	%
Duty Cycle[1]	D_{t2}	20pF load @ V_{OUT}=50%	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	PCLK & BCLK; Load=20pF, Rs=33Ω	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK; Load=20pF, Rs=33Ω	-250	-	250	ps
Jitter, One Sigma[1]	T_{j1s2}	REF CLKs; Load=20pF Rs=33Ω	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	REF CLKs; Load=20pF Rs=33Ω	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal OscillatorCapacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 66.5 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK & BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



LEAD COUNT	28L
DIMENSIONL	0.704

SOIC Package

Ordering Information

ICS9159CM-14

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device