

TC74VHC299F, TC74VHC299FW, TC74VHC299FT**8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR**

The TC74VHC299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

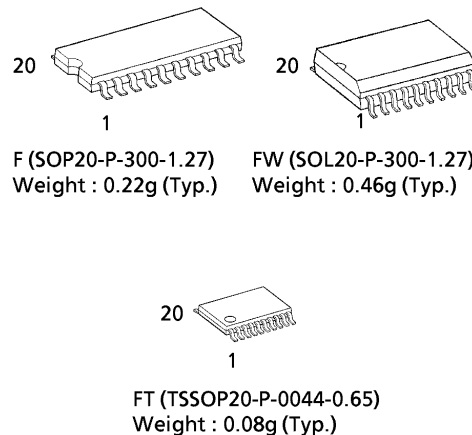
When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

All inputs are equipped with protection circuits against static discharge.

FEATURES :

- High Speed..... $f_{MAX} = 160\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\%V_{CC} (\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range
..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise $V_{OLP} = 1.4\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS299

(Note) The JEDEC SOP (FW) is not available in Japan.

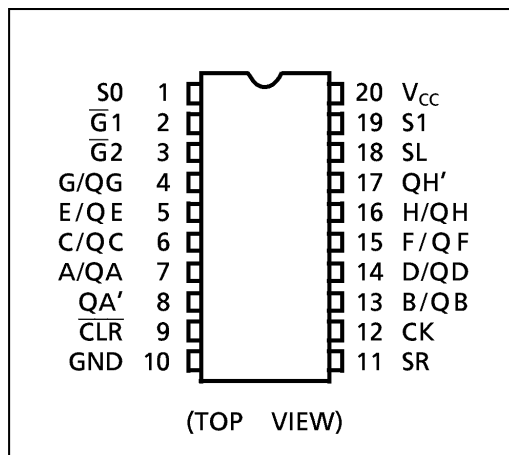
**APPLICATION NOTE**

- 1) Do not apply a signal to A / QA~H / QH bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) A / QA~H / QH bus terminals must have their input levels fixed by means of pull up or pull down resistors.
- 3) A parasitic diode is formed between A / QA~H / QH bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

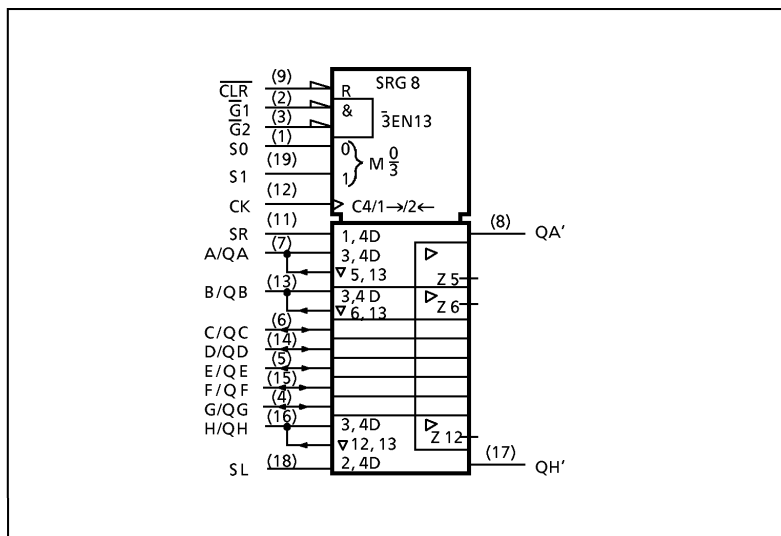
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PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

MODE	INPUTS								INPUTS/ OUTPUTS		OUTPUTS	
	$\overline{\text{CLR}}$	FUNCTION SELECT		OUTPUT CONTROL		CK	SERIAL					
		S1	S0	$\overline{\text{G1}}^*$	$\overline{\text{G2}}^*$		SL	SR	A/QA	H/QH	QA'	QH'
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT	H	L	H	L	L	$\downarrow$	X	H	H	QGn	H	QGn
RIGHT	H	L	H	L	L	$\downarrow$	X	L	L	QGn	L	QGn
SHIFT	H	H	L	L	L	$\downarrow$	H	X	QBn	H	QBn	H
LEFT	H	H	L	L	L	$\downarrow$	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	$\downarrow$	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state ; however sequential or clearing of the register is not affected.

Z : High impedance

Qn0 : The level of Qn before the indicated steady-state input conditions were established.

Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.

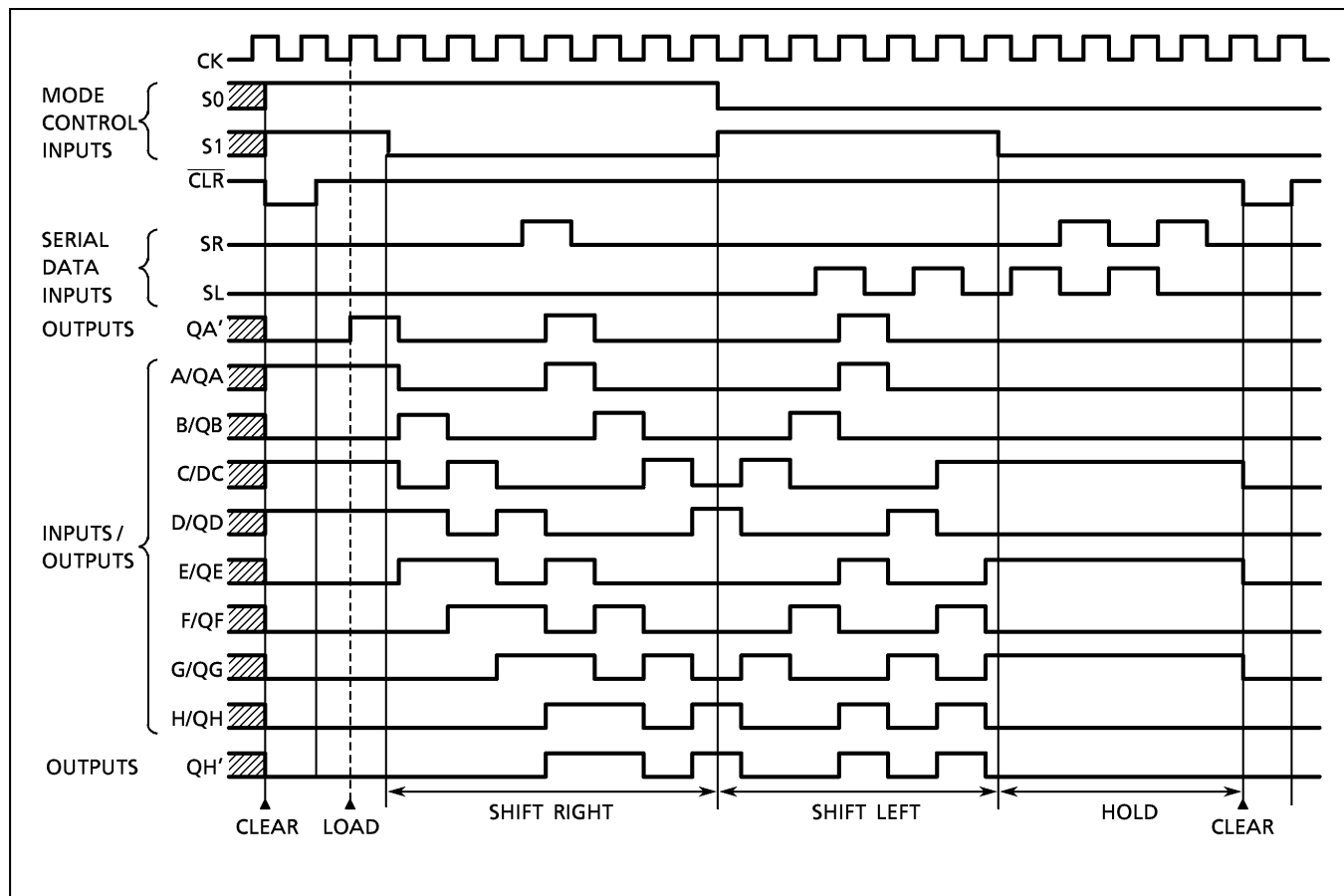
a, h : The level of the steady-state inputs A, H, respectively.

X : Don't Care.

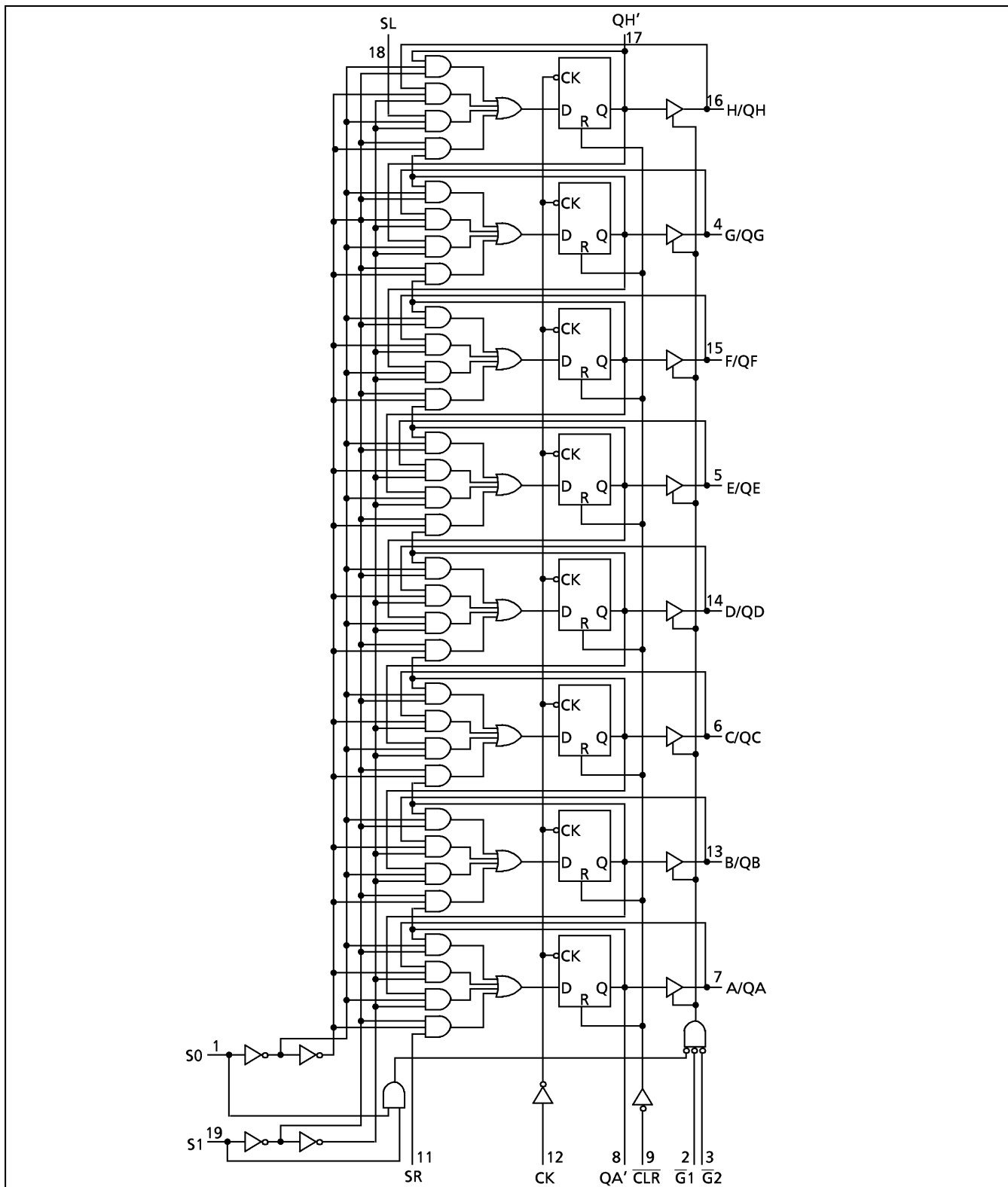
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TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC BUS I / O Voltage (A/QA~H/QH)	$V_{IN/OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage (QA'~QH')	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 80	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
DC BUS I / O Voltage (A/QA~H/QH)	$V_{IN/OUT}$	0~ V_{CC}	V
DC Output Voltage (QA'~QH')	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	0~100 ($V_{CC} = 3.3 \pm 0.3\text{V}$) 0~20 ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITON		V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0 3.0~5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V
Low-Level Input Voltage	V_{IL}			2.0 3.0~5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			$I_{OH} = -4\text{mA}$ $I_{OH} = -8\text{mA}$	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$I_{OL} = 4\text{mA}$ $I_{OL} = 8\text{mA}$	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } \text{GND}$		5.5	—	—	± 0.25	—	± 2.50	μA
Input Leakage Current	I_{IN}	$V_{IN} = 5.5\text{V or GND}$		0~5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$		5.5	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK—QA' , QH')	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	12.2	17.2	1.0	19.8	ns
				50	—	14.7	20.7	1.0	23.3	
			5.0 ± 0.5	15	—	8.5	10.8	1.0	12.0	
				50	—	10.0	12.8	1.0	14.0	
Propagation Delay Time (CLR—QA' , QH')	t _{pHL}		3.3 ± 0.3	15	—	13.0	19.0	1.0	22.0	
				50	—	15.5	22.5	1.0	25.5	
			5.0 ± 0.5	15	—	9.1	11.2	1.0	13.5	
				50	—	10.8	13.2	1.0	15.5	
Propagation Delay Time (CK—QA~QH)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	10.3	14.3	1.0	16.6	
				50	—	12.8	17.8	1.0	20.1	
			5.0 ± 0.5	15	—	7.3	9.1	1.0	10.4	
				50	—	8.8	11.1	1.0	12.4	
Propagation Delay Time (CLR—QA~QH)	t _{pHL}		3.3 ± 0.3	15	—	10.8	17.0	1.0	19.5	
				50	—	13.3	20.5	1.0	23.0	
			5.0 ± 0.5	15	—	7.7	10.5	1.0	12.0	
				50	—	9.2	12.5	1.0	14.0	
Output Enable Time	t _{pZL} t _{pZH}	R _L = 1kΩ	3.3 ± 0.3	15	—	13.3	16.5	1.0	19.2	
				50	—	14.8	19.0	1.0	21.7	
			5.0 ± 0.5	15	—	8.9	9.7	1.0	11.3	
				50	—	10.4	11.2	1.0	12.6	
Output Disable Time	t _{pLZ} t _{pHZ}	R _L = 1kΩ	3.3 ± 0.3	50	—	18.0	21.3	1.0	24.3	
			5.0 ± 0.5	50	—	11.8	13.2	1.0	15.0	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	15	100	65	—	55	—	MHz
				50	90	55	—	50	—	
			5.0 ± 0.5	15	160	125	—	110	—	
				50	150	115	—	100	—	
Input Capacitance	C _{IN}				—	4	10	—	—	pF
BUS I/O Capacitance (A/QA~H/QH)	C _{OUT}				—	8	—	—	—	
Power Dissipation Capacitance	C _{PD}	(Note 1)			—	110	—	—	—	

Note (1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

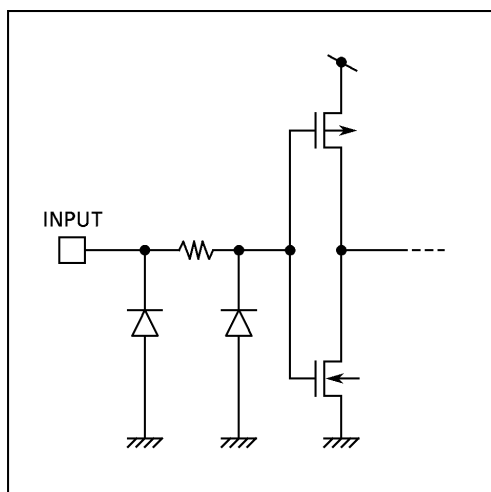
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3	—	7.0	8.0	ns
			5.0 ± 0.5	—	7.0	8.0	
Minimum Pulse Width ($\overline{\text{CLR}}$)	$t_{W(L)}$		3.3 ± 0.3	—	6.0	7.0	
			5.0 ± 0.5	—	6.0	7.0	
Minimum Set-Up Time (SL, SR)	t_S		3.3 ± 0.3	—	8.5	10.0	
			5.0 ± 0.5	—	5.0	5.0	
Minimum Set-Up Time (A~H)	t_S		3.3 ± 0.3	—	8.0	9.0	
			5.0 ± 0.5	—	4.0	4.0	
Minimum Set-Up Time (S0, S1)	t_S		3.3 ± 0.3	—	14.5	17.0	
			5.0 ± 0.5	—	7.0	8.0	
Minimum Hold Time (SL, SR)	t_h		3.3 ± 0.3	—	1.0	1.0	
			5.0 ± 0.5	—	1.0	1.0	
Minimum Hold Time (A~H)	t_h		3.3 ± 0.3	—	0.5	0.5	
			5.0 ± 0.5	—	1.5	1.5	
Minimum Hold Time (S0, S1)	t_h		3.3 ± 0.3	—	0	0	
			5.0 ± 0.5	—	0.5	0.5	
Minimum Removal Time ($\overline{\text{CLR}}$)	t_{rem}		3.3 ± 0.3	—	5.0	6.0	
			5.0 ± 0.5	—	4.0	4.0	

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

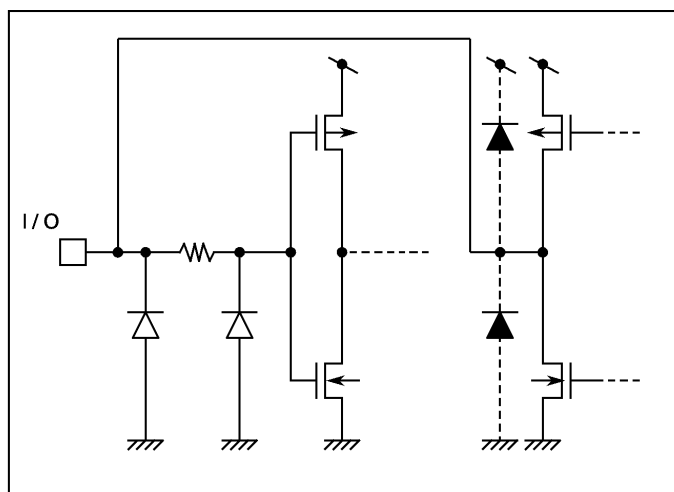
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		UNIT
				TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50\text{pF}$	5.0	0.9 (1.0)	1.2 (1.4)	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50\text{pF}$	5.0	-0.9 (-1.0)	-1.2 (-1.4)	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50\text{pF}$	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50\text{pF}$	5.0	—	1.5	V

(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT

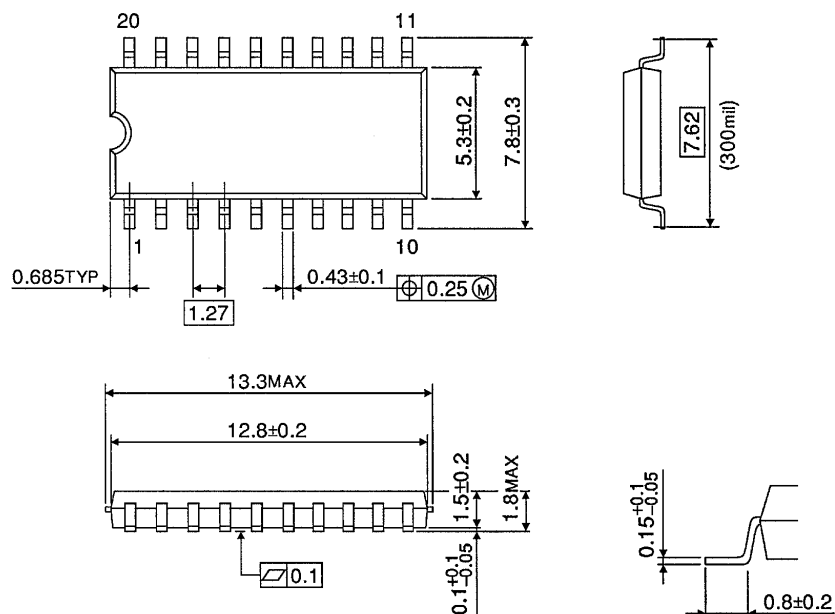


A/QA~H/QH BUS TERMINAL EQUIVALENT CIRCUIT



SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

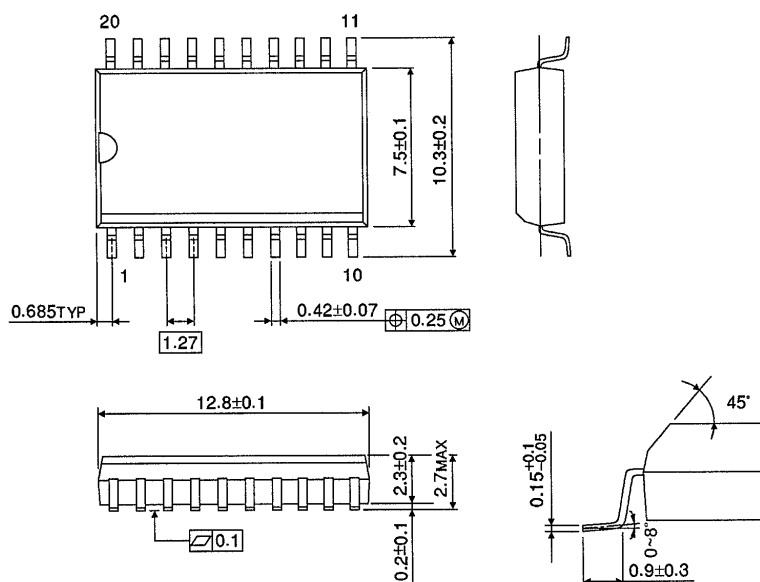


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm

