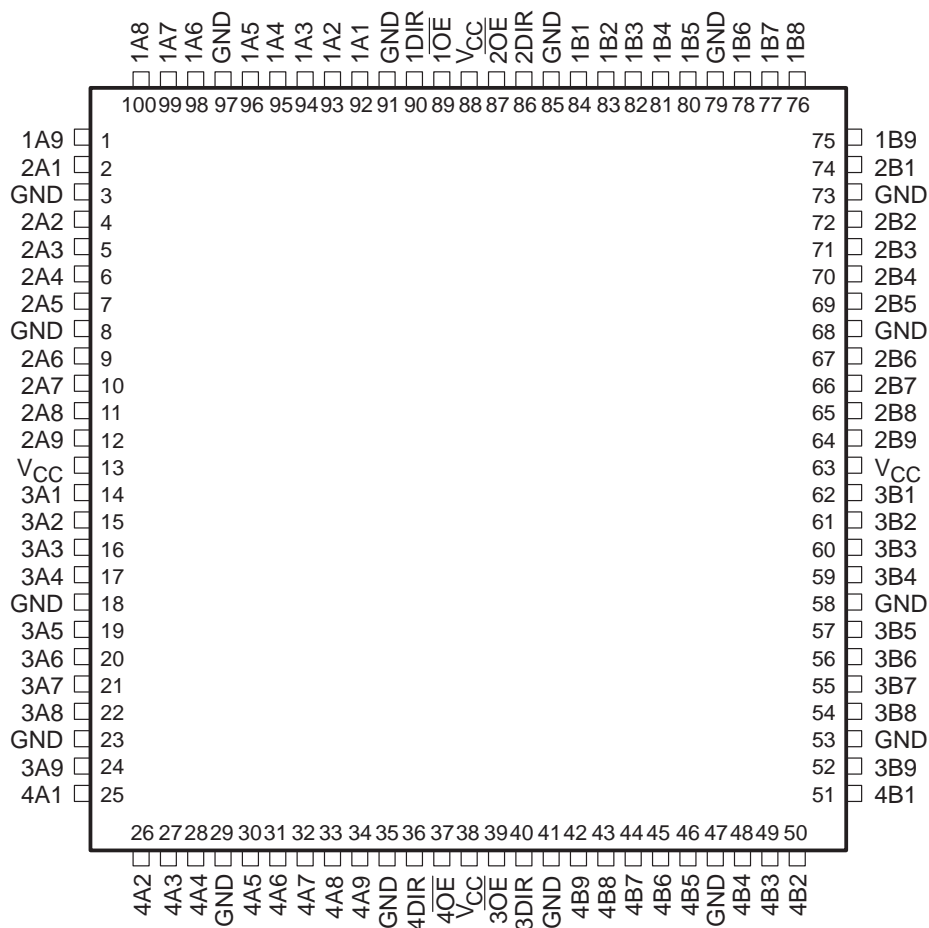


# SN54ABTH32245, SN74ABTH32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Released as DSCC SMD 5962-9557701NXD
- PZ Package Qualified for Military Per MIL-PRF-38535 (QML)
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With  $14 \times 14\text{-mm}$  Body Using  $0.5\text{-mm}$  Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

ABTH32245 . . . PZ PACKAGE  
(TOP VIEW)



† The HS package is not production released.



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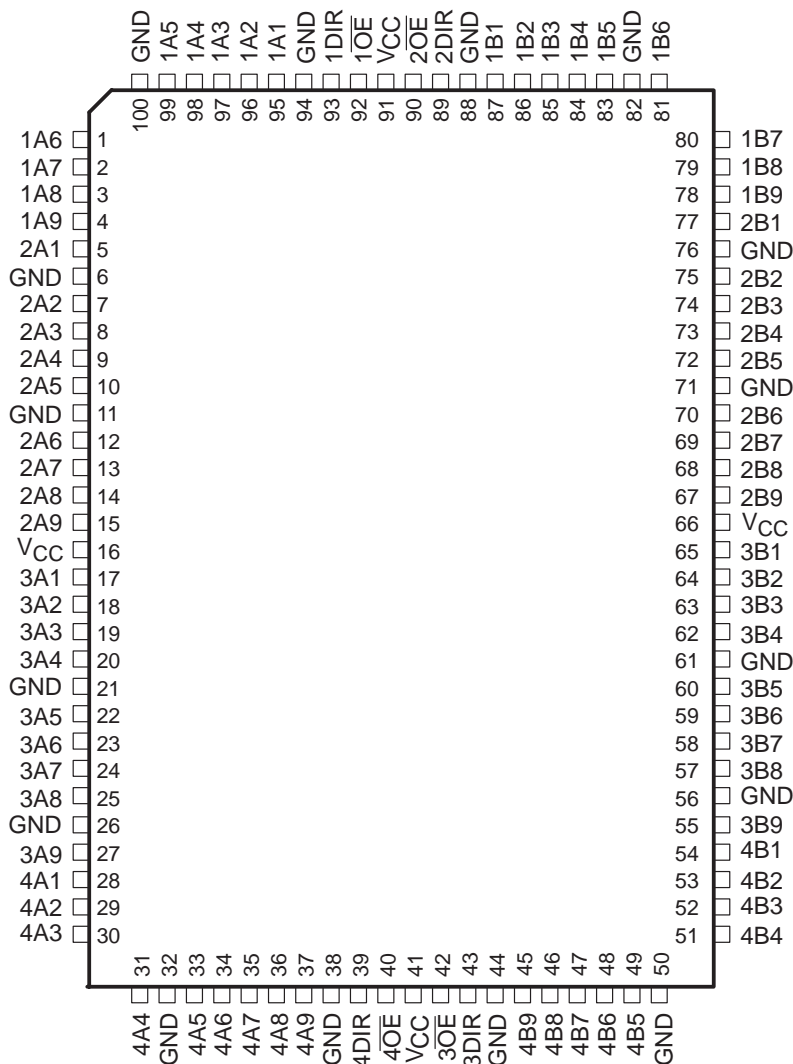
# SN54ABTH32245, SN74ABTH32245

## 36-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

SN54ABTH32245 . . . HS PACKAGE†  
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

## description

The 'ABTH32245 are 36-bit (quad 9-bit) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as four 9-bit transceivers, two 18-bit transceivers, or one 36-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) inputs. The output-enable ( $\overline{OE}$ ) inputs can be used to disable the device so that the buses are effectively isolated.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.



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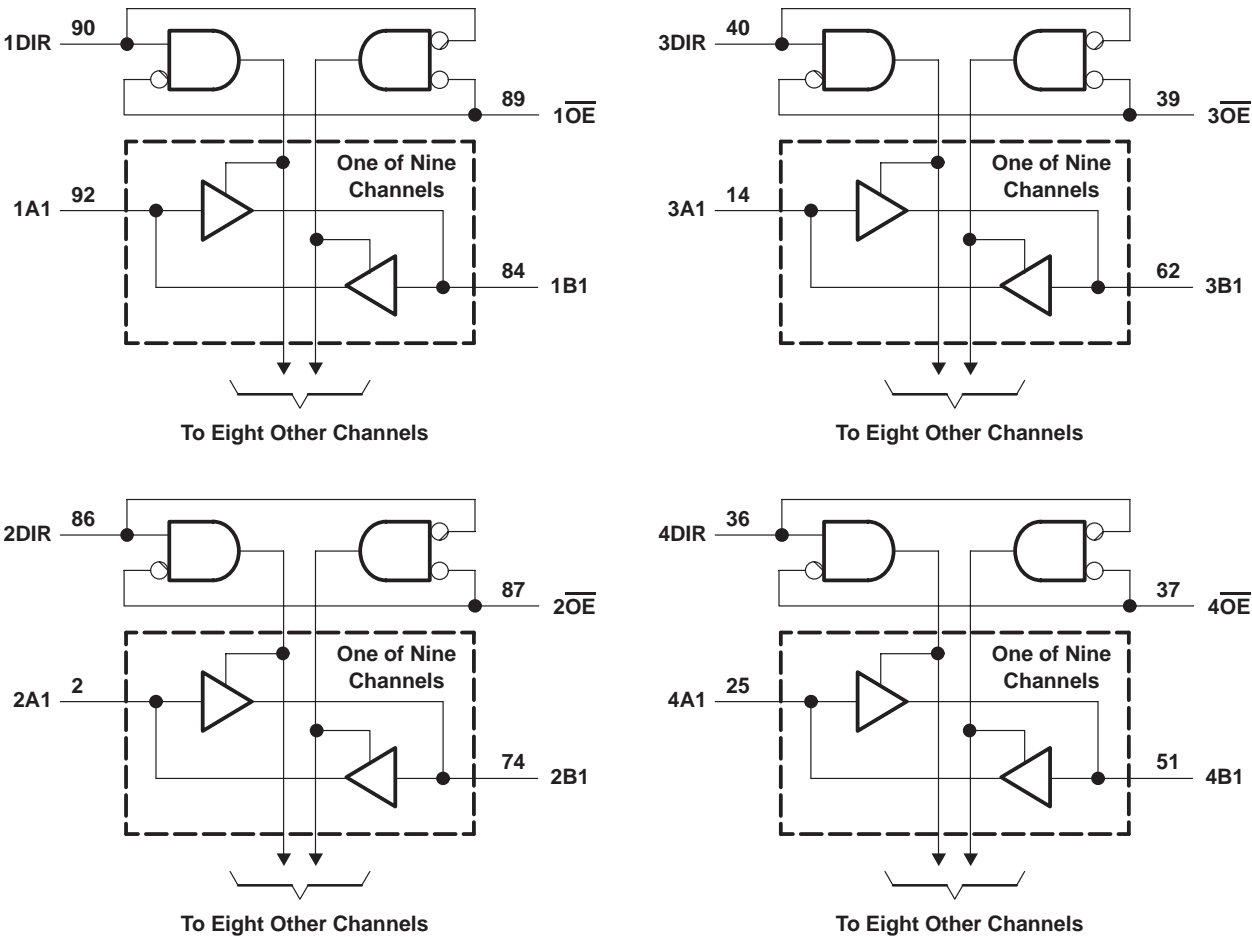
**description (continued)**

The SN54ABTH32245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
 The SN74ABTH32245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
 (each 9-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**logic diagram (positive logic)**



Pin numbers shown are for the PZ package.

# SN54ABTH32245, SN74ABTH32245

## 36-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABTH32245	96 mA
SN74ABTH32245	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): PZ package	50°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

#### recommended operating conditions (see Note 3)

		SN54ABTH32245		SN74ABTH32245		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



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SN54ABTH32245, SN74ABTH32245  
36-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32245			SN74ABTH32245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.5			2.5			V
		$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3			3			
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -24\text{ mA}$	2						
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -32\text{ mA}$				2			
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$			0.55			0.55	V
		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 64\text{ mA}$						0.55	
$V_{hys}$			100			100			mV
$I_I$	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$						$\pm 1$	$\mu\text{A}$
	A or B ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$						$\pm 20$	
	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$				$\mu\text{A}$
	A or B ports	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 20$				
$I_I(\text{hold})$	A or B ports	$V_{CC} = 4.5\text{ V}$ , $V_I = 0.8\text{ V}$	100			100			$\mu\text{A}$
		$V_{CC} = 4.5\text{ V}$ , $V_I = 2\text{ V}$	-100			-100			
$I_{OZPU}^\ddagger$		$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$			$\pm 50$	$\mu\text{A}$
$I_{OZPD}^\ddagger$		$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$			$\pm 50$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$						$\pm 100$	$\mu\text{A}$
$I_{CEX}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$ , Outputs high			50			50	$\mu\text{A}$
$I_O^\S$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-100	-180	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$			3			3	mA
					20			20	
					2			2	
$\Delta I_{CC}^\P$		$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1			1	mA
$C_i$	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5			3.5	pF
$C_{io}$	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$			9.5			9.5	pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}^\#$			SN54ABTH32245		SN74ABTH32245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.7	3.2	4.4	1	5.3	1.7	5	ns
$t_{PHL}$			1.7	3.3	4.6	1	5.3	1.7	5.2	
$t_{PZH}$	$\overline{OE}$	B or A	1.6	4.2	6.1	1	7.6	1.6	7.3	ns
$t_{PZL}$			2.7	5.2	7	1.5	8.2	2.7	8.1	
$t_{PHZ}$	$\overline{OE}$	B or A	1.3	3.9	6.1	0.8	6.7	1.3	6.5	ns
$t_{PLZ}$			2	4.4	6.6	1	7.2	2	6.9	

# These limits apply only to the SN74ABTH32245

# SN54ABTH32245, SN74ABTH32245

## 36-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



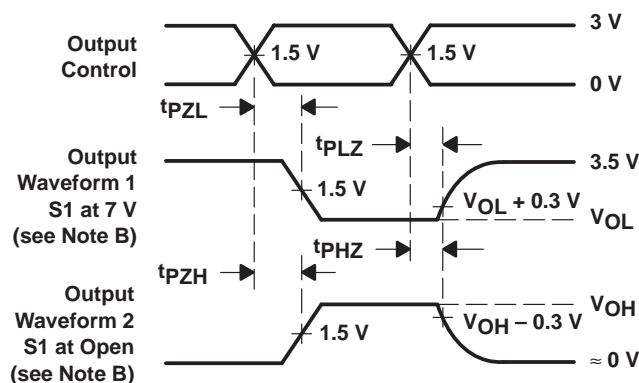
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9557701NXD	ACTIVE	LQFP	PZ	100	90	TBD	Call TI	Level-2-220C-1 YR
SN74ABTH32245PZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN74ABTH32245PZG4	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

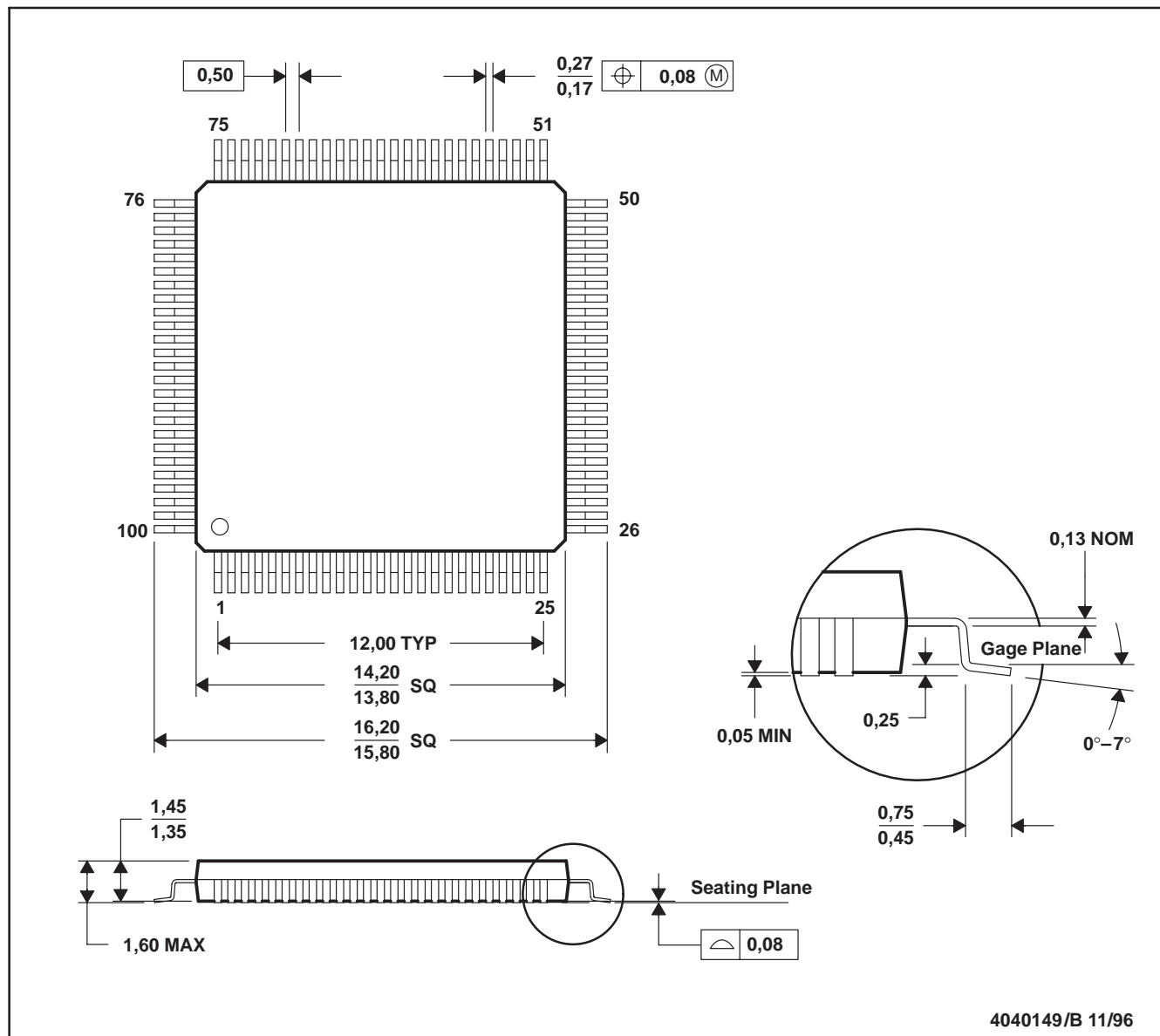
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## PZ (S-PQFP-G100)

## PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026



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