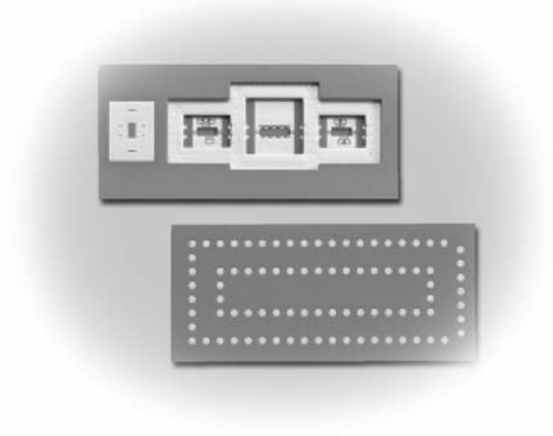
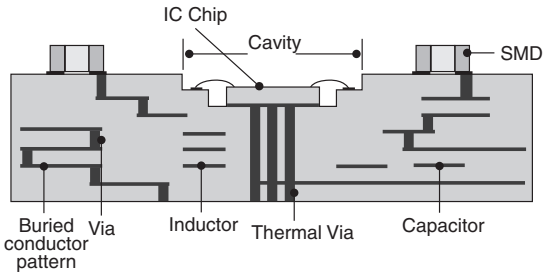
EU RoHS COMPLIANT



features

- The high-density wiring by the fine line and pattern is available
- Miniaturization is possible by burying L, C and Strip-line
- By the uses of low dielectric-loss ceramics and low loss conductors, the substrates excel in the high frequency characteristic
- As the thermal expansion coefficient is close to silicon's, the substrates are suitable for the bare chip mounting
- By preparing the thermal vias under bare chips, the substrates are excellent in the heat dissipation
- The substrates are outstanding in heat resistance and humidity resistance due to the ceramics used

construction



ordering information

New Part #

KLC	AB1
Type	KOA Ref. Number

definition

With the high functioning and the advance in down-sizing of electronic equipment, wiring substrates are also required to be highly functioned.

One of the technologies to respond to the high functioning of the substrates is LTCC (Low Temperature Co-fired Ceramics), which is the ceramic multilayer technology that enables the alumina to be fired at a "low temperature" of 900°C or lower by adding glass materials to the alumina while it is fired by a "high temperature" of about 1500°C.

It is the LTCC's important characteristic that low melting point materials like Ag, etc. can be used for the buried conductors for the low temperature firing.

environmental applications

Characteristics of Substrate Material

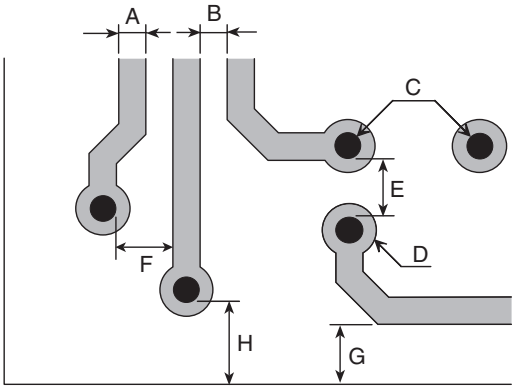
Parameter	Characteristics
Bending Strength	250
Thermal Expansion Coefficient	5.5
Thermal Conductivity	3
Insulation Resistance	$>10^{13}$
Dielectric Constant	7
Dielectric Loss	<0.003
Resistivity of Buried Conductor	Ag 2.5
Density	2.8
Surface Roughness Ra	<0.4
Withstanding Voltage	>15
Layer Thickness	80, 100, 125 Standard
Substrate Flatness	<0.03

environmental applications (continued)

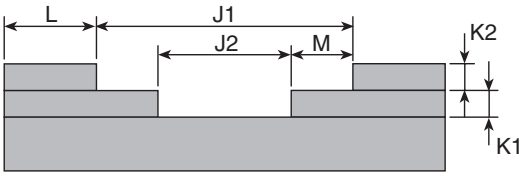
Characteristics of Substrate Material

Symbol	Parameter	Design Value
A	Line Width	0.06mm Min.
B	Line to Line Spacing	0.06mm Min.
C	Via Diameter	0.1mm, 0.15mm, 0.2mm
D	Via Pad Diameter	Via diameter +0.05mm Min.
E	Via to Via Spacing	0.2mm Min.
F	Via to Line Spacing	0.15mm Min.
G	Part Edge to Conductor Spacing	0.2mm Min.
H	Part Edge to Via Spacing	0.3mm Min.
J1, J2	Cavity Width	0.6mm Min.
K1, K2	Cavity Depth	0.1mm Min.
L	Wall Thickness of Cavity	0.5mm Min.
M	Shelf Width in the Cavity	0.5mm Min.

Surface layer - Inner layer



Cavity



modules