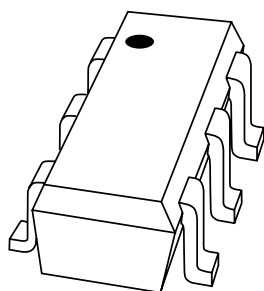


DATA SHEET



PUMD10

**NPN/PNP resistor-equipped
transistors**

Product specification
Supersedes data of 1998 Dec 04

1999 May 20

NPN/PNP resistor-equipped transistors

PUMD10

FEATURES

- Transistors with different polarity and built-in bias resistors R1 and R2 (typ. 2.2 kΩ and 47 kΩ respectively)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in portable equipment
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

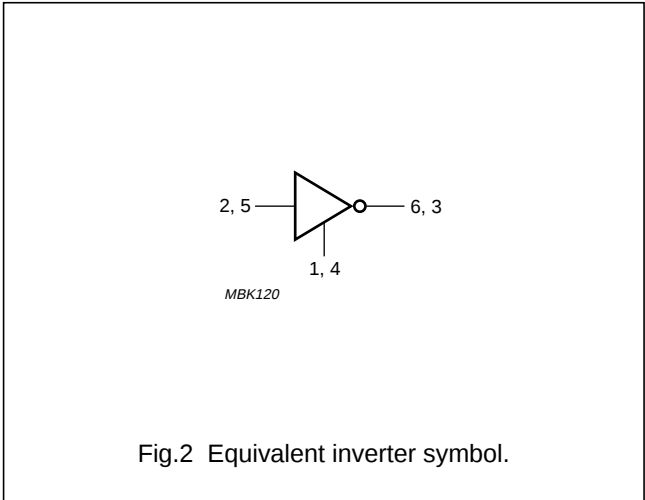
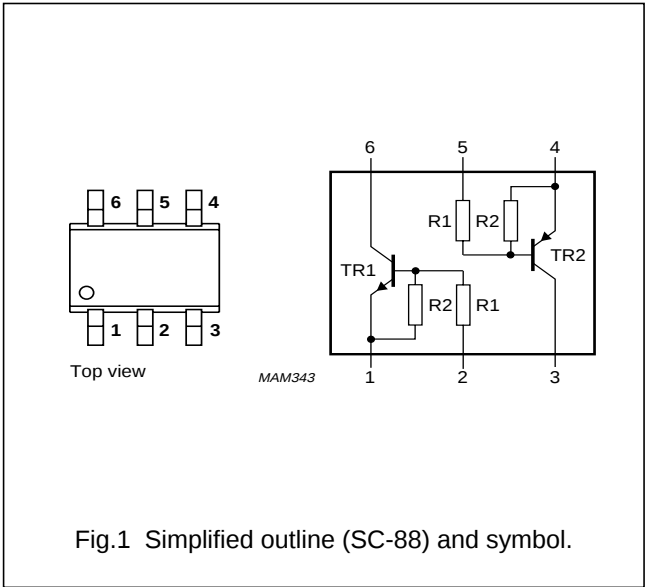
NPN/PNP resistor-equipped transistors in an SC-88 (SOT363) plastic package.

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

MARKING

TYPE NUMBER	MARKING CODE
PUMD10	Dt0



NPN/PNP resistor-equipped transistors

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage				
	positive		–	+12	V
	negative		–	–5	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Refer to SC-88 standard mounting conditions.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	416	K/W

Note

1. Refer to SC-88 standard mounting conditions.

NPN/PNP resistor-equipped transistors

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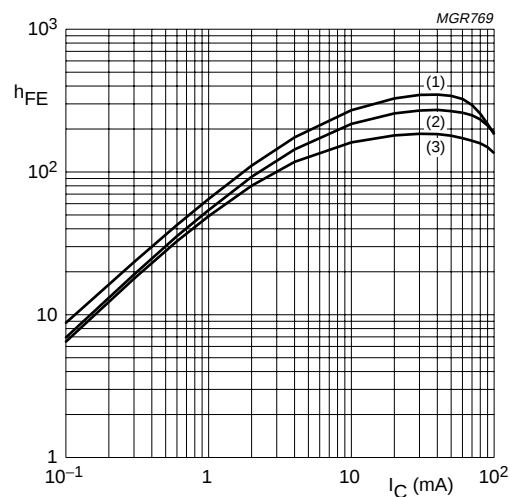
CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector cut-off current	$I_C = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
I_{CEO}	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	μA
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	–	–	50	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	180	μA
h_{FE}	DC current gain	$I_C = 10\text{ mA}; V_{CE} = 5\text{ V}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	–	–	100	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	0.6	0.5	V
$V_{i(on)}$	input-on voltage	$I_C = 5\text{ mA}; V_{CE} = 0.3\text{ V}$	1.1	0.75	–	V
$R1$	input resistor		1.54	2.2	2.86	k Ω
$\frac{R2}{R1}$	resistor ratio		17	21	26	
C_c	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	–	2.5	pF
	TR1 (NPN) TR2 (PNP)				3	pF

NPN/PNP resistor-equipped transistors

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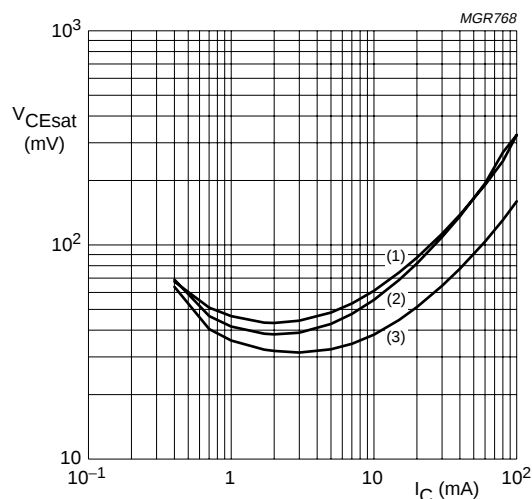
TR1 (NPN); $V_{CE} = 5$ V.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.3 DC current gain as a function of collector current; typical values.



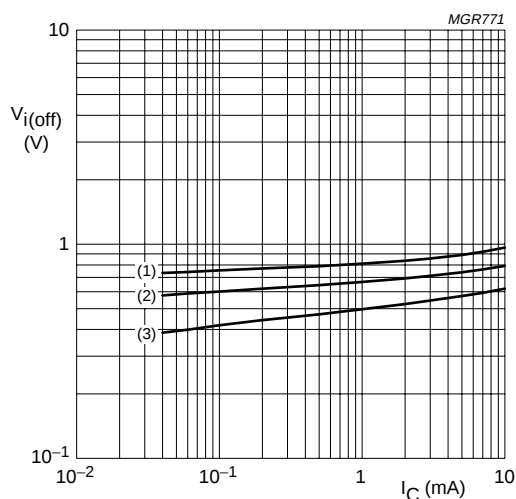
TR1 (NPN); $I_C/I_B = 20$.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.



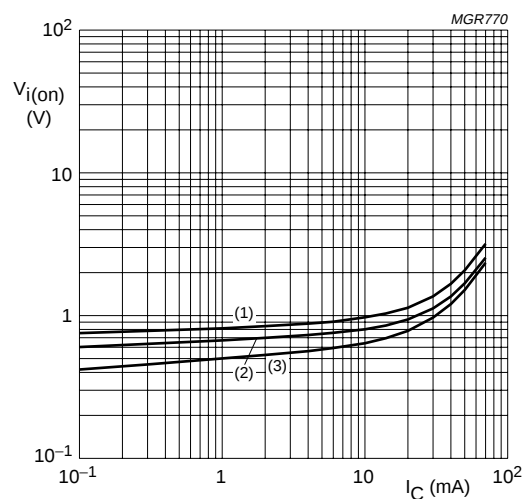
TR1 (NPN); $V_{CE} = 5$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.5 Input-off voltage as a function of collector current; typical values.



TR1 (NPN); $V_{CE} = 0.3$ V.

(1) $T_{amb} = -40$ °C.

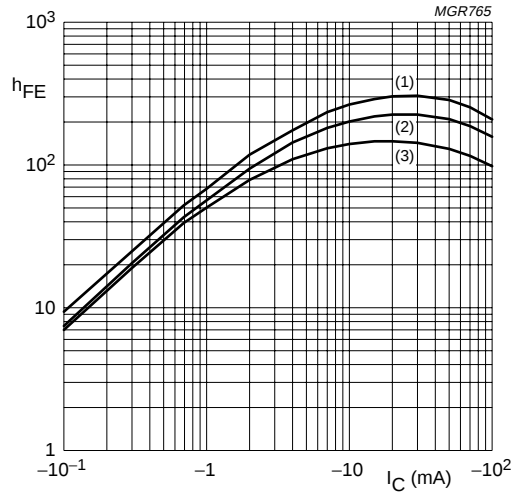
(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.6 Input-on voltage as a function of collector current; typical values.

NPN/PNP resistor-equipped transistors

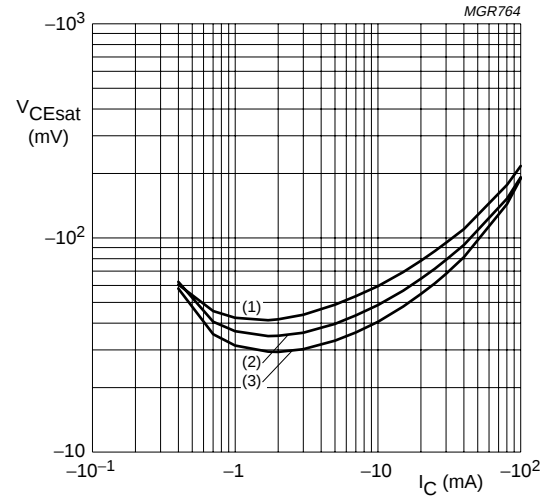
PUMD10



TR2 (PNP); $V_{CE} = -5$ V.

- (1) $T_{amb} = 100$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = -40$ °C.

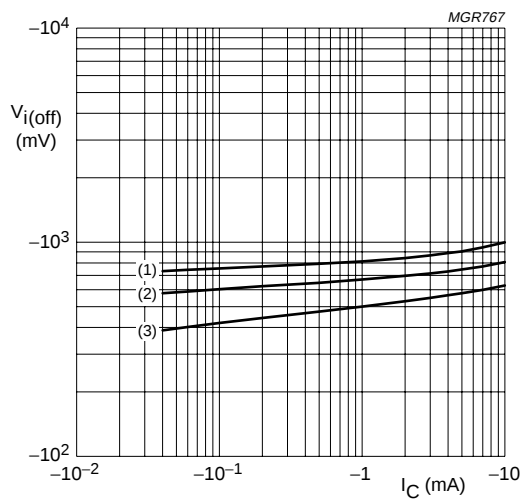
Fig.7 DC current gain as a function of collector current; typical values.



TR2 (PNP); $I_C/I_B = 20$.

- (1) $T_{amb} = 100$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = -40$ °C.

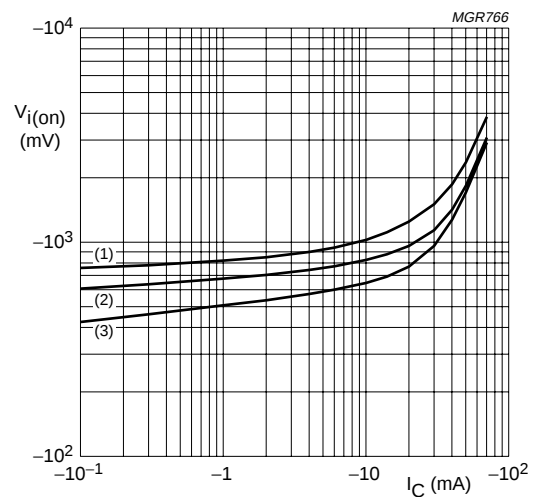
Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.



TR2 (PNP); $V_{CE} = -5$ V.

- (1) $T_{amb} = -40$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = 100$ °C.

Fig.9 Input-off voltage as a function of collector current; typical values.



TR2 (PNP); $V_{CE} = -0.3$ V.

- (1) $T_{amb} = -40$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = 100$ °C.

Fig.10 Input-on voltage as a function of collector current; typical values.

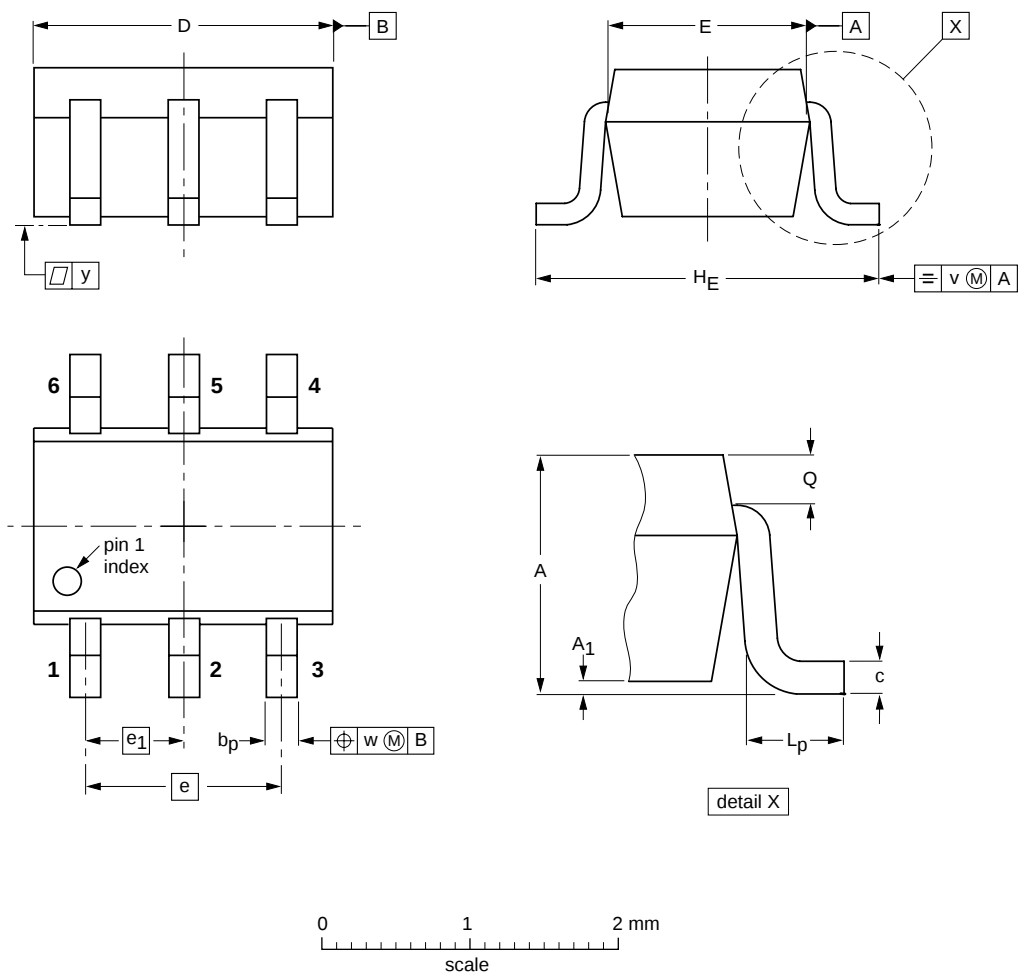
NPN/PNP resistor-equipped transistors

PUMD10

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

NPN/PNP resistor-equipped transistors

PUMD10

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN/PNP resistor-equipped transistors**PUMD10**

NOTES

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NOTES

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