Input voltage up to 144 V DC
Single output of 5.1...48 V DC
No input to output isolation

- Efficiency up to 97%
- Low input-output differential voltage
- No derating over temperature

Selection chart

Output $U_{o\,nom}$ [V DC]	Output $I_{o\,nom}$ [A]	Input voltage U_i [V DC]	Rated power $P_{o\,tot}$ [W]	Efficiency η_{typ} [%]	Type	Options
5.1	10	8...80	51	79	PSL 5A10-7R	-9, L, i, P, C, D, A
5.1	11	8...40	56.1	79	PSL 5A11-2R	
5.1	12	7...40	61.2	83	PSL 5A12-7R	-9, L, i, P, C, D, A
12	6	18...144	72	89	PSL 126-7R	-9, L, i, P, C, D, A
12	8	15...80	96	90	PSL 128-7R	-9, L, i, P, C, D, A
12	9	15...40	108	90	PSL 129-2R	
15	6	22...144	90	90	PSL 156-7R	-9, L, i, P, C, D, A
15	8	19...80	120	91	PSL 158-7R	-9, L, i, P, C, D, A
15	9	19...40	135	91	PSL 159-2R	
24	6	31...144	144	94	PSL 246-7R	-9, L, i, P, C, D, A
24	8	29...80	192	94	PSL 248-7R	-9, L, i, P, C, D, A
24	9	29...60	216	94	PSL 249-2R	
36	6	44...144	216	96	PSL 366-7R	-9, L, i, P, C, D, A
36	8	42...80	288	96	PSL 368-7R	-9, L, i, P, C, D, A
48	6	58...144	288	97	PSL 486-7R	-9, L, i, P, C, D, A

Input

Input voltage		refer to selection chart
No load input current		≤50 mA

Output

Efficiency	$U_{i\,nom}$, $I_{o\,nom}$	up to 97%
Output voltage setting accuracy	$U_{i\,nom}$, $I_{o\,nom}$	±0.6% $U_{o\,nom}$
Output voltage switching noise	IEC/EN 61204, total	typ. 0.4%
Line regulation	$U_{i\,min}$...$U_{i\,max}$, $I_{o\,nom}$	typ. ±0.3%
Load regulation	$U_{i\,nom}$, 0...$I_{o\,nom}$	typ. 0.3%
Minimum load	not required	0 A
Current limitation	rectangular U/I characteristic	typ. 110% $I_{o\,nom}$
Operation in parallel	by current limitation	

Protection

Input reverse polarity	with external fuse (built-in fuse with option C installed)	
Input undervoltage lockout		typ. 80% $U_{i\,min}$
Input transient protection	suppressor diode	
Output	no-load, overload and short circuit proof	
Output overvoltage	suppressor diode in each output	typ. 150% $U_{o\,nom}$

Safety

Approvals	EN 60950, UL 1950, CSA C22.2 No. 950	
Protection degree		IP 20
Electric strength test voltage	I/case and O/case	500/750/1500 V DC

EMC

Electrostatic discharge	IEC/EN 61000-4-2
Electromagnetic field	IEC/EN 61000-4-3
Electr. fast transients/bursts	IEC/EN 61000-4-4
Surge	IEC/EN 61000-4-5
Conducted disturbances	IEC/EN 61000-4-6
Electromagnetic emissions	CISPR 22/EN 55022

Environmental

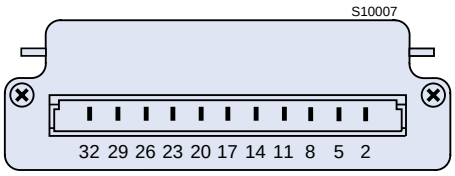
Operating ambient temperature	-2, $U_{i\,nom}$, $I_{o\,nom}$, convection cooled	–10...50°C
Operating case temperature T_C	-2, $U_{i\,nom}$, $I_{o\,nom}$	–10...80°C
Storage temperature	-2, non operational	–25...100°C
Operating ambient temperature	-7, $U_{i\,nom}$, $I_{o\,nom}$, convection cooled	–25...71°C
Operating case temperature T_C	-7, $U_{i\,nom}$, $I_{o\,nom}$	–25...95°C
Storage temperature	-7, non operational	–40...100°C
Damp heat	IEC/EN 60068-2-3	
Vibration, sinusoidal	IEC/EN 60068-2-6	
Shock	IEC/EN 60068-2-27	
Bump	IEC/EN 60068-2-29	
Random vibration	IEC/EN 60068-2-64	
MTBF	MIL-HDBK-217	

Options

Extended temperature range	–40...71°C, ambient, operating	-9
Inhibit, TTL input, output(s) enabled if left open		i
Output voltage adjustment	0...108% $U_{o\ nom}$	R
Additional internal input filter		L
Output voltage adjustment	±8% $U_{o\ nom}$	P
Thyristor crowbar on output		C
Input or output undervoltage monitoring		D/D1
Test sockets for check of output voltage		A

Pin allocation

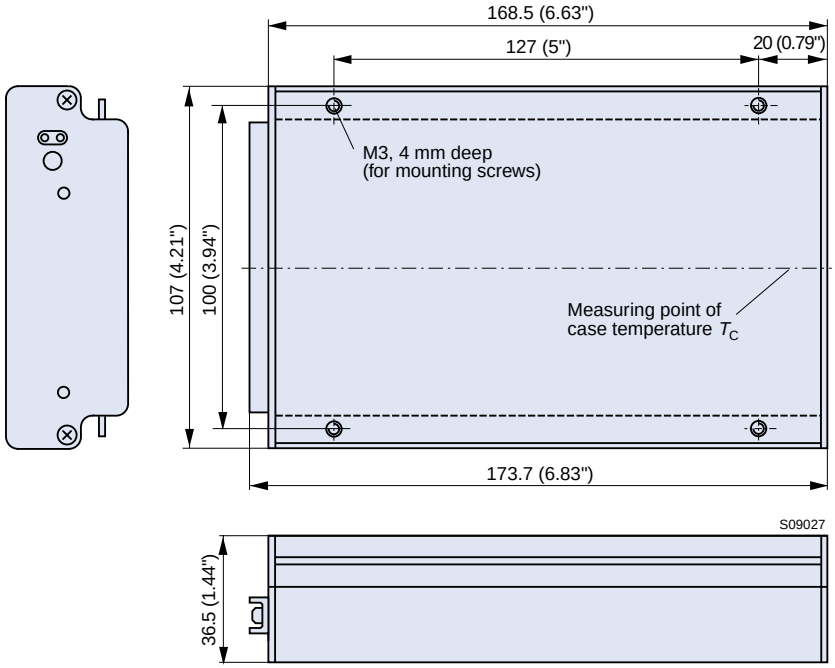
Pin	Electrical determination	Design.
2	R-input (or inhibit input)	R (i)
5	Undervoltage monitor (Option D)	D
8	Output voltage (negative)	Go–
11	Output voltage (negative)	Go–
14	Output voltage (positive)	Vo+
17	Output voltage (positive)	Vo+
20	Input voltage (negative)	Gi–
23	Input voltage (negative)	Gi–
26	Input voltage (positive)	Vi+
29	Input voltage (positive)	Vi+
32	Protective ground (leading pin)	⏚



Mechanical data

Tolerances ±0.3 mm (0.012") unless otherwise indicated.

European Projection



Accessories

Isolation pads for easy and safe PCB mounting
Ring core chokes for ripple and interference reduction