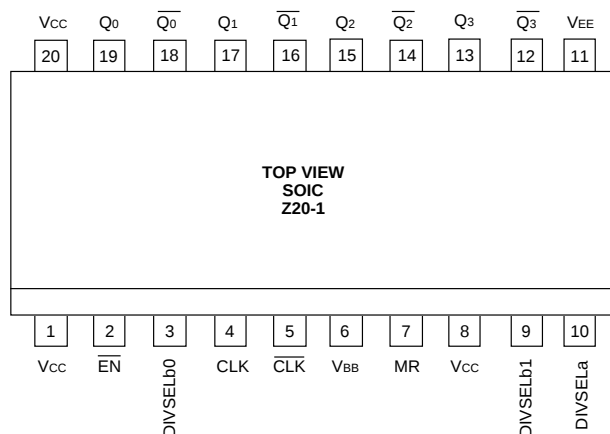


FEATURES

- 3.3V and 5V power supply option
- 50ps output-to-output skew
- 50% duty cycle outputs
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- Available in 20-pin SOIC package

PIN CONFIGURATION/BLOCK DIAGRAM



TRUTH TABLE

CLK	/EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0-3
X	X	H	Reset Q0-3

NOTE:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

DIVSELa	Q0, Q1 OUTPUTS
0	Divide by 2
1	Divide by 4

DIVSELb1	DIVSELb0	Q2, Q3 OUTPUTS
0	0	Divide by 4
0	1	Divide by 6
1	0	Divide by 5
1	1	Divide by 5

DESCRIPTION

The SY100S839V is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL/LVECL or, if positive power supplies are used, PECL/LVPECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the /CLK input and bypassed to ground via a 0.01μF capacitor. The VBB output is designed to act as the switching reference for the input of the S839V under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable (/EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one S839V, the MR pin need not be exercised as the internal divider designs ensures synchronization between the ÷2/4, and the ÷4/5/6 outputs of a single device.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
/EN	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q0, Q1	Differential ÷2/4 Outputs
Q2, Q3	Differential ÷4/5/6 Outputs
DIVSEL	Frequency Select Input

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

VEE = VEE (min) to VEE (max); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current	—	50	95	—	50	95	—	50	95	—	54	95	mA
VBB	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V
I _{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
V _{OH}	Output HIGH Voltage ⁽²⁾	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage ⁽²⁾	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{OHA}	Output HIGH Voltage ⁽³⁾	-1095	—	—	-1035	—	—	-1035	—	—	-1035	—	—	mV
V _{OLA}	Output LOW Voltage ⁽³⁾	—	—	-1555	—	—	-1610	—	—	-1610	—	—	-1610	mV
V _{IH}	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	-1165	—	-880	-1165	—	-880	mV
V _{IL}	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	mV
I _{IL}	Input LOW Current ⁽⁴⁾	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	μA

NOTE:

1. Parametric values specified at: -3.0V to -3.8V or -4.2V to -5.5V.
2. V_{IN} = V_{IH}(Max) or V_{IL}(Min): Loading with 50Ω to -2.0V.
3. V_{IN} = V_{IH}(Min) or V_{IL}(Max): Loading with 50Ω to -2.0V.
4. V_{IN} = V_{IL}(Min).

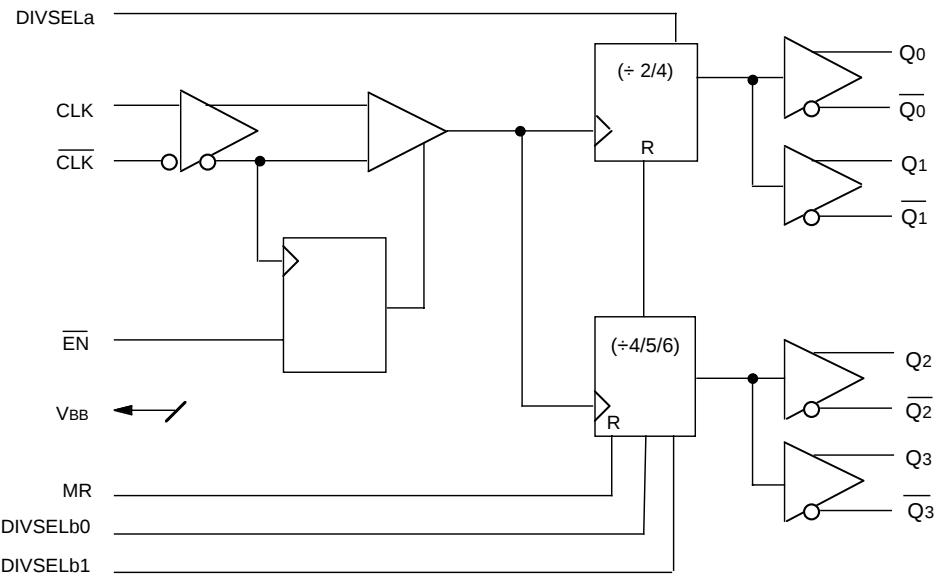
AC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = GND

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f _{MAX}	Maximum Toggle Frequency	1000	—	—	1000	—	—	1000	—	—	1000	—	—	MHz
t _{PLH} t _{PHL}	Propagation Delay to Output CLK → Output (Diff.) CLK → Output (S.E.) MR → Output	725 675 600	— — —	925 975 900	725 675 600	— — —	925 975 900	725 675 610	— — —	925 975 910	725 675 630	— — —	925 975 930	ps
t _{skew}	Within-Device Skew ⁽²⁾ Q ₀ — Q ₃ Part-to-Part Q ₀ — Q ₃ (Diff.)	— —	— —	50 200	— —	— —	50 200	— —	— —	50 200	— —	— —	50 200	ps
t _s	Set-up Time /EN → /CLK DIVSEL → CLK	250 400	— —	— —	250 400	— —	— —	250 400	— —	— —	250 400	— —	— —	ps
t _H	Hold Time /CLK → /EN CLK → DIVSEL	100 150	— —	— —	100 150	— —	— —	100 150	— —	— —	100 150	— —	— —	ps
V _{PP}	Minimum Input Swing ⁽³⁾ CLK	250	—	—	250	—	—	250	—	—	250	—	—	mV
V _{CMR}	Common Mode Range ^{(4), (5)}	-1.6	—	-0.4	-1.7	—	-0.4	-1.7	—	-0.4	-1.7	—	-0.4	V
t _{RR}	Reset Recovery Time	—	—	100	—	—	100	—	—	100	—	—	100	ps
t _{PW}	Minimum Pulse Width CLK MR	500 700	— —	— —	500 700	— —	— —	500 700	— —	— —	500 700	— —	— —	ps
t _r t _f	Output Rise/Fall Times (20% — 80%) Q	280	—	550	280	—	550	280	—	550	280	—	550	ps

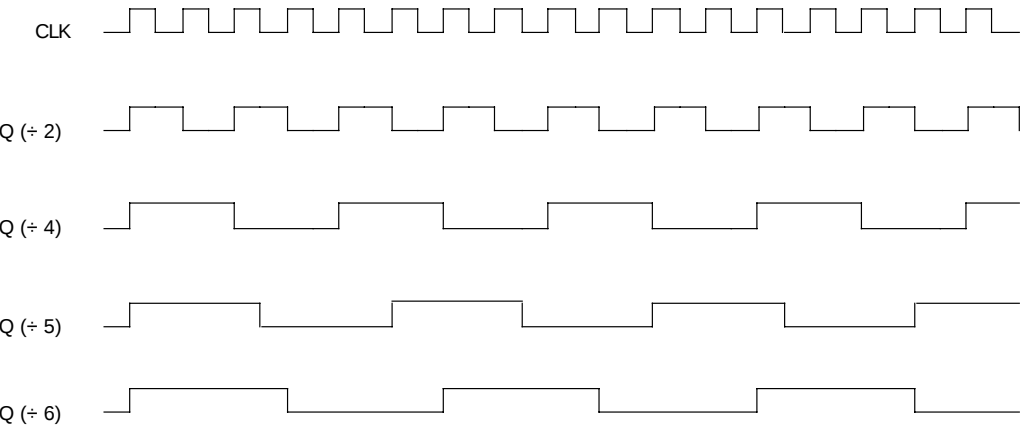
NOTES:

1. Parametric values specified at: -3.0V to -3.8V or -4.2V to -5.5V.
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – IV_{CMR} (min)I.
5. Duty Cycle: (Min. 48%; Max. 52%) } over temp.

LOGIC DIAGRAM

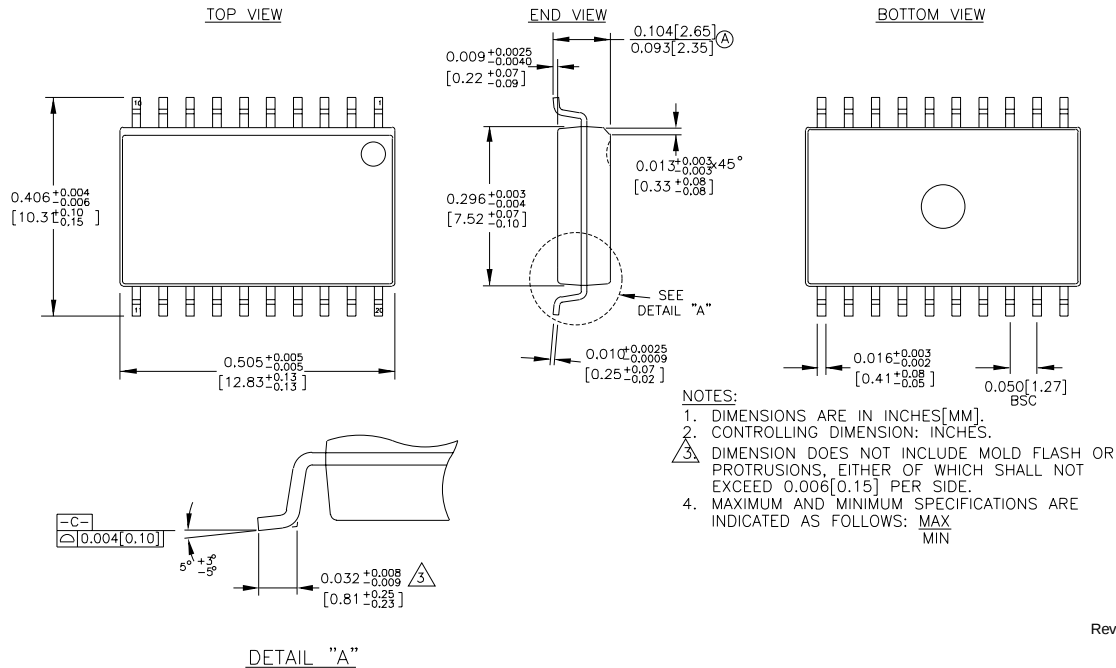


TIMING DIAGRAMS



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S839VZC	Z20-1	Commercial
SY100S839VZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)

Rev. 03

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