

DATA SHEET

PHN110

N-channel enhancement mode
MOS transistor

Product specification

1997 Jun 17

Supersedes data of 1996 Jul 16

File under Discrete Semiconductors, SC13b

N-channel enhancement mode
MOS transistor

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

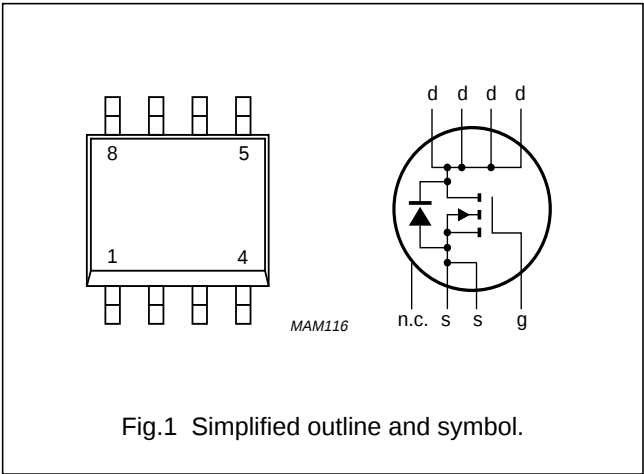
- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.



CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$I_S = 1.25\text{ A}$	–	1.2	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	$T_S = 80\text{ }^\circ\text{C}$	–	4	A
R_{DSon}	drain-source on-state resistance	$I_D = 2.2\text{ A}$; $V_{GS} = 10\text{ V}$	–	0.1	Ω
P_{tot}	total power dissipation	$T_S = 80\text{ }^\circ\text{C}$	–	2.8	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_S = 80\text{ }^{\circ}\text{C}$; note 1	–	4	A
I_{DM}	peak drain current	note 2	–	16	A
P_{tot}	total power dissipation	$T_S = 80\text{ }^{\circ}\text{C}$	–	2.8	W
		$T_{amb} = 25\text{ }^{\circ}\text{C}$; note 3	–	2.4	W
		$T_{amb} = 25\text{ }^{\circ}\text{C}$; note 4	–	1.1	W
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–65	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_S = 80\text{ }^{\circ}\text{C}$	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

- T_S is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Value based on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
- Value based on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

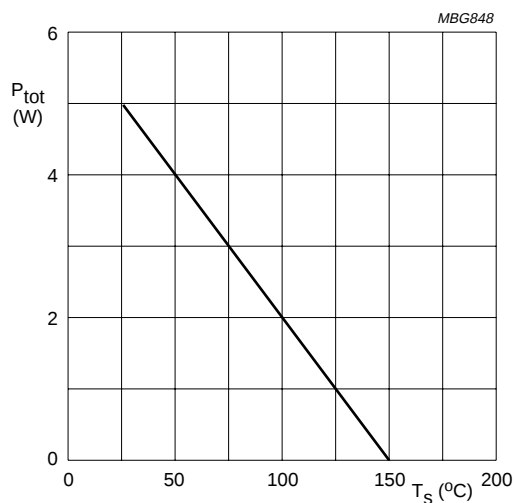


Fig.2 Power derating curve.

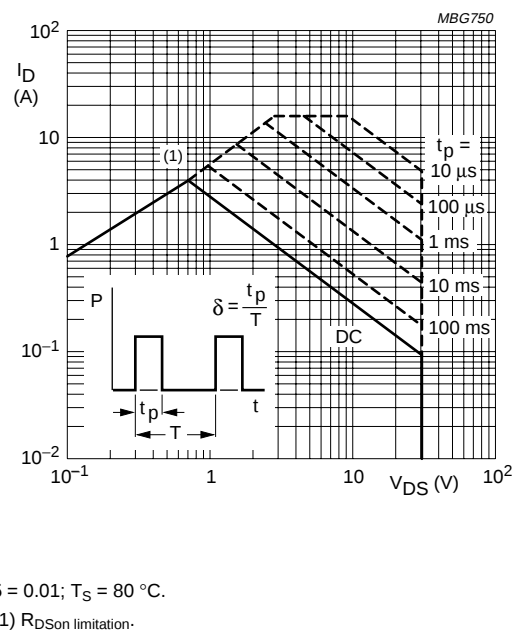


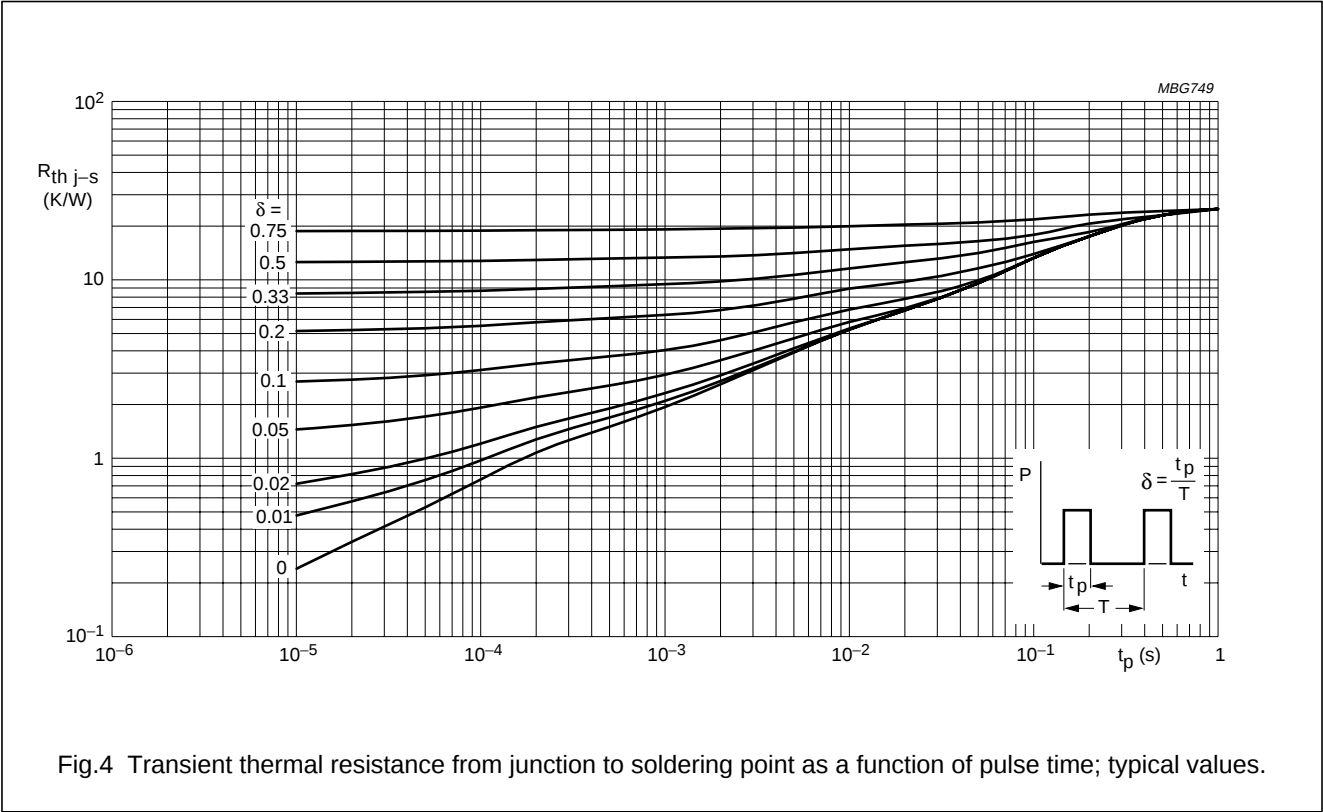
Fig.3 SOAR.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	25	K/W



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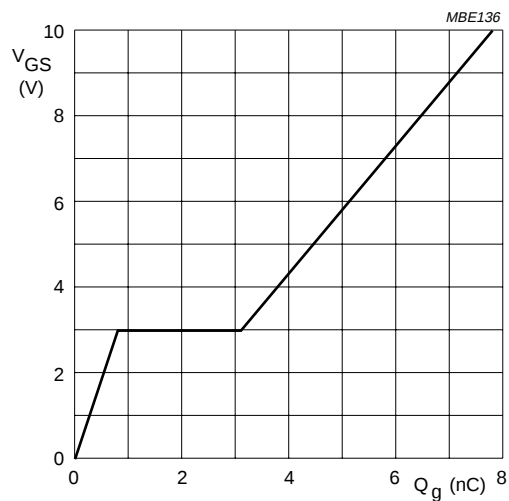
CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0; I _D = 10 μA	30	–	–	V
V _{GSth}	gate-source threshold voltage	V _{GS} = V _{DS} ; I _D = 1 mA	1	–	2.8	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 24 V	–	–	100	nA
I _{GSS}	gate leakage current	V _{GS} = ±20 V; V _{DS} = 0	–	–	±100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 1 A	–	0.11	0.2	Ω
		V _{GS} = 10 V; I _D = 2 A	–	0.08	0.1	Ω
C _{iss}	input capacitance	V _{GS} = 0; V _{DS} = 24 V; f = 1 MHz	–	250	–	pF
C _{oss}	output capacitance	V _{GS} = 0; V _{DS} = 24 V; f = 1 MHz	–	140	–	pF
C _{rss}	reverse transfer capacitance	V _{GS} = 0; V _{DS} = 24 V; f = 1 MHz	–	50	–	pF
Q _g	total gate charge	V _{GS} = 10 V; V _{DD} = 15 V; I _D = 2 A	–	10	30	nC
Q _{gs}	gate-source charge	V _{GS} = 10 V; V _{DD} = 15 V; I _D = 2 A	–	1	–	nC
Q _{gd}	gate-drain charge	V _{GS} = 10 V; V _{DD} = 15 V; I _D = 2 A	–	2.5	–	nC
Switching times (see Fig.11)						
t _{d(on)}	turn-on delay time	V _{GS} = 0 to 10 V; V _{DD} = 15 V; I _D = 1 A; R _L = 15 Ω; R _{gen} = 6 Ω	–	4.5	–	ns
t _f	fall time		–	3.5	–	ns
t _{on}	turn-on switching time		–	8	16	ns
t _{d(off)}	turn-off delay time	V _{GS} = 10 to 0 V; V _{DD} = 15 V; I _D = 1 A; R _L = 15 Ω; R _{gen} = 6 Ω	–	15	–	ns
t _r	rise time		–	10	–	ns
t _{off}	turn-off switching time		–	25	50	ns
Source-drain diode						
V _{SD}	source-drain diode forward voltage	V _{GD} = 0; I _S = 1.25 A	–	–	1.2	V
t _{rr}	reverse recovery time	I _S = 1.25 A; di/dt = –100 A/μs	–	35	100	ns

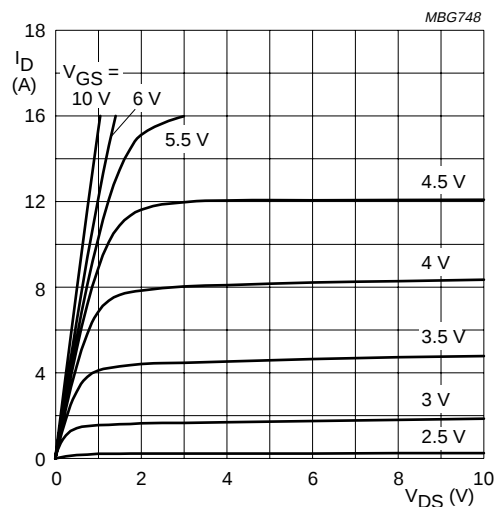
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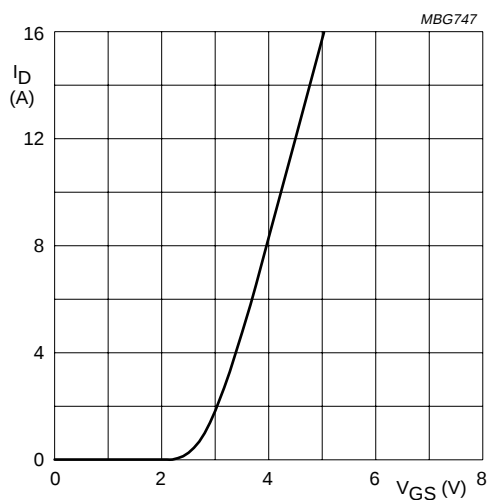
$V_{DD} = 15\text{ V}$; $I_D = 2\text{ A}$.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



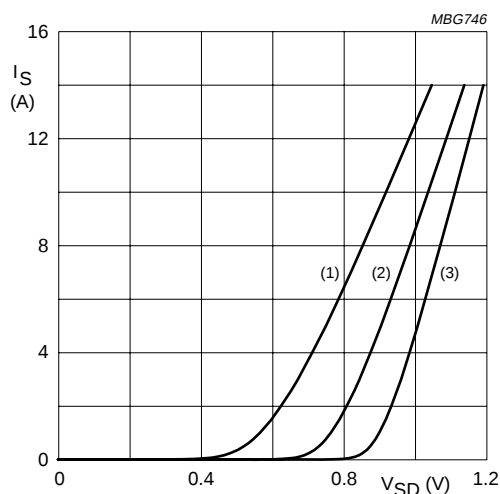
$T_j = 25\text{ }^{\circ}\text{C}$.

Fig.6 Output characteristics; typical values.



$V_{DS} = 10\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.

Fig.7 Transfer characteristics; typical values.



$V_{GD} = 0$.

(1) $T_j = 150\text{ }^{\circ}\text{C}$.

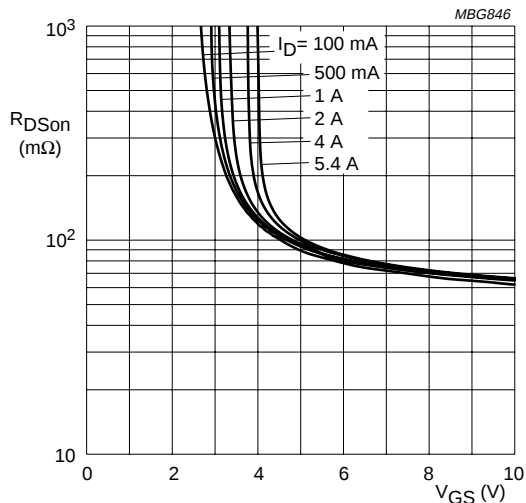
(2) $T_j = 25\text{ }^{\circ}\text{C}$.

(3) $T_j = -65\text{ }^{\circ}\text{C}$.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.

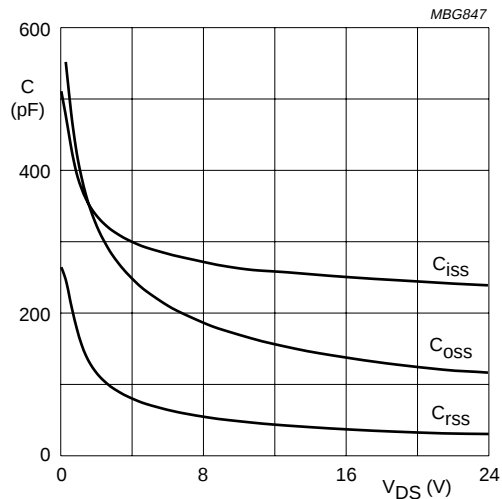
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$V_{DS} \geq I_D \times R_{DS(on)}$; $T_j = 25^\circ\text{C}$.

Fig.9 Drain-source on-resistance as a function of gate-source voltage; typical values.



$V_{GS} = 0$; $f = 1\text{ MHz}$; $T_j = 25^\circ\text{C}$.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

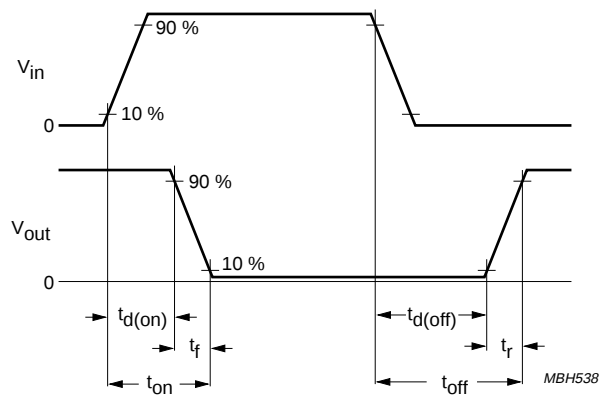
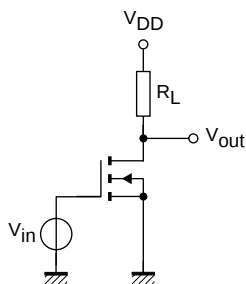
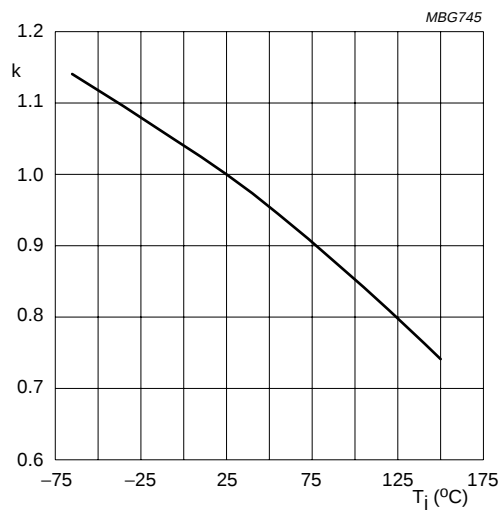


Fig.11 Switching time test circuit and input and output waveforms.

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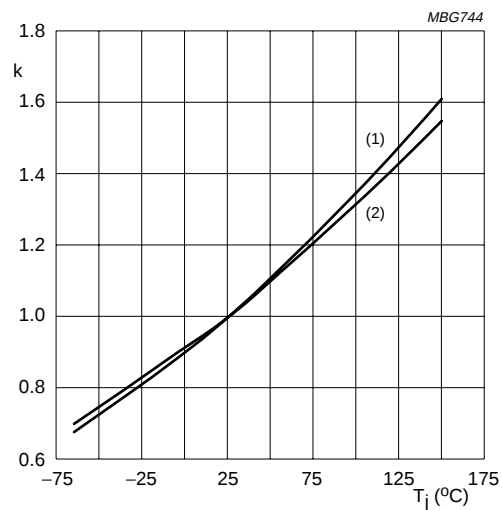
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$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

Typical V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}} \quad \text{Typical } R_{DSon} \text{ at:}$$

- (1) $I_D = 2$ A; $V_{GS} = 10$ V.
- (2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.13 Temperature coefficient of drain-source on-resistance; typical values.

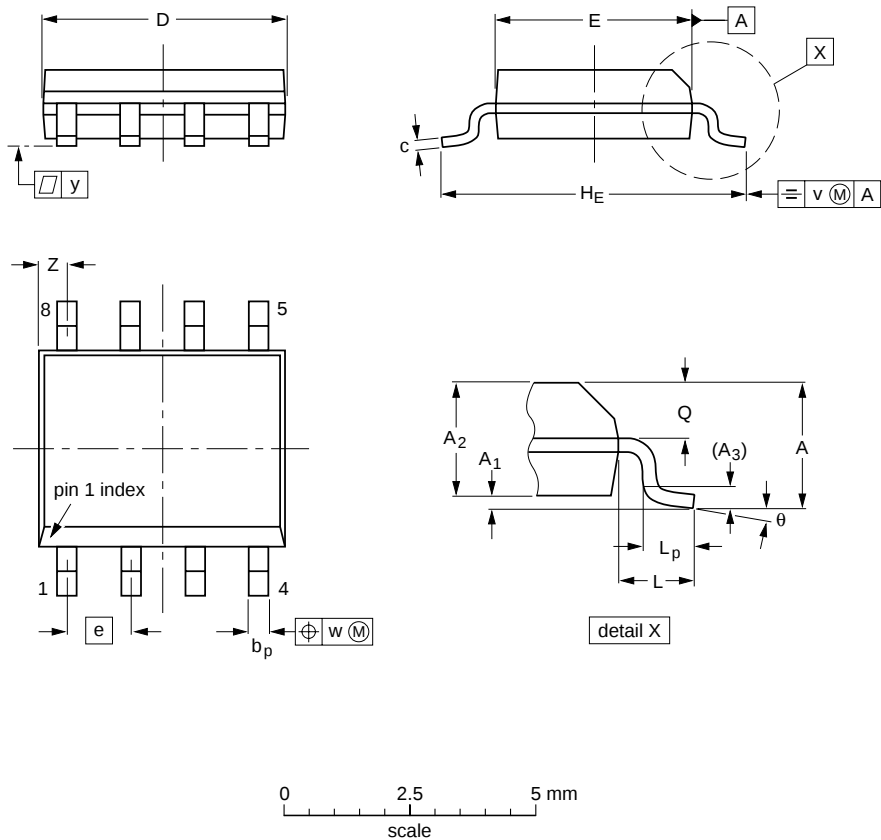
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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