

DATA SHEET

PCF1174C

4-digit static LCD car clock

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC16

1997 Apr 16

4-digit static LCD car clock

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FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

GENERAL DESCRIPTION

The PCF1174C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1174CT	VSO40	plastic very small outline package; 40 leads; face down ⁽¹⁾	SOT158-2
PCF1174CU	–	uncased chip in tray ⁽²⁾	–

Notes

1. See Fig.1 and Chapter “Package outline” for pin layout and package details.
2. See Chapter “Chip dimensions and bonding pad locations” for pad layout and package details.

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PINNING

SYMBOL	PIN	DESCRIPTION
BP	1	backplane output
PM	2	segment driver
AM	3	segment driver
ADEG1	4	segment driver
C1	5	segment driver
E2	6	segment driver
D2	7	segment driver
C2	8	segment driver
E3	9	segment driver
C3	10	segment driver
E4	11	segment driver
D4	12	segment driver
C4	13	segment driver
B4	14	segment driver
S1	15	hour adjustment input
DATA	16	EEPROM data input
OSC IN	17	oscillator input
OSC OUT	18	oscillator output
V _{SS}	19	negative supply
MODE	20	12/24-hour mode select input
V _{PP}	21	programming voltage input
TS	22	test speed-up mode input
ENABLE	23	set enable input for S1 and S2
V _{DD}	24	positive supply voltage
FLASH	25	colon option input
SEL	26	EEPROM select input
S2	27	minute adjustment input
A4	28	segment driver
F4	29	segment driver
G4	30	segment driver
B3	31	segment driver
AD3	32	segment driver
F3	33	segment driver
G3	34	segment driver
COL	35	segment driver
B2	36	segment driver
A2	37	segment driver
F2	38	segment driver
G2	39	segment driver
B1	40	segment driver

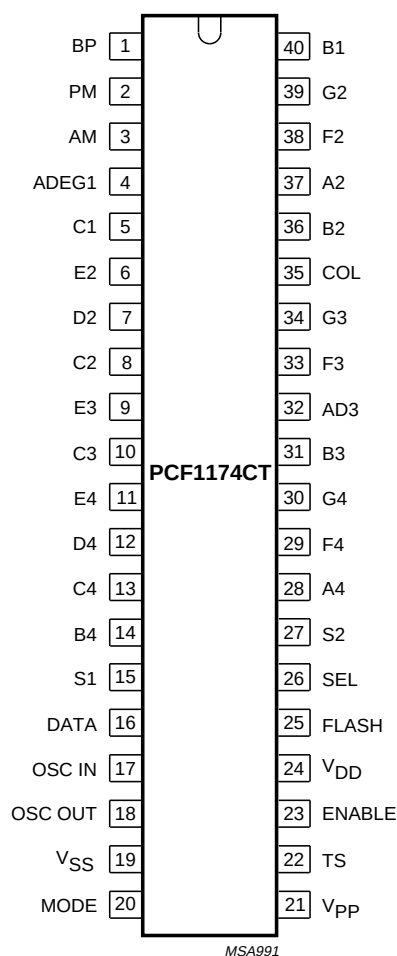


Fig.1 Pin configuration, PCF1174CT, (VSO40).

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FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig.4.

The average voltages across the segments are:

- 1. $V_{ON(RMS)} = V_{DD}$
- 2. $V_{OFF(RMS)} = 0\text{ V}$.

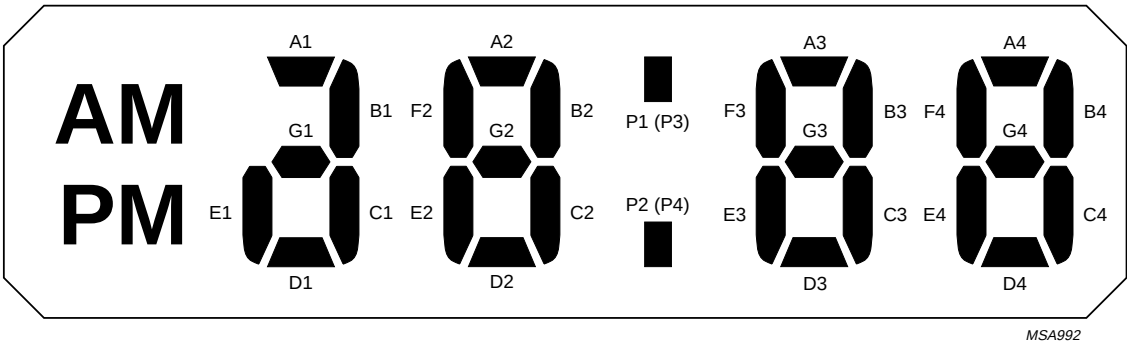


Fig.2 Segment designation of LCD.



(a)

a. 12-hour mode.



(b)

b. 24-hour mode.

Fig.3 Typical displays.

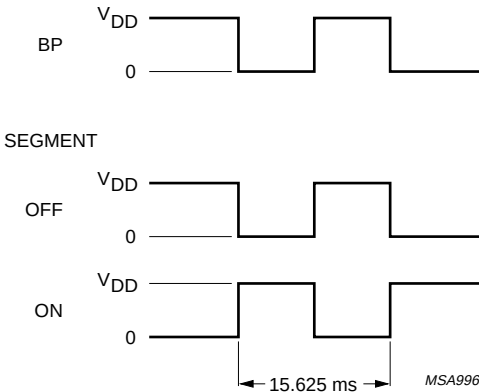


Fig.4 Backplane and output signals.

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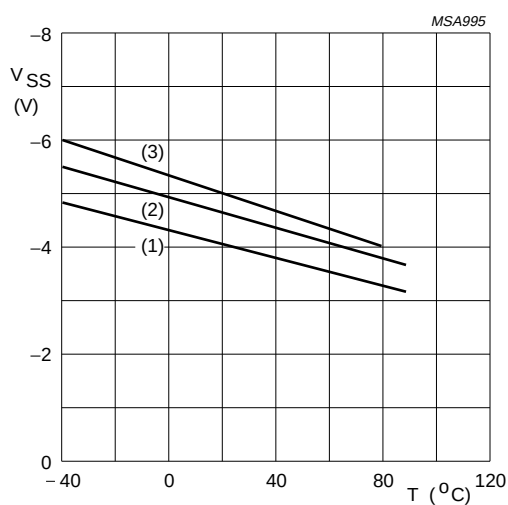
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LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section "LCD voltage programming") in relation to temperature for good contrast, for example when $V_{DD} = 4.5$ V at $+25$ °C, then:

$V_{DD} = 3$ to 4 V at $+85$ °C.

$V_{DD} = 5$ to 6 V at -40 °C.



- (1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
- (2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
- (3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

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12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode.

0:00; 24-hour mode.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz.
If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS} .

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS} , all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD} , the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD} .

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD} .

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV ($T_{amb} = 25$ °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps ($n = 31$) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262144 Hz pulses are inhibited every second of operation.

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The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of $V_{DD} - 5\text{ V}$ to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H , t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and (when correct) fixed by applying the store pulse t_W
6. Release SEL and V_{PP} .

Table 1 Time calibration ($\Delta t = 3.81\text{ }\mu\text{s}$; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.629
+7.6	2	15.633
+11.4	3	15.636
.	.	.
.	.	.
.	.	.
+117.8	31	15.743

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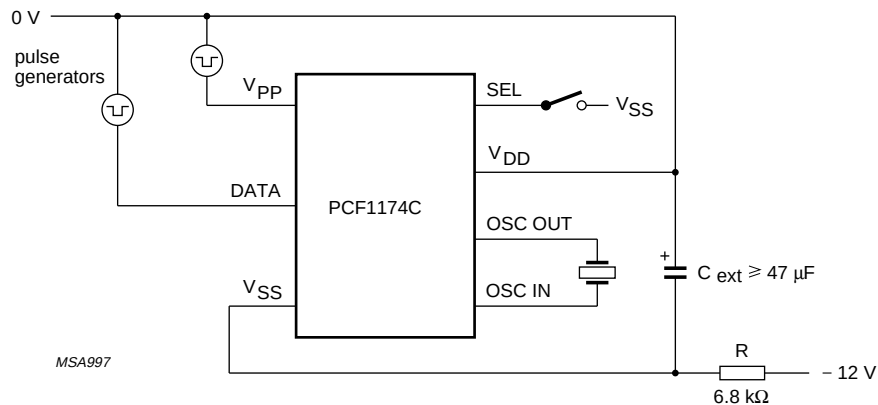
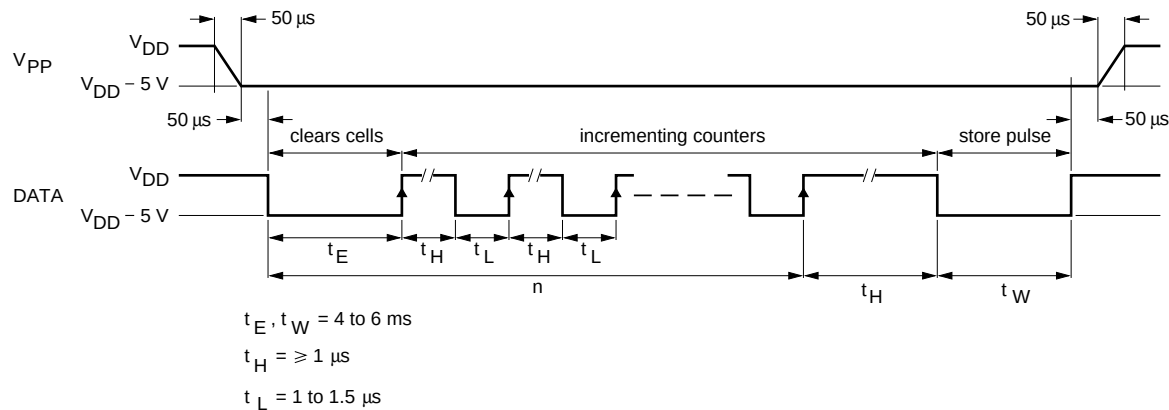


Fig.6 Programming diagram.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	$V_{SS} = 0$ V; note 1	–	3	mA
V_I	input voltage	all pins except V_{PP} and DATA	–0.3	$V_{DD} + 0.3$	V
		pins V_{PP} and DATA	–3	$V_{DD} + 0.3$	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in "Data Handbook IC16, General, Handling MOS Devices".

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CHARACTERISTICS

$V_{DD} = 3$ to 6 V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C; crystal: $f = 4.194304$ MHz; $R_s = 50$ Ω ; $C_L = 12$ pF; maximum frequency tolerance = $\pm 30 \times 10^{-6}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V _{DD}	supply voltage	voltage regulator programmed to 4.5 V at T _{amb} = 25 °C	3	–	6	V
ΔV _{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	–0.35	–	%/K
		V _{DD} = 4.5 V	–	–16	–	mV/K
I _{DD}	supply current	note 1	700	950	–	μA
C _{EXT}	capacitance	external capacitor	47	–	–	μF
Oscillator						
t _{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 × 10 ^{–6}	110 × 10 ^{–6}	
Δf/f	frequency stability	ΔV _{DD} = 100 mV	–	–	1 × 10 ^{–6}	
R _{fb}	feedback resistance		300	1000	3000	kΩ
C _i	input capacitance		–	16	–	pF
C _o	output capacitance		–	27	–	pF
Inputs						
R _O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
I _{IL}	leakage current	FLASH, ENABLE, MODE	–	–	2	μA
t _d	debounce time	S1 and S2 only	30	65	100	ms
V _{PP} programming voltage						
I _{O2}	output current	V _{PP} = V _{DD} – 5 V	70	–	700	μA
		during programming	–	500	–	μA
Backplane (high and low levels)						
R _{BP}	output resistance	±100 μA	–	–	3	kΩ
Segment						
R _{SEG}	output resistance	±100 μA	–	–	5	kΩ
LCD						
V _{offset(DC)}	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

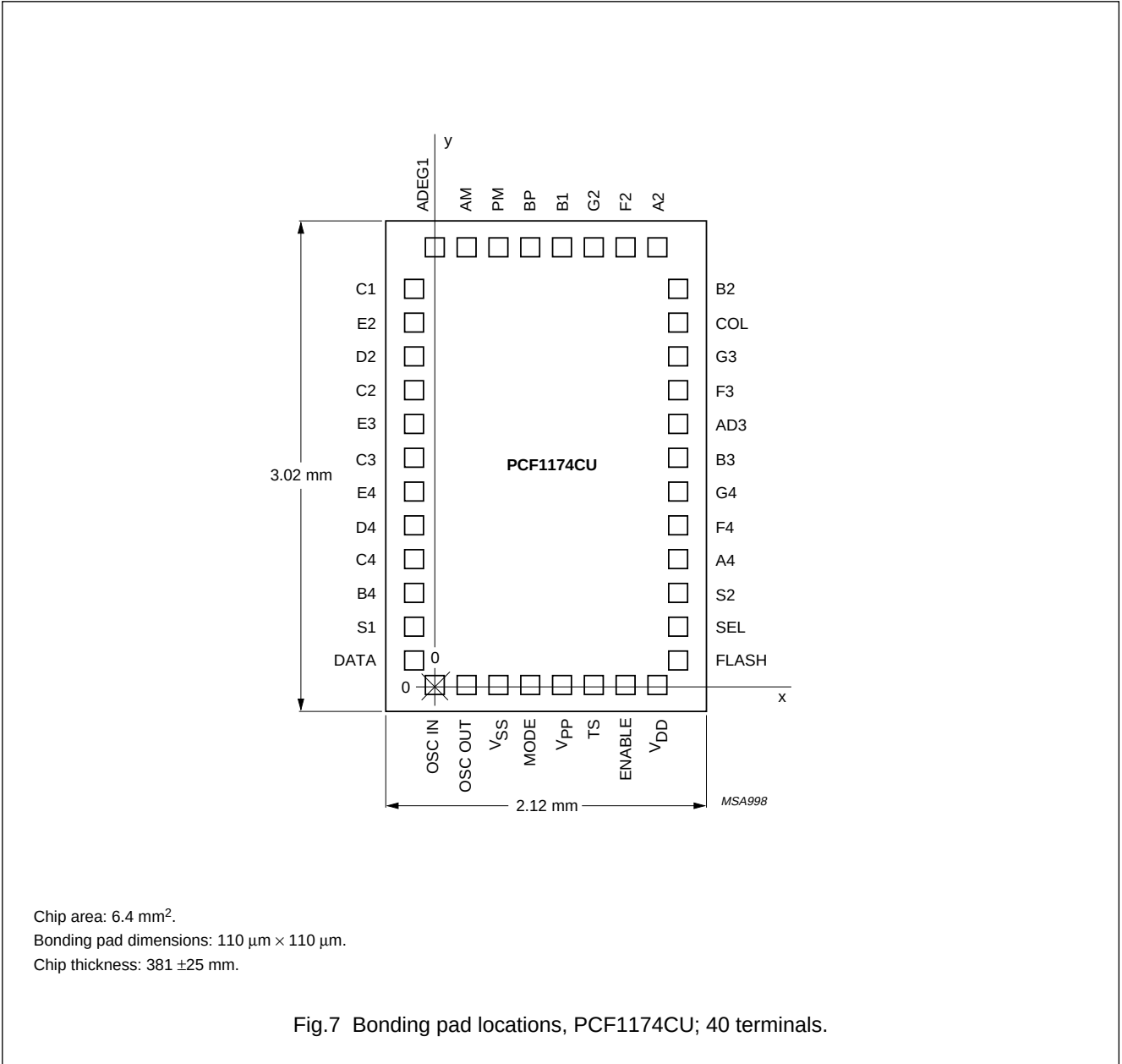
Note

- A suitable resistor (R) must be selected (example):
 - $V_{DD} = 5$ V; R max. $(12 \text{ V} - 5 \text{ V})/700 \text{ } \mu\text{A} = 10 \text{ k}\Omega$.
 - $V_{DD} = 5$ V; R typ. $(12 \text{ V} - 5 \text{ V})/900 \text{ } \mu\text{A} = 7.8 \text{ k}\Omega$ (more reserve).
 - I_{DD} must not exceed 3 mA.

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CHIP DIMENSIONS AND BONDING PAD LOCATIONS



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Table 2 Bonding pad locations (dimensions in μm)

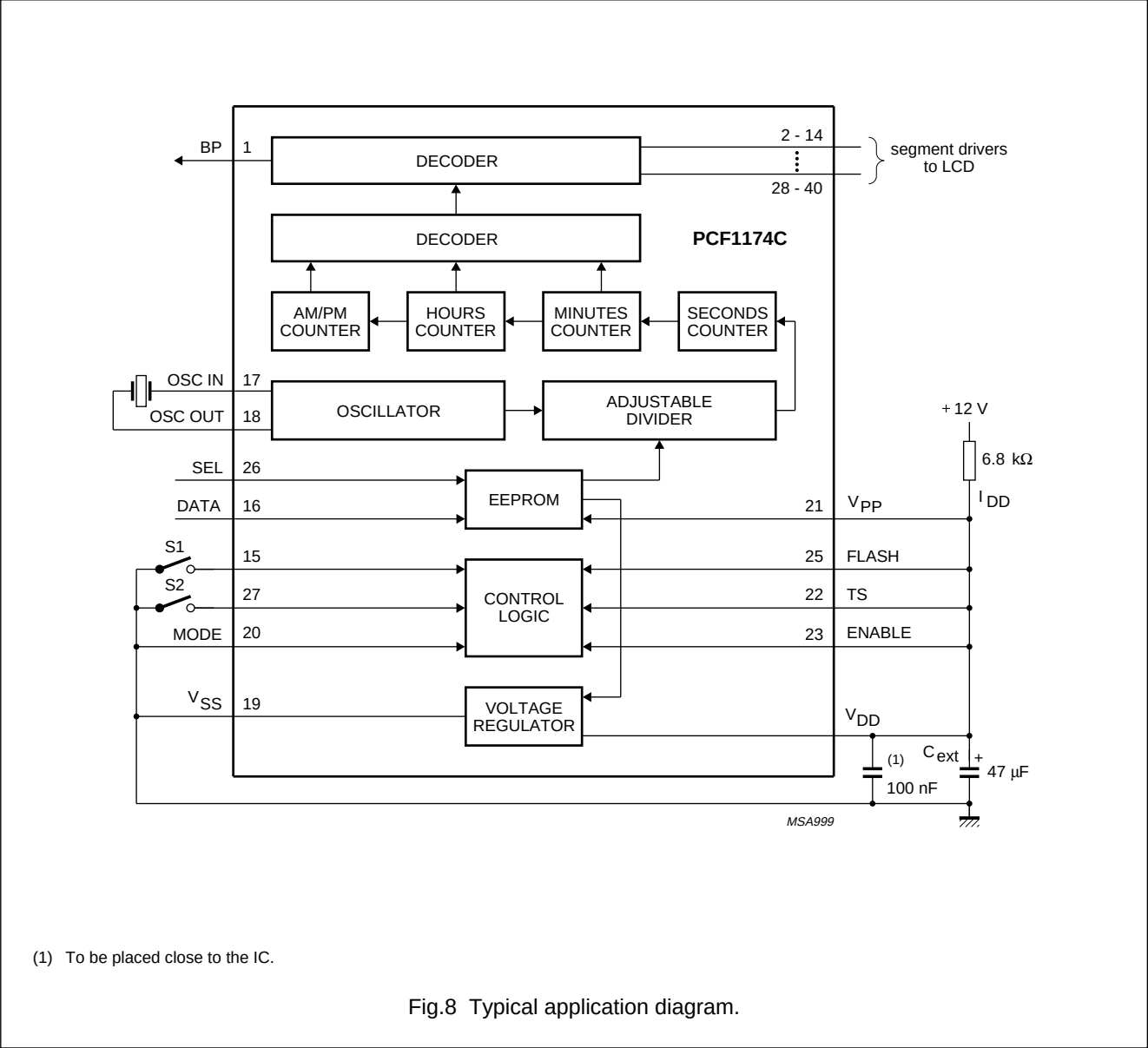
All x/y coordinates are referenced to the bottom left pad (OSC IN), see Fig.7.

PAD	x	y	PAD	x	y
BP	600	2676	V _{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V _{DD}	1400	0
C1	-138	2448	FLASH	1538	168
E2	-138	2228	SEL	1538	388
D2	-138	2008	S2	1538	608
C2	-138	1808	A4	1538	808
E3	-138	1608	F4	1538	1008
C3	-138	1408	G4	1538	1208
E4	-138	1208	B3	1538	1408
D4	-138	1008	AD3	1538	1608
C4	-138	808	F3	1538	1808
B4	-138	608	G3	1538	2008
S1	-138	388	COL	1538	2208
DATA	-138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V _{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max. value)	-360	-170			

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APPLICATION INFORMATION



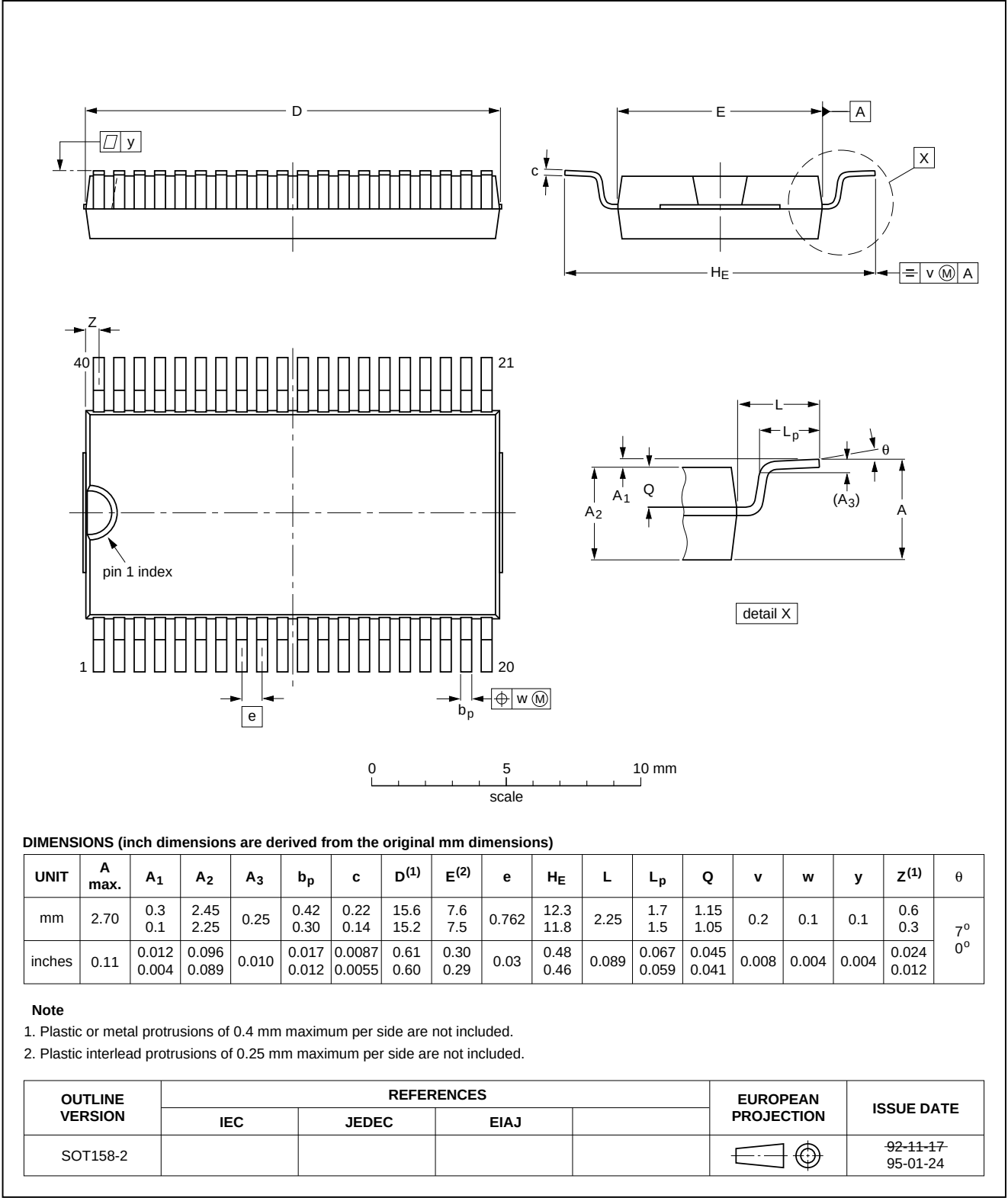
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PACKAGE OUTLINE

VSO40: plastic very small outline package; 40 leads; face down

SOT158-2



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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
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Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
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Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
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Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
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Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
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Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

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