
BB301M

Build in Biasing Circuit MOS FET IC
VHF RF Amplifier

HITACHI

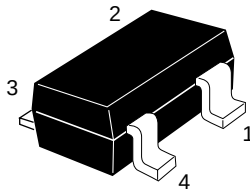
ADE-208-506
1st. Edition

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics; (NF = 1.3 dB typ. at $f = 200$ MHz)
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at $C = 200$ pF, $R_s = 0$ conditions.

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DS}	6	V
Gate 1 to source voltage	V _{G1S}	+6 −0	V
Gate 2 to source voltage	V _{G2S}	±6	V
Drain current	I _D	25	mA
Channel power dissipation	P _{ch}	150	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

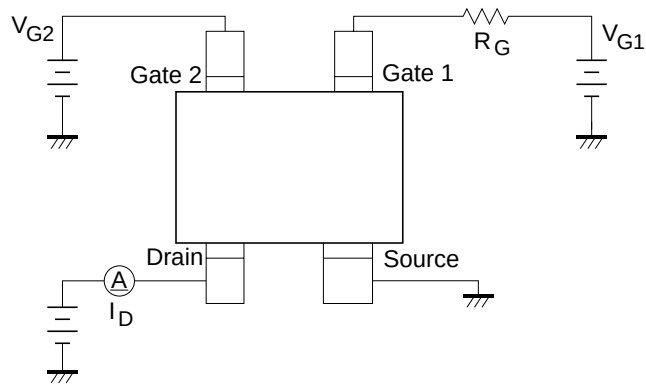
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A$ $V_{G1S} = V_{G2S} = 0$
Gate 1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A$ $V_{G2S} = V_{DS} = 0$
Gate 2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	$I_{G2} = \pm 10 \mu A$ $V_{G1S} = V_{DS} = 0$
Gate 1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V$ $V_{G2S} = V_{DS} = 0$
Gate 2 to source cutoff current	I_{G2SS}	—	—	±100	nA	$V_{G2S} = \pm 5 V$ $V_{G1S} = V_{DS} = 0$
Gate 1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	$V_{DS} = 5 V, V_{G2S} = 4 V$ $I_D = 100 \mu A$
Gate 2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	$V_{DS} = 5 V, V_{G1S} = 5 V$ $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	10	15	20	mA	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V, R_G = 100 k\Omega$
Forward transfer admittance	$ y_{fs} $	15	20	—	mS	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V$ $R_G = 100 k\Omega, f = 1 kHz$
Input capacitance	Ciss	2.2	3.0	4.0	pF	$V_{DS} = 5 V, V_{G1} = 5 V$
Output capacitance	Coss	0.9	1.2	1.6	pF	$V_{G2S} = 4 V, R_G = 100 k\Omega$
Reverse transfer capacitance	Crss	—	0.018	0.04	pF	$f = 1 MHz$
Power gain	PG	22	26	—	dB	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V$
Noise figure	NF	—	1.3	1.9	dB	$R_G = 100 k\Omega, f = 200 MHz$

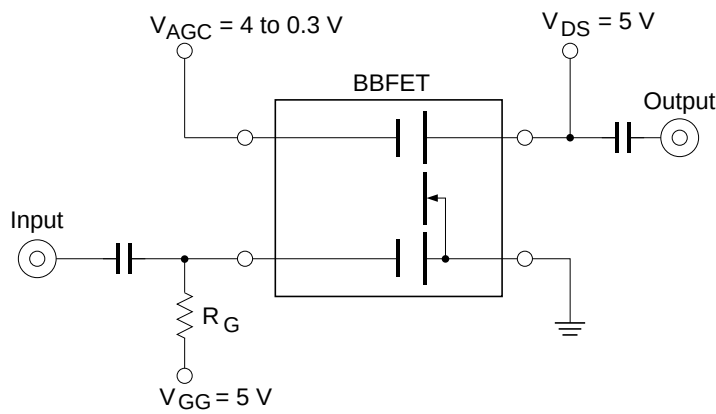
Note: Marking is “AW—”.

Main Characteristics

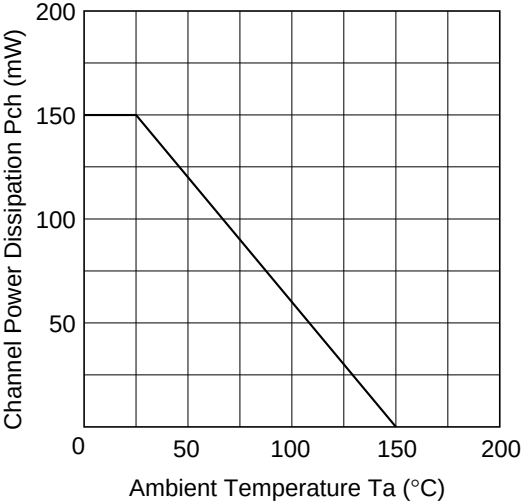
Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)



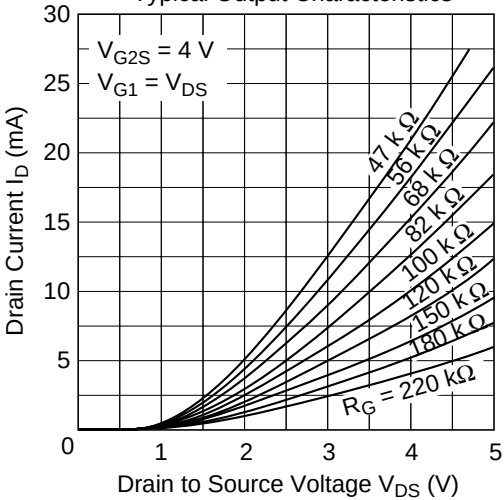
Application Circuit



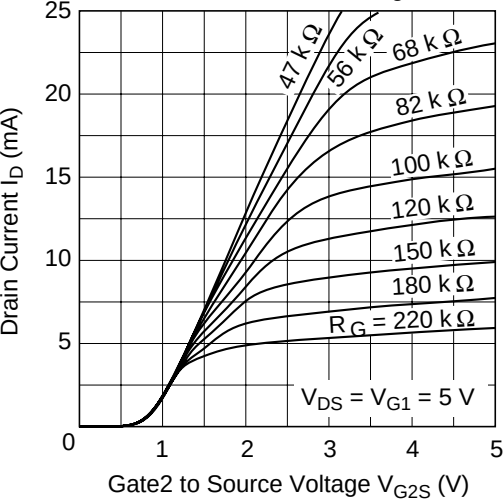
Maximum Channel Power
Dissipation Curve



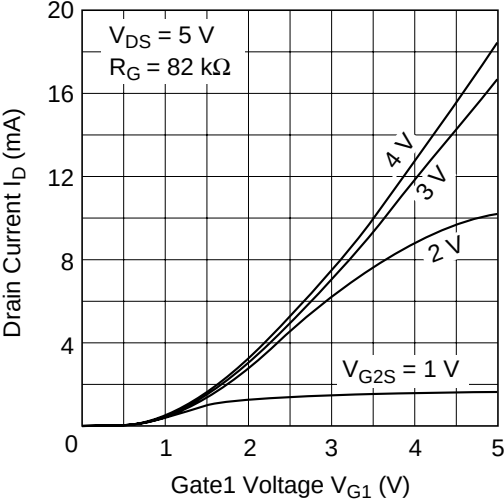
Typical Output Characteristics

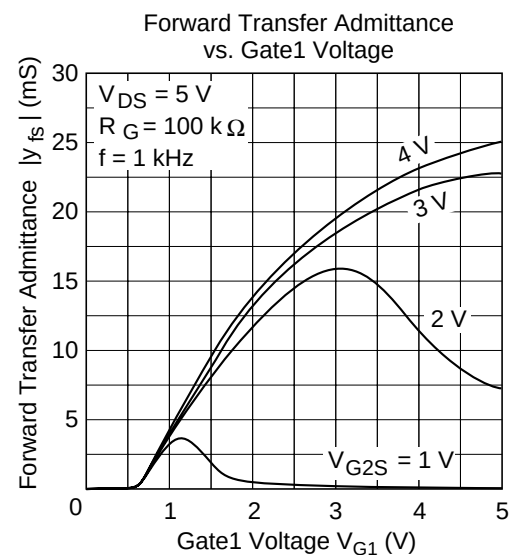
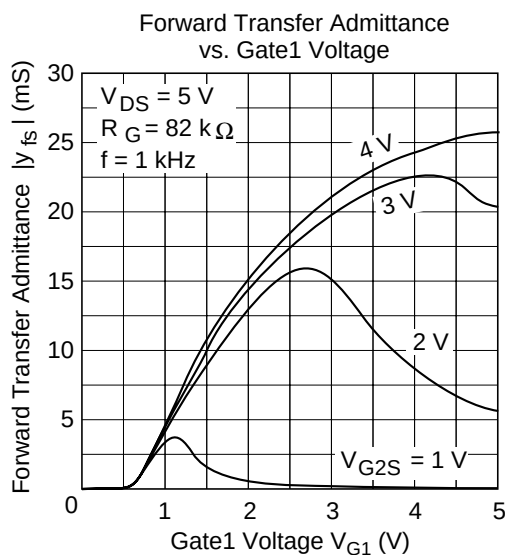
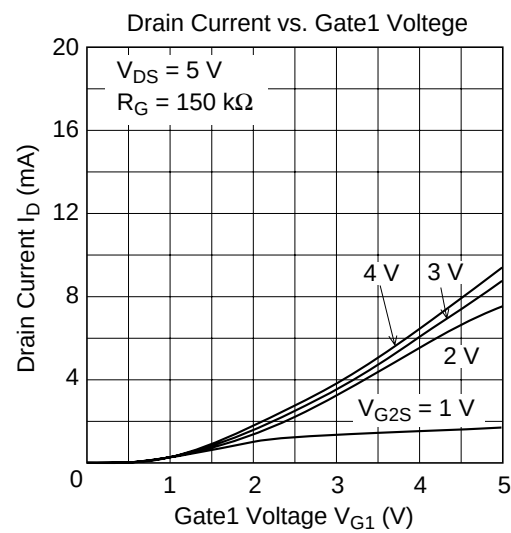
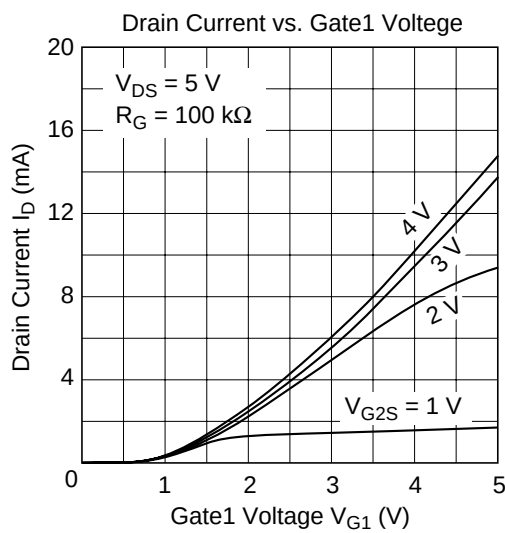


Drain Current vs.
Gate2 to Source Voltage

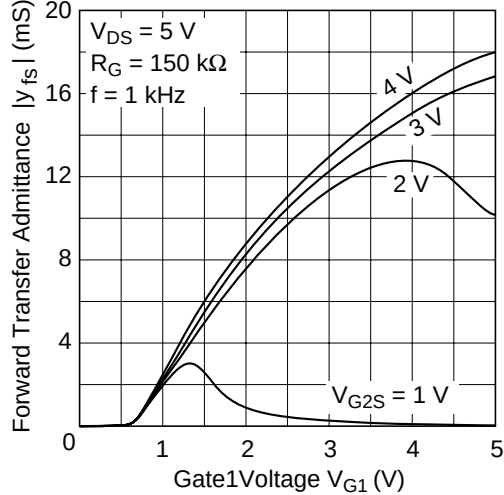


Drain Current vs. Gate1 Voltage

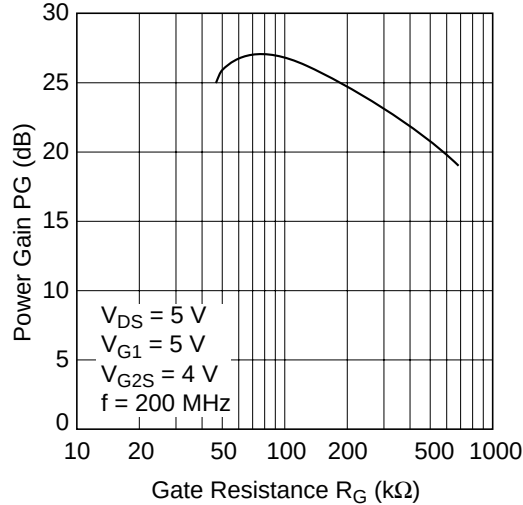




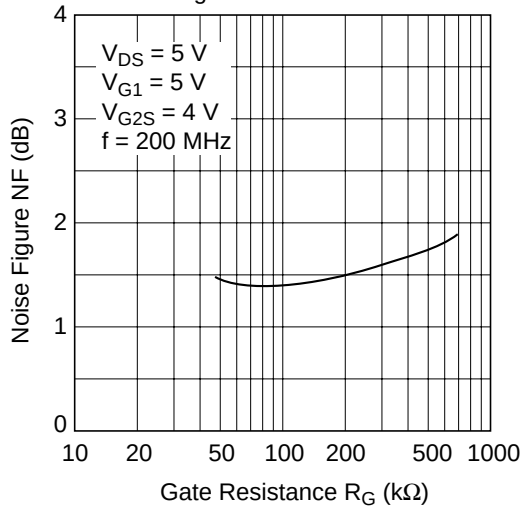
Forward Transfer Admittance
vs. Gate1 Voltage



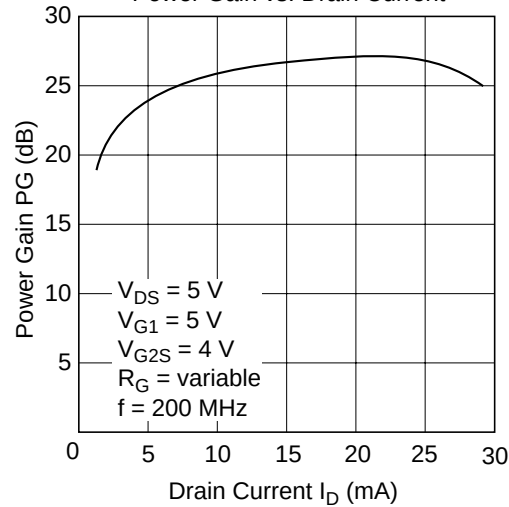
Power Gain vs. Gate Resistance

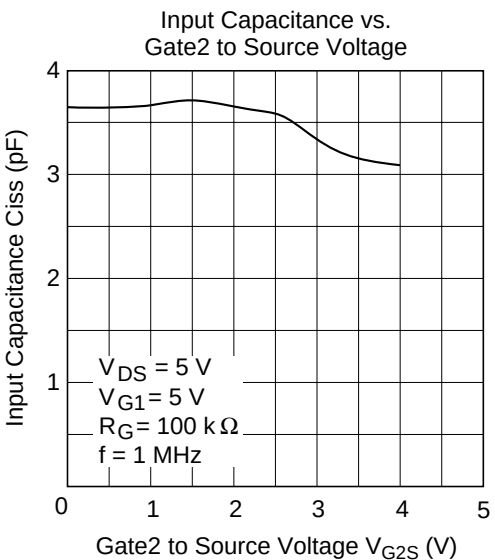
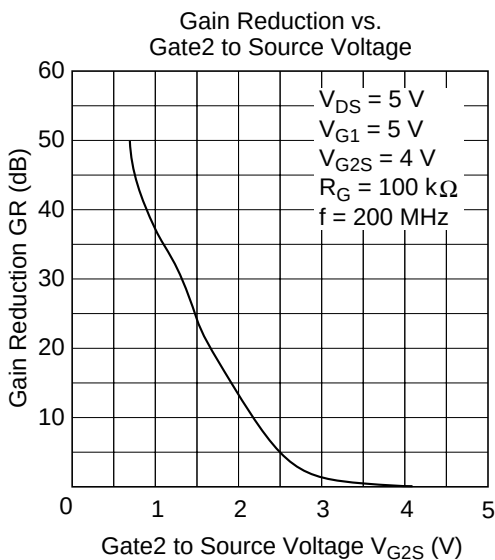
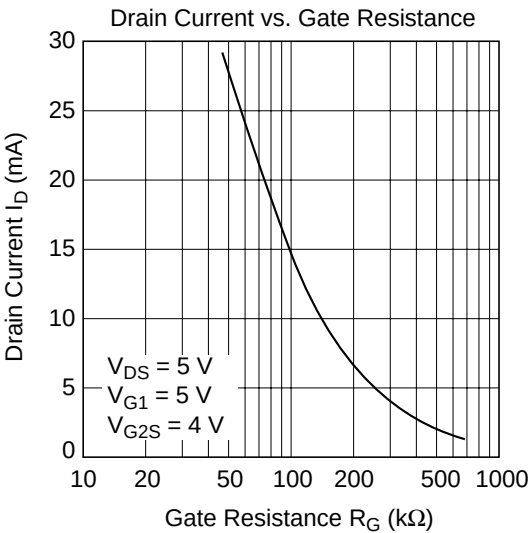
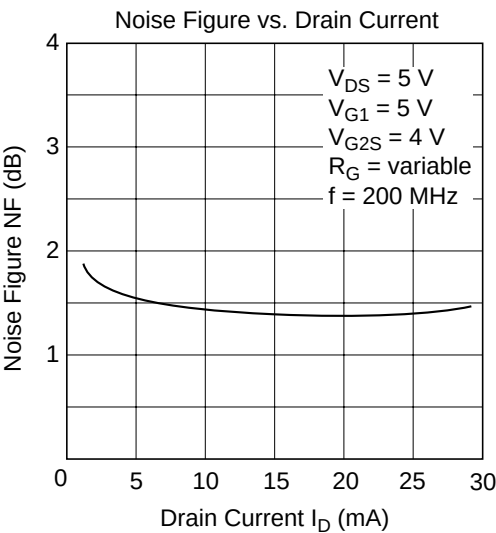


Noise Figure vs. Gate Resistance



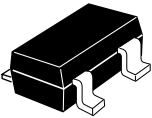
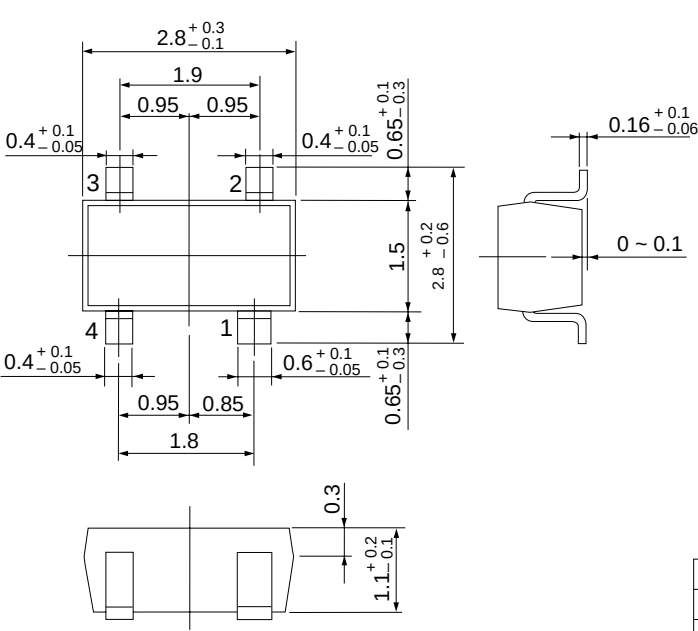
Power Gain vs. Drain Current





Package Dimentions

Unit: mm



Hitachi Code	MPAK-4
EIAJ	SC-61AA
JEDEC	—

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