

17-20GHz Integrated Down Converter

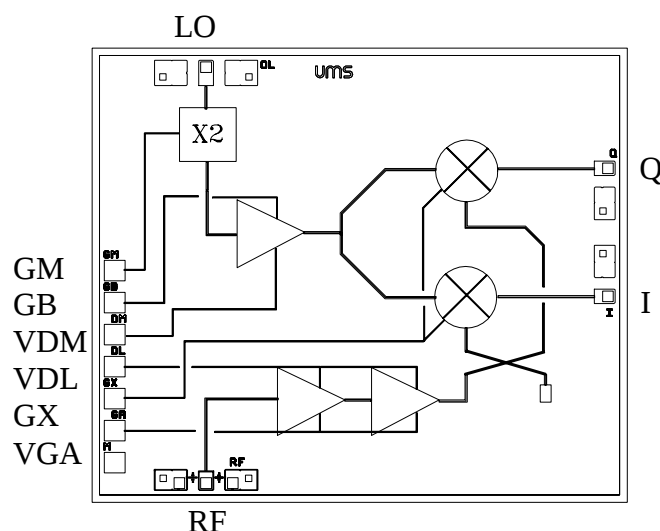
GaAs Monolithic Microwave IC

preliminary

Description

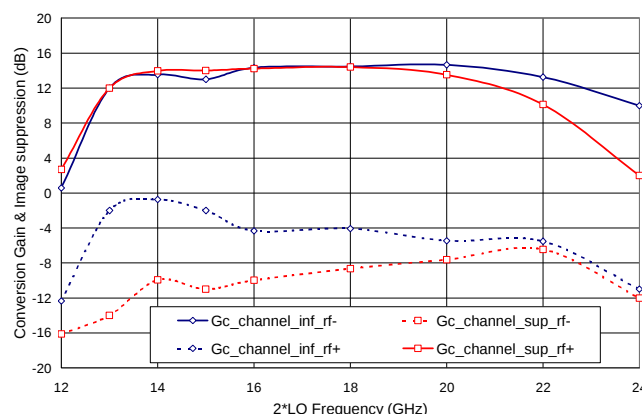
The CHR2292 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Main Features

- Broadband performances : 17-20GHz
- 13dB conversion gain
- 4.0dB noise figure
- 10dBm LO input power
- -10dBm RF input power (1dB gain comp.)
- Low DC power consumption, 110mA@3.5V
- Chip size : 2.49 X 2.13 X 0.10 mm



Conversion Gain for F_{IF}=1GHz (on wafer meas.)
P_{LO}=+10dBm / P_{RF}= -20dBm

Main Characteristics

T_{amb.} = 25°C

	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	17		20	GHz
F _{LO}	LO frequency range	7.5		10	GHz
F _{IF}	IF frequency range	0.25		1.5	GHz
G _c	Conversion gain		13		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics for Broadband Operation

T_{amb} = +25°C, V_d = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	17		20	GHz
F _{LO}	LO frequency range	7.5		10	GHz
F _{IF}	IF frequency range	0.25		1.5	GHz
P _{LO}	LO Input power		+10		dBm
G _c	Conversion gain (1)		13		dB
NF	Noise Figure (1)		4.0		dB
Img Sup	Image Suppression (1)		15		dBc
P1dB	RF Input power at 1dB gain compression (1)		-10		dBm
LO VSWR	Input LO VSWR (1)		1.5:1		
RF VSWR	Input RF VSWR (1)		2.5:1		
I _d	Bias current (2)		110		mA

(1) On Wafer measurements without bonding wires at the RF ports.

(2) Current source biasing network is recommended. Optimum performances for I_{dm}=50mA and I_{dl}=60mA

Absolute Maximum Ratings

T_{amb.} = 25°C (1)

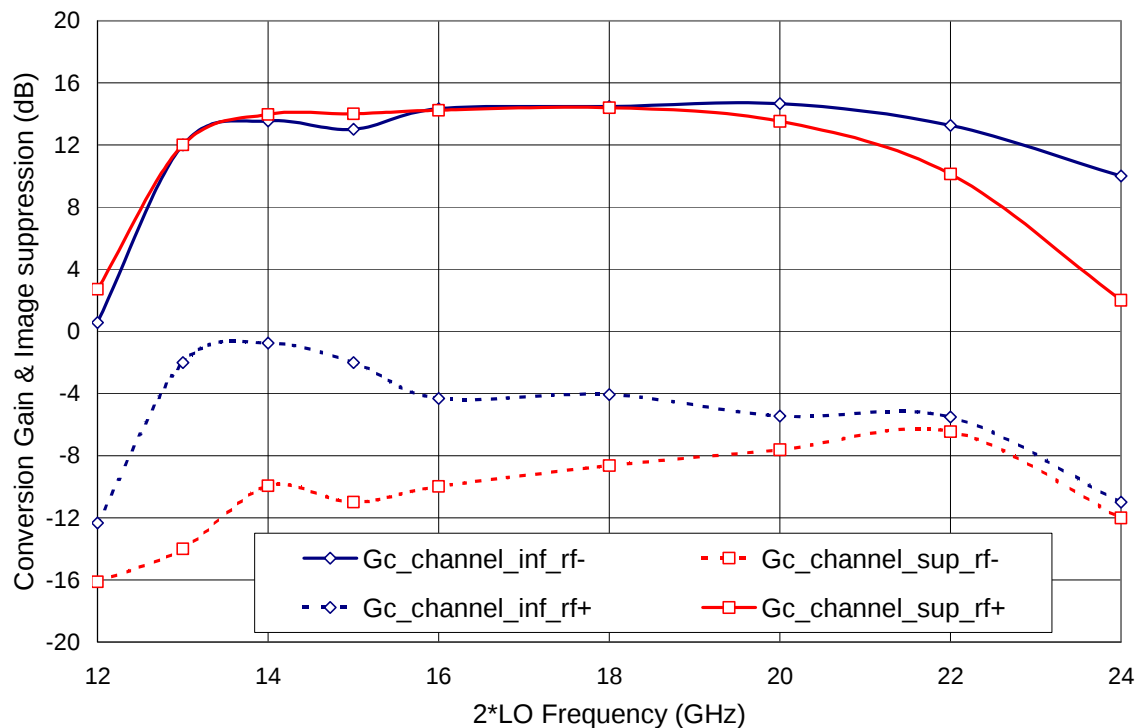
Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4.0	V
I _d	Drain bias current	200	mA
V _g	Gate bias voltage	-2.0 to +0.4	V
P _{in}	Maximum peak input power overdrive (2)	+15	dBm
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

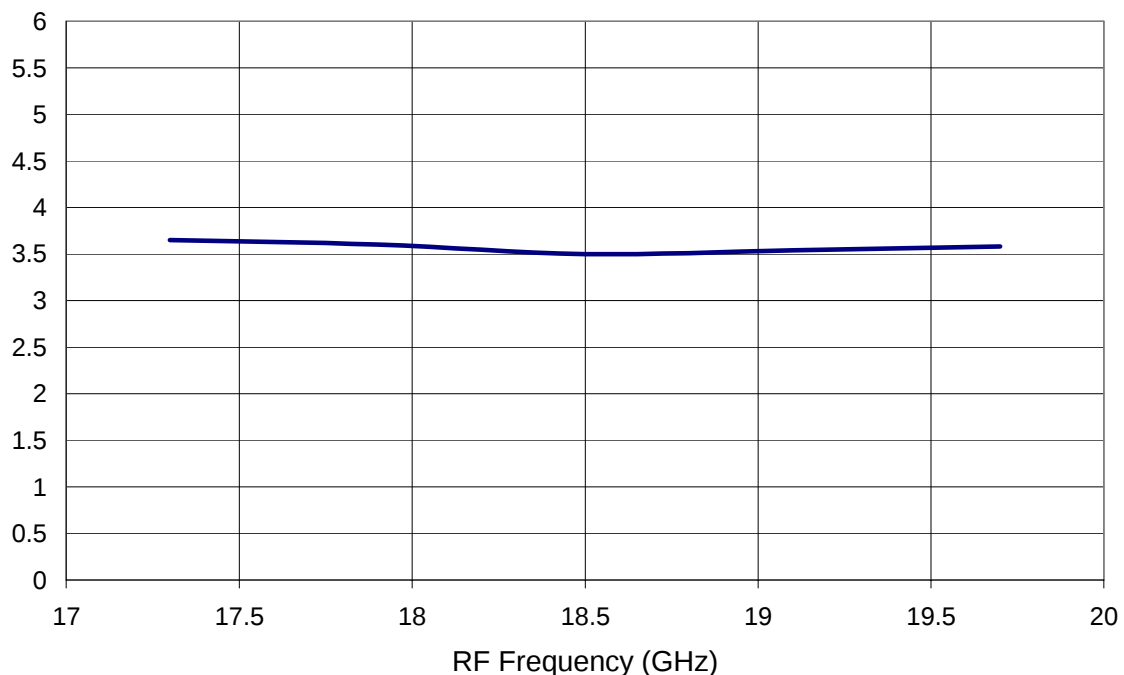
(2) Duration < 1s.

Typical On-wafer Measurements

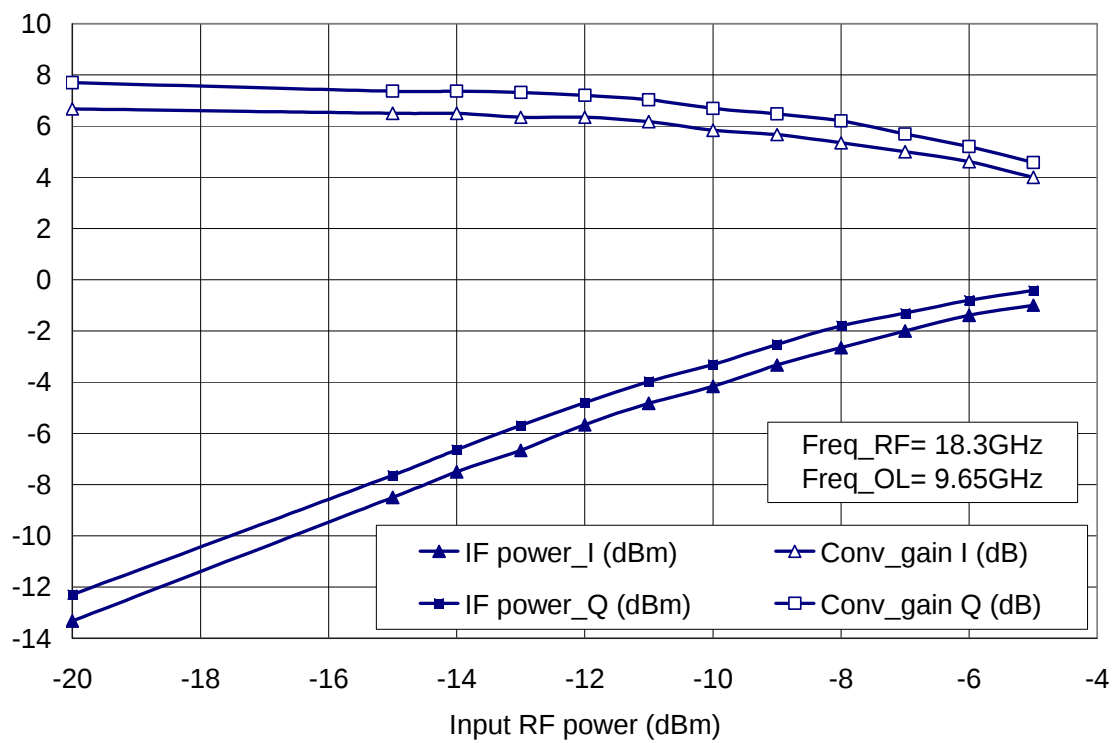
Bias Conditions : $V_{dm} = V_{dl} = 3.5\text{ V}$, $V_{gm} = -0.9\text{ V}$, $V_{gb} = 0.4\text{ V}$, $V_{gx} = -0.7\text{ V}$, $V_{ga} = -0.35\text{ V}$



Conversion Gain & Image Suppression @ IF=1GHz

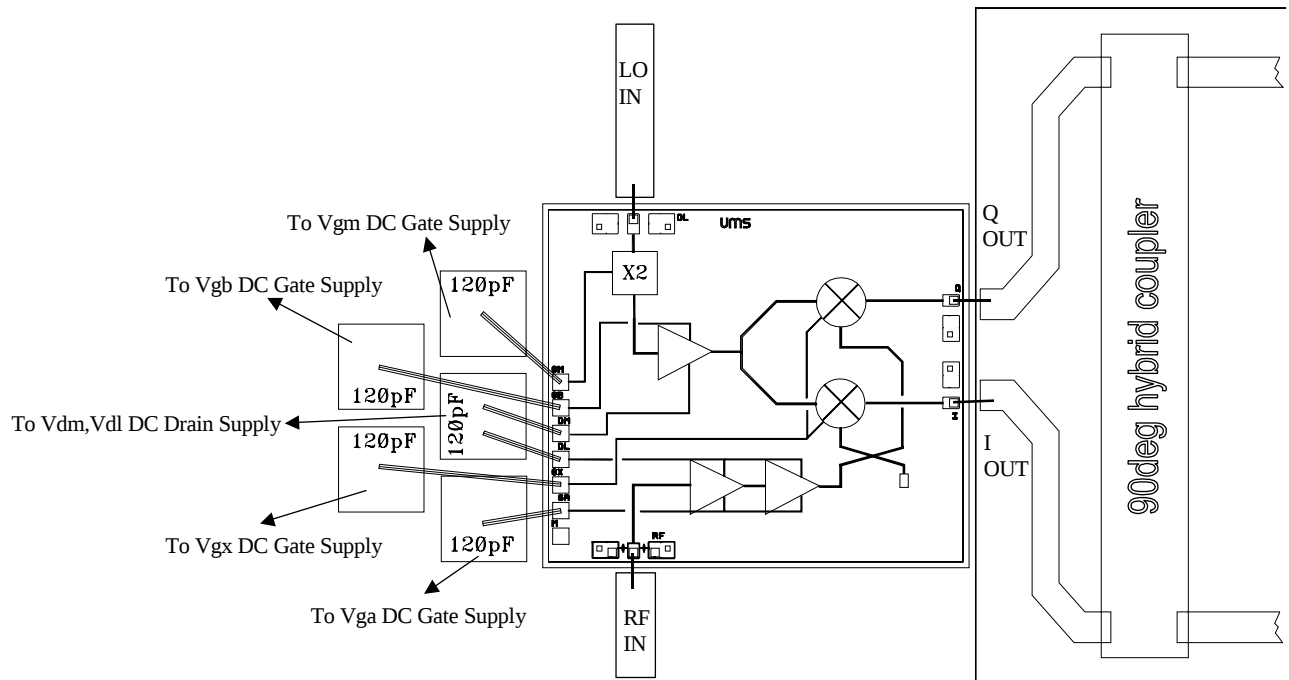


Noise figure (dB) by channel

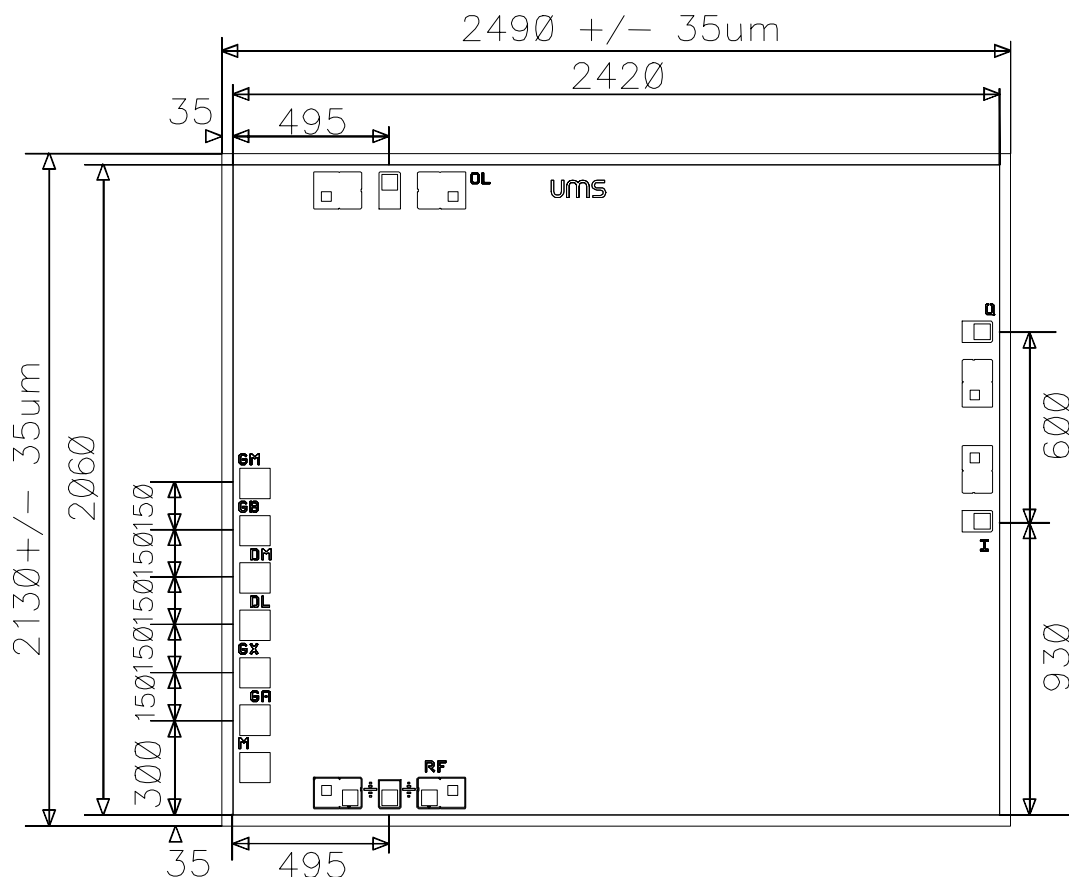


Input RF compression by channel

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions

(Chip thickness : 100 μ m. All dimensions are in micrometers)

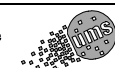
Ref. : DSCHR22921201 -20-July-01

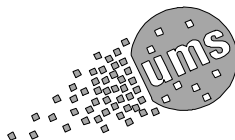
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Specifications subject to change without notice

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Ordering Information

Chip form : CHR2292-99F/00

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