### NE5020

### DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and  $\pm 0.1\%$  accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

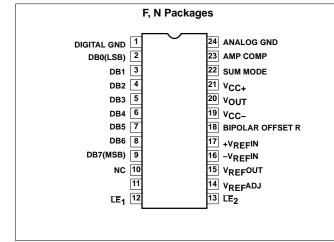
The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

### FEATURES

- 10-bit resolution
- Guaranteed monotonicity over operating range
- ±0.1% relative accuracy
- Unipolar (0V to +10V) and bipolar (± 5V) output range
- Logic bus compatible
- 5µs settling time

### PIN CONFIGURATION



### **APPLICATIONS**

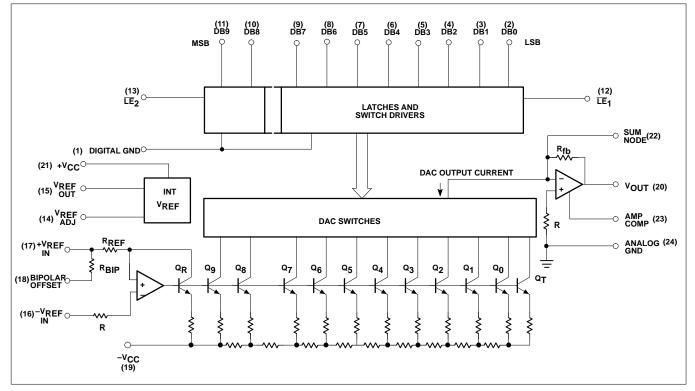
- Precision 10-bit D/A converters
- 10-bit analog-to-digital converters
- Programmable power supplies
- Test equipment
- Measurement instruments

### **ORDERING INFORMATION**

| DESCRIPTION                                  | TEMPERATURE RANGE | ORDER CODE | DWG # |
|--|-------------------|------------|-------|
| 24-Pin Ceramic Dual In-Line Package (CERDIP) | 0 to 70°C         | NE5020F    | 0588B |
| 24-Pin Plastic Dual In-Line Package (DIP)    | 0 to 70°C         | NE5020N    | 0412A |

### NE5020

### **BLOCK DIAGRAM**



### **ABSOLUTE MAXIMUM RATINGS**

| SYMBOL               | PARAMETER  | RATING                | UNIT |
|----------------------|--|-----------------------|------|
| V <sub>CC</sub> +    | Positive supply voltage  | 18                    | V    |
| V <sub>CC</sub> -    | Negative supply voltage  | -18                   | V    |
| V <sub>IN</sub>      | Logic input voltage  | 0 to 18               | V    |
| V <sub>REF IN</sub>  | Voltage at +V <sub>REF</sub> input                                       | 12                    | V    |
| V <sub>REF ADJ</sub> | Voltage at V <sub>REF</sub> adjust                                       | 0 to V <sub>REF</sub> | V    |
| V <sub>SUM</sub>     | Voltage at sum node  | 12                    | V    |
| IREFSC               | Short-circuit current to ground at V <sub>REF OUT</sub>                  | Continuous            |      |
| loutsc               | Short-circuit current to ground or either supply at $V_{OUT}$            | Continuous            |      |
| P <sub>D</sub>       | Maximum power dissipation T <sub>A</sub> =25°C, (still-air) <sup>1</sup> |                       |      |
|                      | F package  | 2150                  | mW   |
|                      | N package  | 2150                  | mW   |
| T <sub>A</sub>       | Operating temperature range NE5020                                       | 0 to +70              | °C   |
| T <sub>STG</sub>     | Storage temperature range  | -65 to +150           | °C   |
| T <sub>SOLD</sub>    | Lead soldering temperature<br>(10 sec. max)                              | 300                   | °C   |

NOTES:

1. Derate above 25°C at the following rates: F package at 17.2mW/°C N package at 17.2mW/°C

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### DC ELECTRICAL CHARACTERISTICS

 $V_{CC}\text{+=+15V}, \ V_{CC}\text{-=-15V}, \ 0 \leq T_A \leq 70^\circ C, \ \text{unless otherwise specified.}^1 \ \text{Typical values are specified at } 25^\circ C.$ 

| SYMBOL                                   | PARAMETER TEST CONDI                               | TEST CONDITIONS   | LIMITS        |             |                  |                     |
|--|--|---|---------------|-------------|------------------|---------------------|
|  |  | TEST CONDITIONS   | Min           | Тур         | Max              | UNIT                |
|  | Resolution<br>Monotonicity<br>Relative accuracy    |   |               |             | 10<br>10<br>±0.1 | Bits<br>Bits<br>%FS |
| V <sub>CC+</sub><br>V <sub>CC-</sub>     | Positive supply voltage<br>Negative supply voltage |   | 11.4<br>-11.4 | 15<br>-15   | 16.5<br>-16.5    | V<br>V              |
| V <sub>IN(1)</sub><br>V <sub>IN(0)</sub> | Logic "1" input voltage<br>Logic "0" input voltage | Pin 1=0V<br>Pin 1=0V  | 2.0           |             | 0.8              | V<br>V              |
| I <sub>IN(1)</sub><br>I <sub>IN(0)</sub> | Logic "1" input current<br>Logic "0" input current | Pin 1=0V, 2 <v<sub>IN&lt;18V<br/>Pin 1=0V, -5V<v<sub>IN&lt;0.8V</v<sub></v<sub>         |               | 0.1<br>-2.0 | 10<br>-10        | μΑ<br>μΑ            |
| V <sub>FS</sub>                          | Full-scale output                                  | Unipolar mode, V <sub>REF</sub> =5.000V, all bits high, $T_{\rm A}{=}25^{\circ}{\rm C}$ | 9.5           |             | 10.5             | V                   |
| +V <sub>FS</sub>                         | Full-scale output                                  | Bipolar mode, $V_{REF}$ =5.000V, all bits high, $T_A$ =25°C                             | 4.75          |             | 5.25             | V                   |
| -V <sub>FS</sub>                         | Negative full-scale                                | Bipolar mode, $V_{REF}$ =5.000V, all bits low, $T_A$ =25°C                              | -5.25         |             | -4.75            | V                   |

NOTES:

1. Refer to Figure 1.

### DC ELECTRICAL CHARACTERISTICS (Continued)

| 0)///201                      | DADAMETED   |   |     | LIMITS |      |              |  |
|-------------------------------|---|---|-----|--------|------|--------------|--|
| SYMBOL                        | PARAMETER   | TEST CONDITIONS   | Min | Тур    | Max  | UNIT         |  |
| V <sub>ZS</sub>               | Zero-scale output Unipolar mode, V <sub>REF</sub> =5.000V, all bits low, T <sub>A</sub> =25°C |   | -30 |        | +30  | mV           |  |
| I <sub>OS</sub>               | Output short-circuit current  | T <sub>A</sub> =25°C<br>V <sub>OUT</sub> =0V                      |     | ±15    | ±40  | mA           |  |
| PSR+ <sub>(OUT)</sub>         | Output power supply rejection (+)   | V-=-15V, 13.5V≤V+≤16.5V, external<br>V <sub>REF IN</sub> =5.000V  |     | 0.001  | 0.01 | %FS/<br>%VS  |  |
| PSR- <sub>(OUT)</sub>         | Output power supply rejection (-)   | V+=15V, -13.5V≤V-≤-16.5V, external<br>V <sub>REF IN</sub> =5.000V |     | 0.001  | 0.01 | %FS/<br>%VS  |  |
| TC <sub>FS</sub>              | Full-scale temperature coefficient  | V <sub>REF IN</sub> =5.000V                                       |     | 20     |      | ppmFS<br>/°C |  |
| TC <sub>ZS</sub>              | Zero-scale temperature coefficient  |   |     | 5      |      | ppmFS/°C     |  |
| I <sub>REF</sub> <sup>2</sup> | Reference output current  |   |     |        | 3    | mA           |  |
| IREF SC                       | Reference short circuit current   | T <sub>A</sub> =25°C<br>V <sub>REF OUT</sub> =0V                  |     | 15     | 30   | mA           |  |
| PSR+ <sub>REF</sub>           | Reference power supply rejection (+)  | V-=-15V, 13.5V≤V+≤16.5V, I <sub>REF</sub> =1.0mA                  |     | .003   | .01  | %VR/<br>%VS  |  |
| PSR- <sub>REF</sub>           | Reference power supply rejection (-)  | V <b>+=</b> 15V, -13.5V≤V-≤16.5V,                                 |     | .003   | .01  | %VR/<br>%VS  |  |
| V <sub>REF</sub>              | Reference voltage   | I <sub>REF</sub> =1.0mA, T <sub>A</sub> =25°C                     | 4.9 | 5.0    | 5.25 | V            |  |
| TC <sub>REF</sub>             | Reference voltage temperature co-<br>efficient  | I <sub>REF</sub> =1.0mA   |     | 60     |      | ppm/°C       |  |
| Z <sub>IN</sub>               | DAC V <sub>REF IN</sub> input impedance   | I <sub>REF</sub> =1.0mA   |     | 5.0    |      | kΩ           |  |
| I <sub>CC</sub> +             | Positive supply current   | V <sub>CC</sub> +=15V   |     | 7      | 14   | mA           |  |
| I <sub>CC</sub> -             | Negative supply current   | V <sub>CC</sub> -=-15V  |     | -10    | -15  | mA           |  |
| P <sub>D</sub>                | Power dissipation   | I <sub>REF</sub> =1.0mA, V <sub>CC</sub> =±15V                    |     | 255    | 435  | mW           |  |

NOTES:

1. Refer to Figure 1.

2. For I<sub>REF OUT</sub> greater than 3mA, an external buffer is required.

### AC ELECTRICAL CHARACTERISTICS<sup>1</sup>

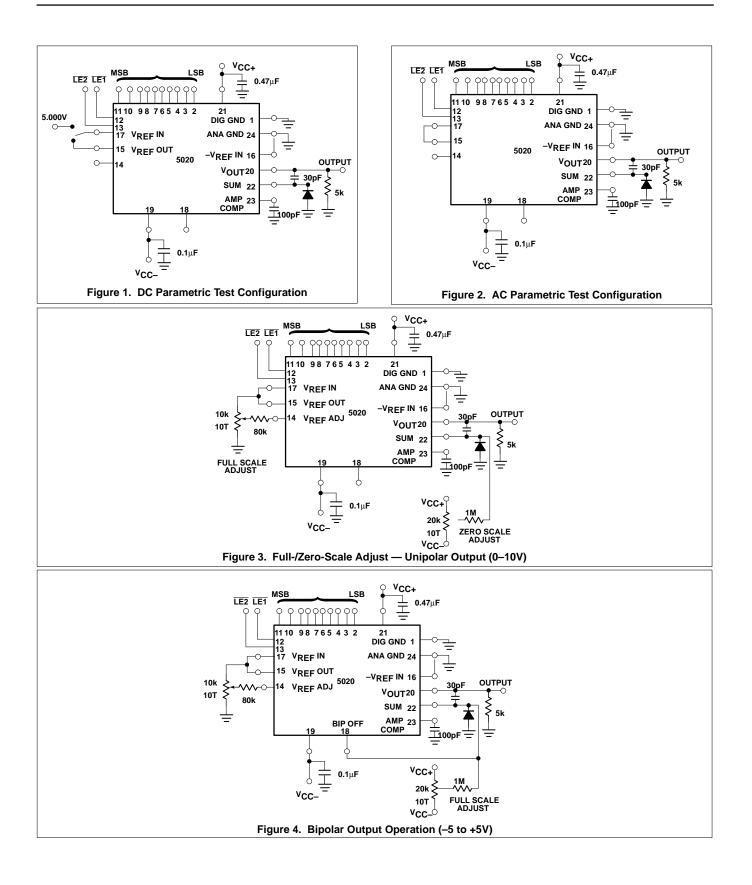
 $V_{CC} = +15V, T_A = 25^{\circ}C.$ 

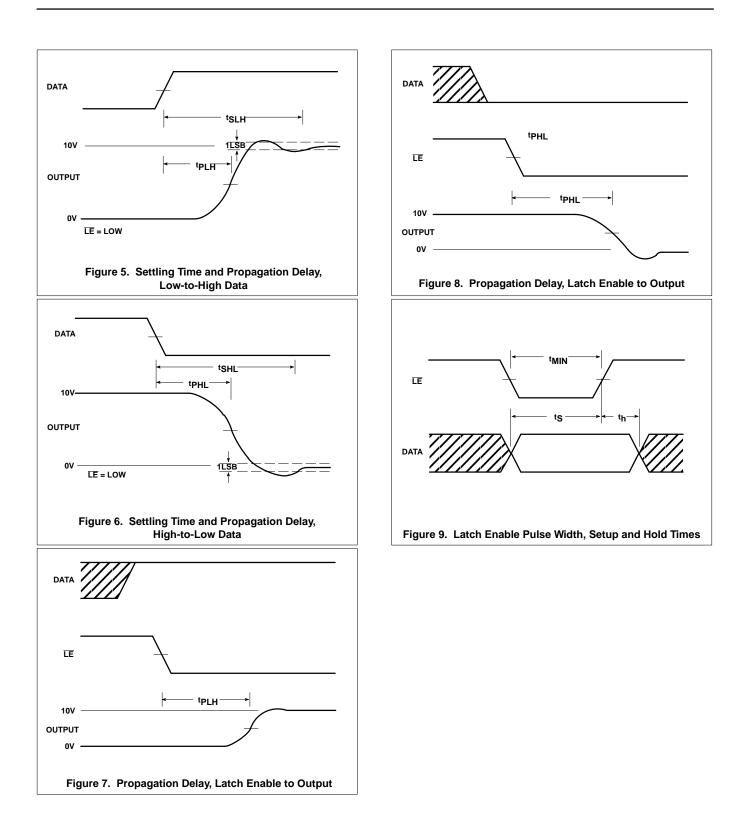
| SYMBOL            | PARAMETER                | то      | FROM          | FROM TEST CONDITIONS                       | LIMITS |     |     | UNIT |
|-------------------|--------------------------|---------|---------------|--|--------|-----|-----|------|
| STWIDOL           | FARAMETER                | 10      | TO FROM TESTC | TEST CONDITIONS                            | Min    | Тур | Max | UNIT |
| t <sub>SLH</sub>  | Settling time            | ±1/2LSB | Input         | All bits low-to-high <sup>2</sup>          |        | 5   |     | μs   |
| t <sub>SHL</sub>  | Settling time            | ±1/2LSB | Input         | All bits high-to-low <sup>3</sup>          |        | 5   |     | μs   |
| t <sub>PLH</sub>  | Propagation delay        | Output  | Input         | All bits switched low-to-high <sup>2</sup> |        | 30  |     | ns   |
| t <sub>PHL</sub>  | Propagation delay        | Output  | Input         | All bits switched high-to-low <sup>3</sup> |        | 150 |     | ns   |
| t <sub>PLSB</sub> | Propagation delay        | Output  | Input         | 1 LSB change <sup>2,3</sup>                |        | 150 |     | ns   |
| t <sub>PLH</sub>  | Propagation delay        | Output  | ΤĒ            | Low-to-high transition <sup>4</sup>        |        | 300 |     | ns   |
| t <sub>PHL</sub>  | Propagation delay        | Output  | ΤĒ            | High-to-low transition <sup>5</sup>        |        | 150 |     | ns   |
| t <sub>S</sub>    | Set-up time              | ΤĒ      | Input         | 1,6  | 100    |     |     | ns   |
| t <sub>H</sub>    | Hold time                | Input   | ΤĒ            | 1,6  | 50     |     |     | ns   |
| t <sub>PW</sub>   | Latch enable pulse width |         |               | 1,6  | 150    |     |     | ns   |

NOTES:

Refer to Figure 2.
See Figure 5.
See Figure 6.
See Figure 7.
See Figure 8.
See Figure 9.

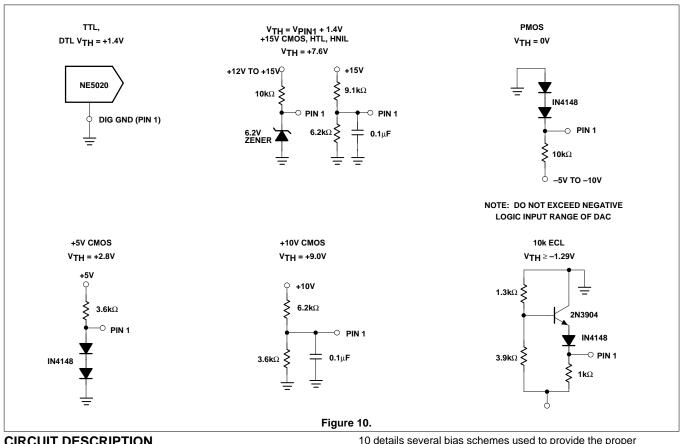
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## 10-Bit µP-compatible D/A converter



### **CIRCUIT DESCRIPTION**

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

### Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ( $\overline{LE}_1$  and  $\overline{LE}_2$ ) and ten data input latches. LE2 controls the two most significant bits of data (DB9 and DB8) while  $\overline{LE}_1$  controls the eight lesser significant bits (DB<sub>7</sub> through DB<sub>0</sub>). Both the latch enable ports ( $\overline{LE}$ ) and the data inputs are static- and threshold-sensitive. When the latch enable ports (LE) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the LE with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which LE goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring  $-2\mu$ A for low (0.8V max) or 0.1 $\mu$ A for high (2.0V min) when the LE is high. Any changes on the data bus with LE high will have no effect on the DAC output.

The digital logic inputs (LE and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure

10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

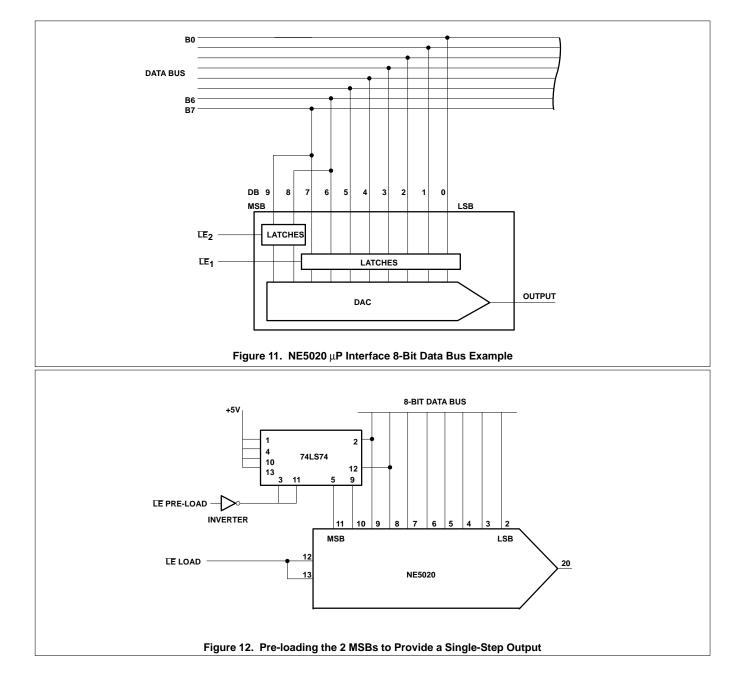
To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after LE is changed to a high state.

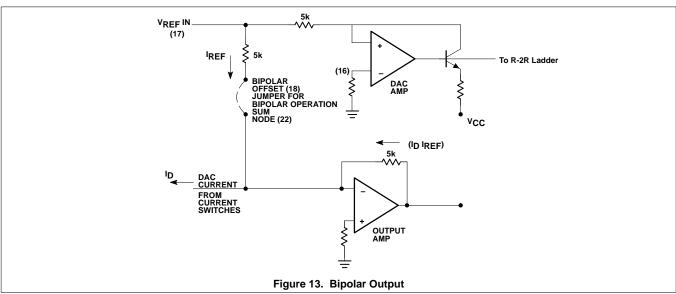
The independent  $\overline{LE}$  ( $\overline{LE}_1$  and  $\overline{LE}_2$ ) lines allow for direct interface from an 8-bit bus (see Figure 11). Data for the two MSBs is supplied and stored when  $\overline{LE}_2$  is activated low and returned high according to the NE5020 timing requirements. Then  $\overline{LE}_1$  is activated low and the remaining eight LSBs of data are transferred into the DAC. With  $\overline{\text{LE}}_1$  returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to pre-load the two MSB data values. Figure 12 shows the circuit configuration.

After pre-loading (via LE pre-load) the external latch with the two MSB values,  $\overline{LE}_2$  is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.





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### **Reference Interface**

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a V<sub>REF ADJ</sub> (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V<sub>REF</sub> adjustment, but also full-scale output adjust. Notice that the V<sub>REF ADJ</sub> pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the V<sub>REF</sub> ADJ pin and observing good layout

#### practices.

The V<sub>REF OUT</sub> node can drive loads greater than the DAC V<sub>REF</sub> input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

### **Input Amplifier**

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through QR with a 5V V<sub>REF</sub>. This current sets the input bias to the ladder network. Data bit 9 (DB9)(Q9), when turned on, will mirror this current and will contribute 1mA to the output. DB8 (Q8) will contribute 1/2 of that value or 0.5mA, and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

| оит = | $\frac{2 V_{REF}}{R_{REF}}  \left( \frac{DB9}{2} \; + \; \frac{DB8}{4} \; + \; \frac{DB7}{8} \; + \right. \\$ |  |
|-------|---|--|
|       | $\frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} +$  |  |
|       | $\frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024} \right)$  |  |

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/ $\mu$ s and source impedance at the V<sub>REF INPUT</sub> greater than 5k $\Omega$  should be avoided to maintain stability.

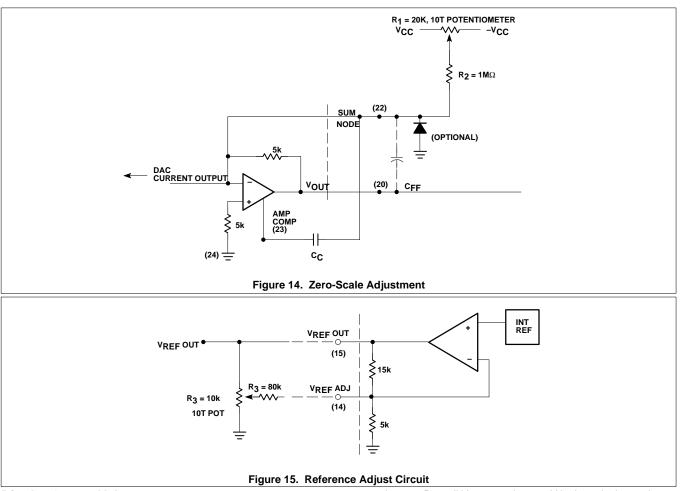
The  $-V_{REF\ INPUT}$  pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode  $+V_{REF\ INPUT}$  is grounded and the negative reference is tied directly to the  $-V_{REF\ INPUT}$  contains a 5k $\Omega$  resistor that matches a like resistor in the  $+V_{REF}$  INPUT to reduce voltage offset caused by op amp input bias currents.

#### **Output Amplifier and Interface**

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/µs and settle to within ±1/2LSB in 5µs. These times are typical when driving the rated loads of  $R_L \ge 5k$  and  $C_L$  50pF with recommended values of  $C_{FF}$  = 1nF and  $C_{FB}$  = 30pF. Typical input offset voltages of 5mV and 50k $\Omega$  open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip  $R_{FB}$  resistor.  $R_{FB}$  is matched to  $R_{REF}$  and  $R_{BIP}$  to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition  $I_{OUT}$  will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

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### **Bipolar Output Voltage**

The NE5020 includes a thermally matched resistor, R<sub>BIP</sub>, to offset the output voltage by 5V to obtain –5V to +5V output voltage range operation. This is accomplished by shorting Pins 18 and 22 (see Figure 13). This connection produces a current equal to (V<sub>REFIN</sub> – SUM NODE) ÷ R<sub>BIP</sub> (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA – 1mA)5k $\Omega$  = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and V<sub>OUT</sub> = –(5k $\Omega$ ) (1mA) = –5V. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim V<sub>OUT</sub> = 0.00 with the MSB high or V<sub>OUT</sub> = –5.0V with all bits off.

### Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is

shown in Figure 14. The trim is the result of injecting a current from resistor  $\mathsf{R}_2$  that counteracts the error current. Adjusting

potentiometer  $\rm R_1$  until  $\rm V_{OUT}$  equals 0.000V in the unipolar mode or -5.000V in the bipolar mode (see bipolar section accomplishes this trim.

#### **Full-Scale Adjustment**

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer  $R_3$  is adjusted until  $V_{OUT}$  equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R<sub>REF</sub>, R<sub>FB</sub>, and R<sub>BIP</sub> shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than  $\pm 0.3\%$  which implies that typical full-scale (or gain) error is less than  $\pm 0.3\%$  of ideal full-scale value.