

**M62364****CMOS IC****8-BIT 8-CH MULTIPLYING
D-A CONVERTER WITH
BUFFER AMPLIFIERS****■ DESCRIPTION**

The UTC **M62364** is a CMOS 8-bit, 8-ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (D_{IN}, CLK, LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0mA or more and can operate in a whole supply range from V_{DD} to GND.

The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal Do for a cascading connection.

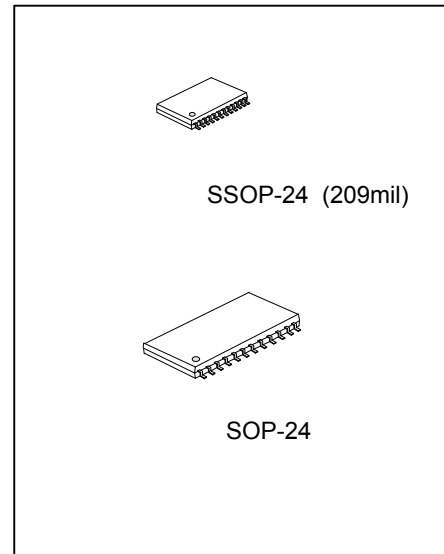
■ FEATURES

- *Three-wiring serial data transmission
- *Doubled precision 8-ch D/A converter employing an R-2R with higher-order segment method
- *8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- *4-quadrant multiplication

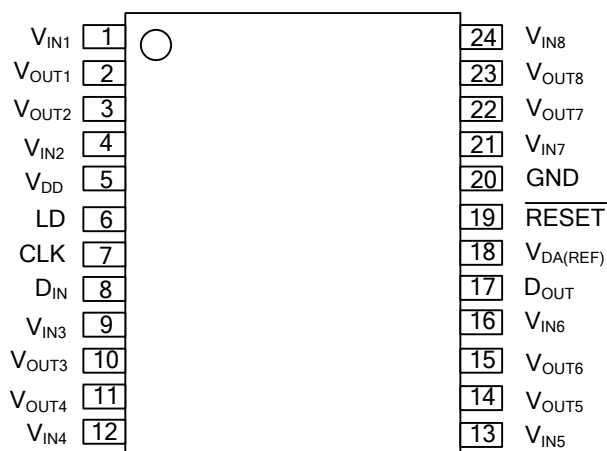
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
M62364L-R24-R	M62364G-R24-R	SSOP-24	Tape Reel
M62364L-R24-T	M62364G-R24-T	SSOP-24	Tube
M62364L-S24-R	M62364G-S24-R	SOP-24	Tape Reel
M62364L-S24-T	M62364G-S24-T	SOP-24	Tube

	(1) R: Tape Reel, T: Tube (2) R24: SSOP-24, S24: SOP-24 (5) G: Halogen Free, L: Lead Free
--	--



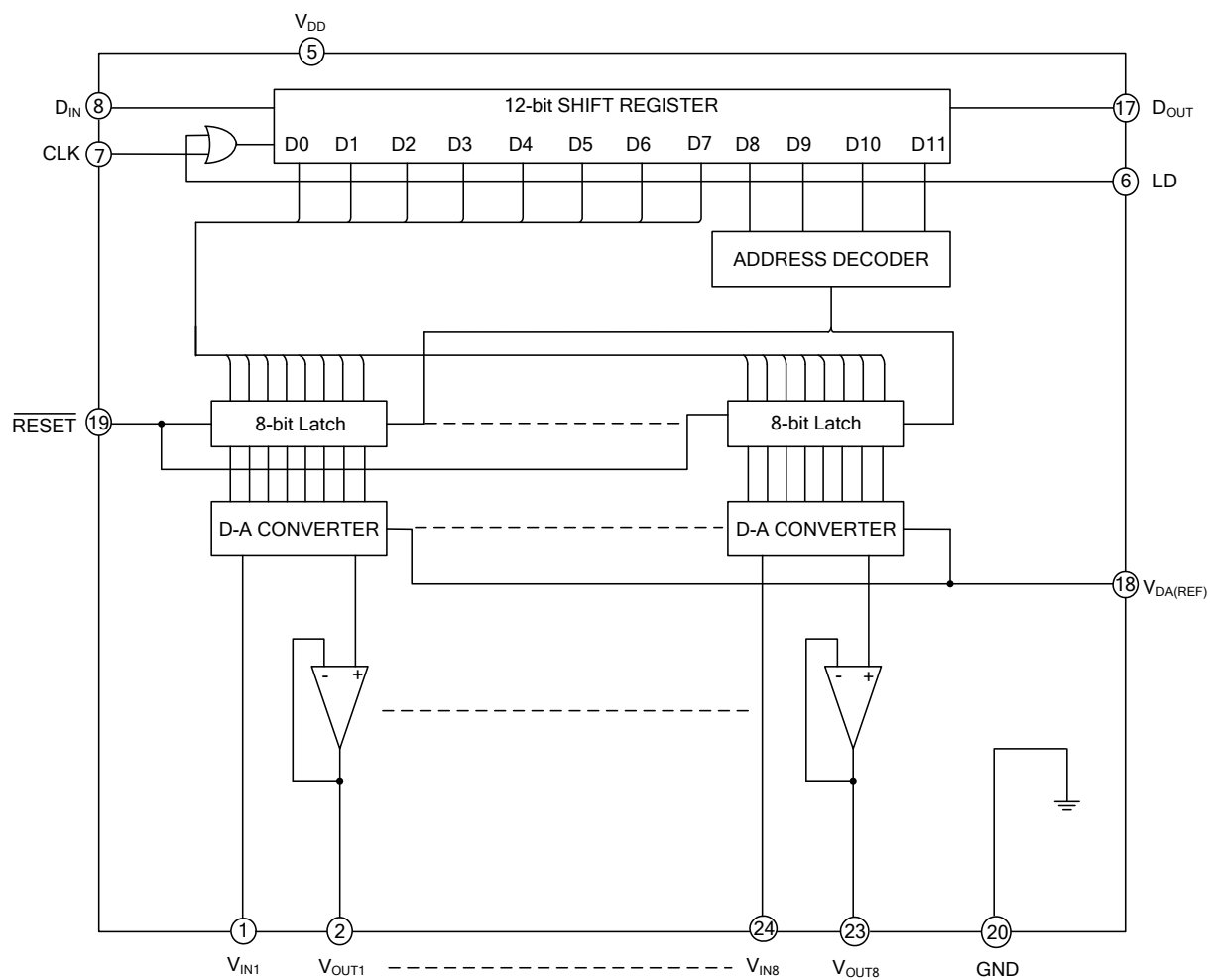
■ PIN CONFIGURATION (TOP VIEW)



■ EXPLANATION OF TERMINALS

PIN NO	SYMBOL	FUNCTION
8	D _{IN}	Serial data input
17	D _{OUT}	Serial data output
7	CLK	Shift clock input. Input data of D _{IN} are taken into the 12-bit shift register on a rising edge of the clock
6	LD	A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register
19	RESET	Reset 8-bit latches
2	V _{OUT1}	D/A Converter Output with 8-bit resolution
3	V _{OUT2}	
10	V _{OUT3}	
11	V _{OUT4}	
14	V _{OUT5}	
15	V _{OUT6}	
22	V _{OUT7}	
23	V _{OUT8}	
5	V _{DD}	Power Supply
20	GND	Ground
1	V _{IN1}	D/A Converter Input
4	V _{IN2}	
9	V _{IN3}	
12	V _{IN4}	
13	V _{IN5}	
16	V _{IN6}	
21	V _{IN7}	
24	V _{IN8}	
18	V _{DA(REF)}	D/A Converter Reference Voltage Input

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Digital Input Voltage	V_{IND}	-0.3 ~ +7.0	V
Analog Input Voltage	V_{IN}	-0.3 ~ $V_{DD}+0.3$	V
Analog Output Voltage	V_{OUT}	-0.3 ~ $V_{DD}+0.3$	V
D-A Reference Voltage	$V_{DA(REF)}$	-0.3 ~ $V_{DD}+0.3$	V
Operating Temperature	T_{OPR}	-20 ~ +75	°C
Storage Temperature	T_{STG}	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

($V_{DD}=5V\pm10\%$, $V_{DD}\geq V_{IN}$, GND, $V_{DA(REF)}=0V$, $T_A=-20\sim85^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
ANA/DIG COMMON PART						
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Current	I_{DD}	CLK=1MHz, $V_{CC}=3V$, $I_{AO}=0\mu A$			3.5	mA
Digital Part						
Digital Input "Low" Voltage	I_{IL}				0.2 V_{DD}	V
Digital Input "High" Voltage	I_{IH}		0.8 V_{DD}			V
DOUT Terminal Output "Low" Voltage	V_{OL}	$I_{OL}=2.5mA$			0.4	V
DOUT Terminal Output "High" Voltage	V_{OH}	$I_{OH}=-400\mu A$	$V_{DD}-0.4$			V
Input Leak Current	I_{ILK}	$V_{IN}=0\sim V_{DD}$	-10		10	μA
ANALOG PART						
Buffer Amplifier Output Voltage Range	V_{AO}	$I_{AO}=\pm100\mu A$	0.1		$V_{CC}-0.1$	V
		$I_{AO}=\pm500\mu A$	0.2		$V_{CC}-0.2$	
Input Current	I_{IN}	$V_{IN}=3V$, $V_{DA(REF)}=0V$, * Proportional to max. input current condition ($V_{IN}-V_{DA(REF)}$) and digital data of each channels.			0.18	mA
D-A Reference Input Current	$I_{DA(REF)}$	$V_{IN}=3V$, $V_{DA(REF)}=0V$, * Proportional to max. input current condition ($V_{IN}-V_{DA(REF)}$) and digital data of each channels	-1.44			mA
Buffer Amplifier Output Current Range	I_{AO}	Upper Saturation Voltage=0.4V Lower Saturation Voltage=0.4V	-1		1	mA
Buffer Amplifier Output Impedance	R_O			5		Ω
Resolution	RES	$V_{DD}=2.61V$, $V_{DA(REF)}=0.050V$		8		bit
Differential Nonlinearity	DNL	(10mV/1LSB)	-1		1	LSB
Nonlinearity	NL	Without Load($I_{AO}=\pm0$)	-1.5		1.5	LSB
Output Capacitive Load	C_O				0.1	μF

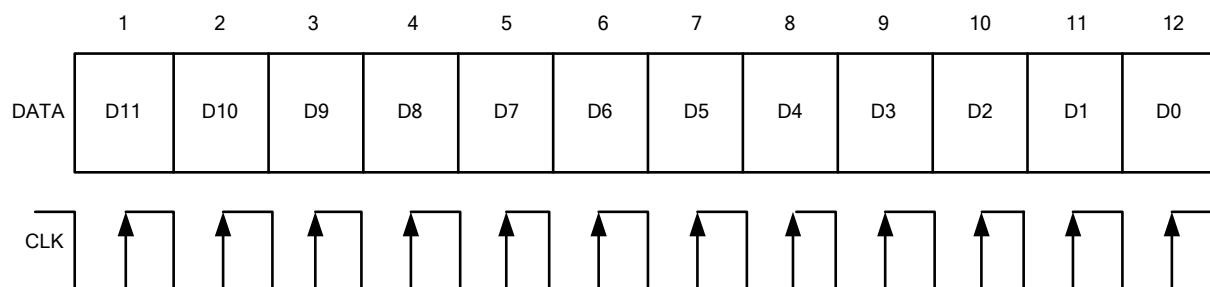
■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS						
Clock "L" Pulse Width	t_{CKL}		200			ns
Clock "H" Pulse Width	t_{CKH}		200			ns
Clock Rise Time	t_{CR}				200	ns
Clock Fall Time	t_{CF}					
Data Set Up Time	t_{DCH}		60			ns
Data Hold Time	t_{CHD}		100			ns
LD Set Up Time	t_{CHL}		200			ns
LD Hold Time	t_{LDC}		100			ns
LD "H" Pulse Duration Time	t_{LDH}		100			ns
Data Output Delay Time	t_{DOUT}	$C_L=100pF$	70		350	ns
D-A Output Setting Time	t_{LDD}	$C_L \leq 100pF, V_{AO} : 0.1 \leq V_{AO} \leq 2.6V$ This Time Until The Output Becomes The final Value Of 1/2 LSB			300	μs

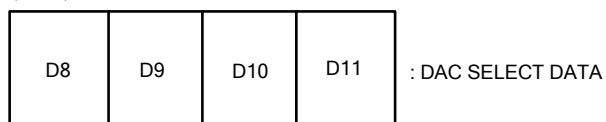
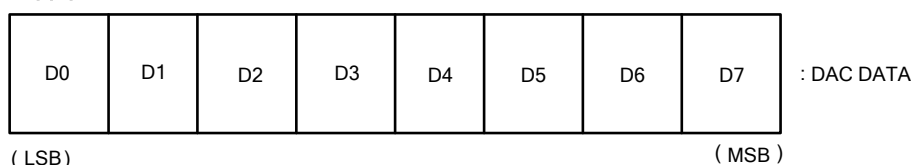
■ DIGITAL FORMAT

12 BIT SERIAL DATA

(LSB)



DATA ASSIGNMENT



Dac Select Data

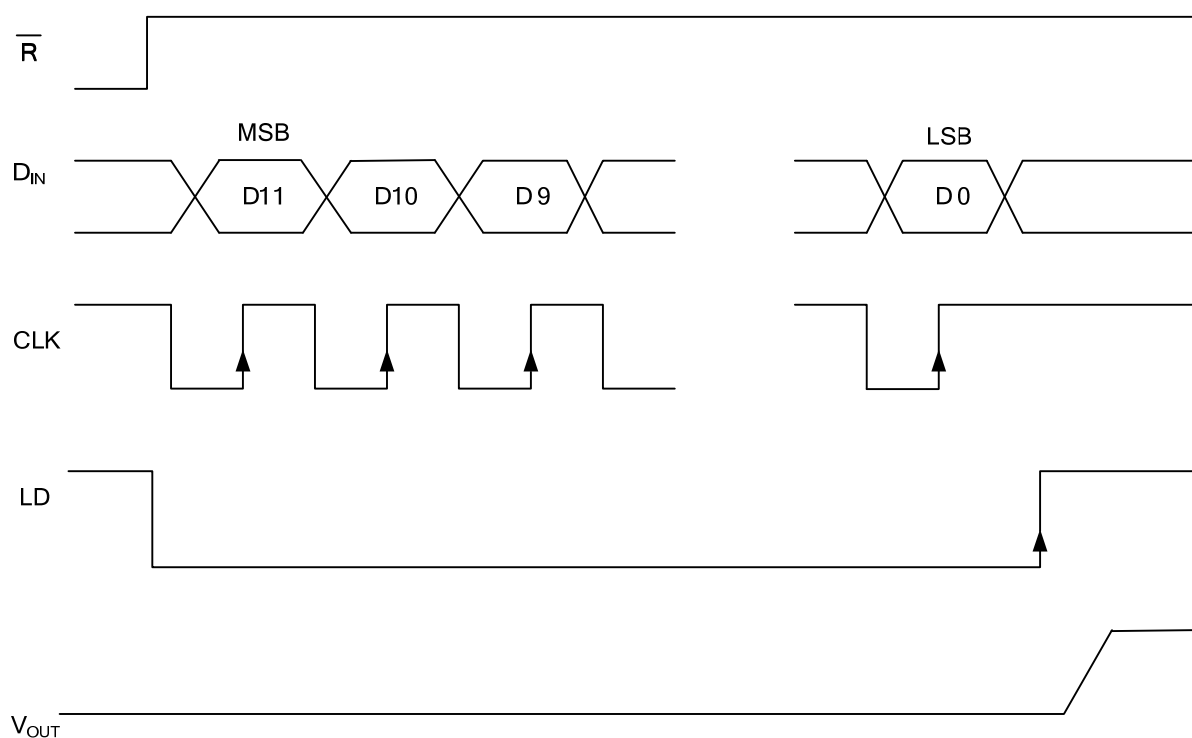
D8	D9	D10	D11	Dac Selection
0	0	0	0	Don't Care
0	0	0	1	V _{OUT1} Selection
0	0	1	0	V _{OUT2} Selection
0	0	1	1	V _{OUT3} Selection
0	1	0	0	V _{OUT4} Selection
0	1	0	1	V _{OUT5} Selection
0	1	1	0	V _{OUT6} Selection
0	1	1	1	V _{OUT7} Selection
1	0	0	0	V _{OUT8} Selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

■ DIGITAL FORMAT(Cont.)

Digital Data Format

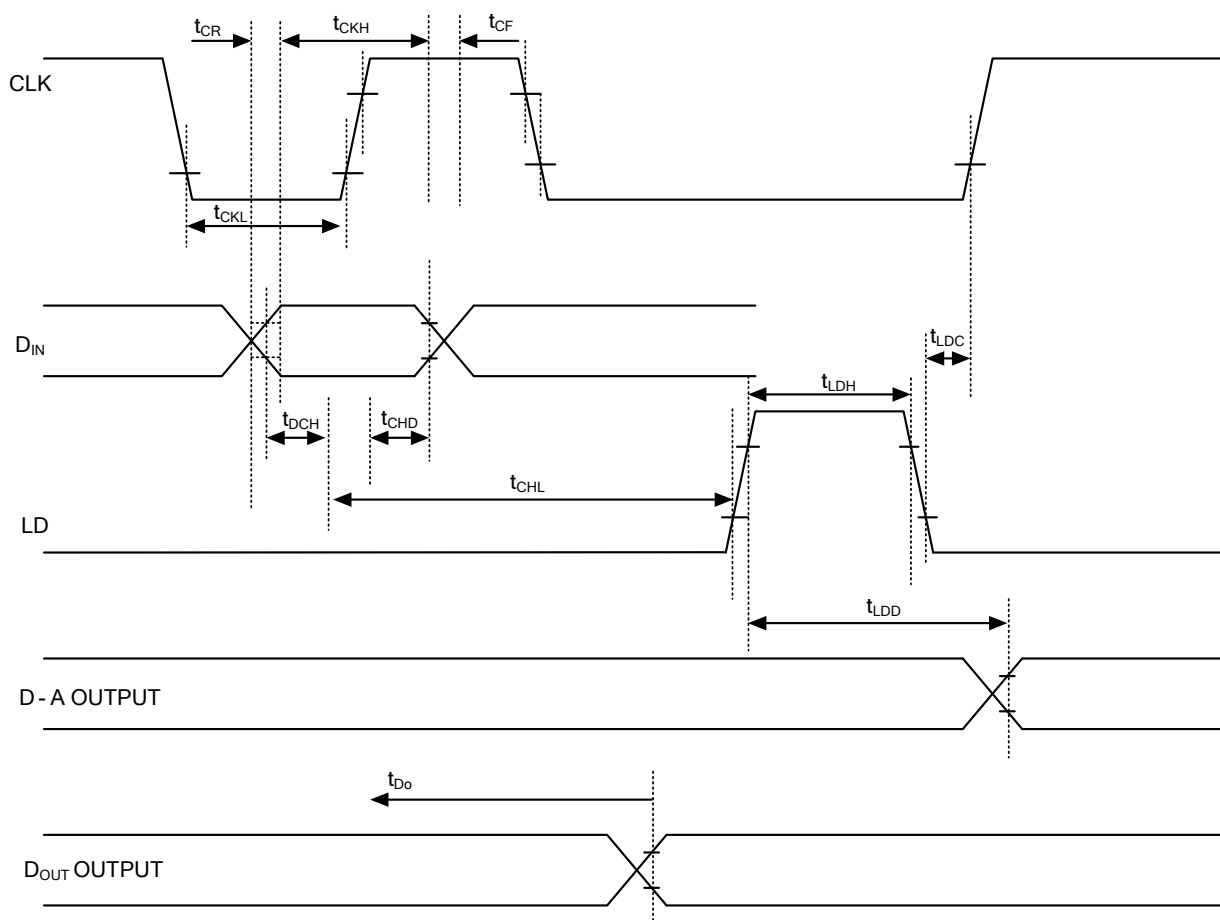
D0	D1	D2	D3	D4	D5	D6	D7	DAC OUTPUT
0	0	0	0	0	0	0	0	$V_{DA(REF)}$
1	0	0	0	0	0	0	0	$(V_{IN}-V_{DA(REF)})/256 \times 1 + V_{DA(REF)}$
0	1	0	0	0	0	0	0	$(V_{IN}-V_{DA(REF)})/256 \times 2 + V_{DA(REF)}$
1	1	0	0	0	0	0	0	$(V_{IN}-V_{DA(REF)})/256 \times 3 + V_{DA(REF)}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	1	1	$(V_{IN}-V_{DA(REF)})/256 \times 255 + V_{DA(REF)}$

■ TIMING CHART



* Input data carried out LD signal Low besides CLK signal positive edge.
CLK, LD is keep generally HIGH level.

■ TIMING CHART(Cont.)



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.