

FEATURES

- Wide V_{CC} operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
 - $V_{CC} = 3.0V$ Operation current : 31mA (Max.) at 55ns
2mA (Max.) at 1MHz
Standby current : 4/8uA (Max.) at 70/85°C
 - $V_{CC} = 5.0V$ Operation current : 76mA (Max.) at 55ns
10mA (Max.) at 1MHz
Standby current : 25/50uA (Max.) at 70/85°C
- High speed access time :
 - 55 55ns (Max.) at $V_{CC} : 3.0\sim 5.5V$
 - 70 70ns (Max.) at $V_{CC} : 2.7\sim 5.5V$
- Automatic power down when chip is deselected
- Easy expansion with CE1, CE2 and OE options
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V

DESCRIPTION

The BS62LV8001 is a high performance, very low power CMOS Static Random Access Memory organized as 1,048,576 by 8 bits and operates form a wide range of 2.4V to 5.5V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with maximum CMOS standby current of 8/50uA at $V_{CC}=3/5V$ at 85°C and maximum access time of 55/70ns.

Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), an active HIGH chip enable (CE2), and active LOW output enable ($\overline{OE}$) and three-state output drivers.

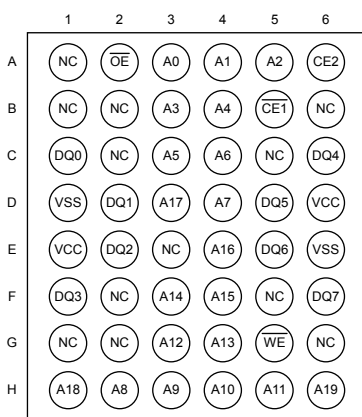
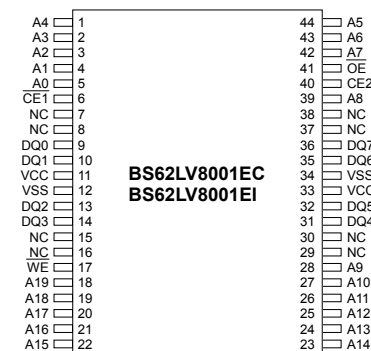
The BS62LV8001 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS62LV8001 is available in DICE form, JEDEC standard 44-pin TSOP II and 48-ball BGA package.

POWER CONSUMPTION

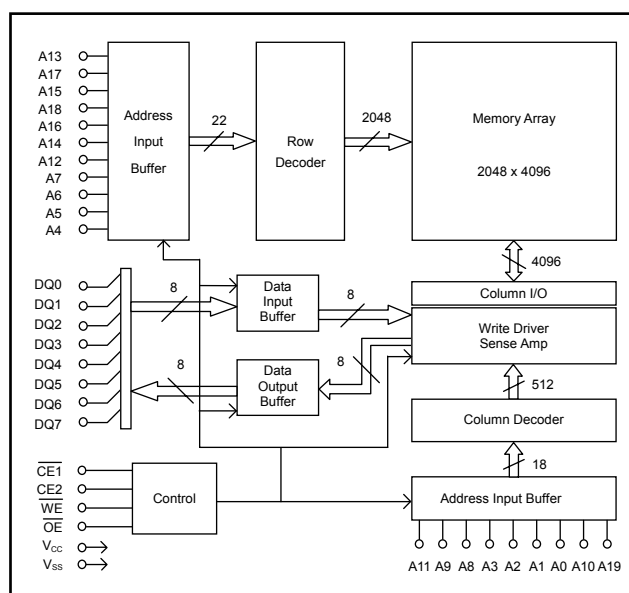
PRODUCT FAMILY	OPERATING TEMPERATURE	POWER DISSIPATION								PKG TYPE
		STANDBY (I _{CCSB1} , Max)		Operating (I _{CC} , Max)						
		V _{CC} =5.0V	V _{CC} =3.0V	V _{CC} =5.0V			V _{CC} =3.0V			
				1MHz	10MHz	f _{Max}	1MHz	10MHz	f _{Max}	
BS62LV8001DC	Commercial +0°C to +70°C	25uA	4.0uA	9mA	39mA	75mA	1.5mA	19mA	30mA	DICE
BS62LV8001EC										TSOP II-44
BS62LV8001FC										BGA-48-0912
BS62LV8001EI	Industrial -40°C to +85°C	50uA	8.0uA	10mA	40mA	76mA	2mA	20mA	31mA	TSOP II-44
BS62LV8001FI										BGA-48-0912

PIN CONFIGURATIONS



48-ball BGA top view

BLOCK DIAGRAM



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■ PIN DESCRIPTIONS

Name	Function
A0-A19 Address Input	These 20 address inputs select one of the 1,048,576 x 8-bit in the RAM
$\overline{\text{CE1}}$ Chip Enable 1 Input $\overline{\text{CE2}}$ Chip Enable 2 Input	$\overline{\text{CE1}}$ is active LOW and $\overline{\text{CE2}}$ is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{\text{WE}}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{\text{WE}}$ is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{\text{OE}}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{\text{OE}}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	There 8 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power Supply
V_{SS}	Ground

■ TRUTH TABLE

MODE	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O OPERATION	V _{CC} CURRENT
Not selected (Power Down)	H	X	X	X	High Z	I _{CCSB1} , I _{CCSB1}
	X	L	X	X		
Output Disabled	L	H	H	H	High Z	I _{CC}
Read	L	H	H	L	D _{OUT}	I _{CC}
Write	L	H	L	X	D _{IN}	I _{CC}

■ ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

SYMBOL	PARAMETER	RATING	UNITS
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 ⁽²⁾ to 7.0	V
T _{BIAS}	Temperature Under Bias	-40 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. -2.0V in case of AC pulse width less than 30 ns.

■ OPERATING RANGE

RANG	AMBIENT TEMPERATURE	V _{CC}
Commercial	0°C to + 70°C	2.4V ~ 5.5V
Industrial	-40°C to + 85°C	2.4V ~ 5.5V

■ CAPACITANCE ⁽¹⁾ (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNITS
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{IO}	Input/Output Capacitance	V _{I/O} = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V_{CC}	Power Supply		2.4	--	5.5	V
V_{IL}	Input Low Voltage		-0.5 ⁽²⁾	--	0.8	V
V_{IH}	Input High Voltage		2.2	--	$V_{CC}+0.3$ ⁽³⁾	V
I_{IL}	Input Leakage Current	$V_{IN} = 0\text{V to } V_{CC}$	--	--	1	μA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\text{V to } V_{CC}$, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, or $\overline{OE} = V_{IH}$	--	--	1	μA
V_{OL}	Output Low Voltage	$V_{CC} = \text{Max}$, $I_{OL} = 2.0\text{mA}$	--	--	0.4	V
V_{OH}	Output High Voltage	$V_{CC} = \text{Min}$, $I_{OH} = -1.0\text{mA}$	2.4	--	--	V
$I_{CC}^{(5)}$	Operating Power Supply Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $I_{DQ} = 0\text{mA}$, $f = F_{MAX}^{(4)}$	--	--	31	mA
					76	
I_{CC1}	Operating Power Supply Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $I_{DQ} = 0\text{mA}$, $f = 1\text{MHz}$	--	--	2	mA
					10	
I_{CCSB}	Standby Current – TTL	$\overline{CE1} = V_{IH}$, or $CE2 = V_{IL}$, $I_{DQ} = 0\text{mA}$	--	--	1.0	mA
					2.0	
$I_{CCSB1}^{(6)}$	Standby Current – CMOS	$\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	--	0.8	8.0	μA
				3.5	50	

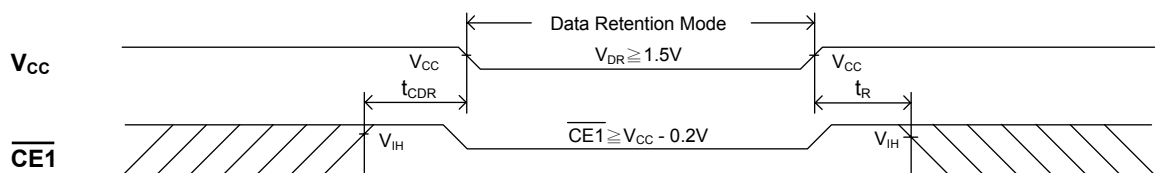
1. Typical characteristics are at $T_A=25^{\circ}\text{C}$ and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: $V_{CC}+1.0\text{V}$ in case of pulse width less than 20 ns.

4. $F_{MAX}=1/t_{RC}$.
5. $I_{CC}(\text{MAX.})$ is 30mA/75mA at $V_{CC}=3.0\text{V}/5.0\text{V}$ and $T_A=70^{\circ}\text{C}$.
6. $I_{CCSB1}(\text{MAX.})$ is 4.0 $\mu\text{A}/25\mu\text{A}$ at $V_{CC}=3.0\text{V}/5.0\text{V}$ and $T_A=70^{\circ}\text{C}$.

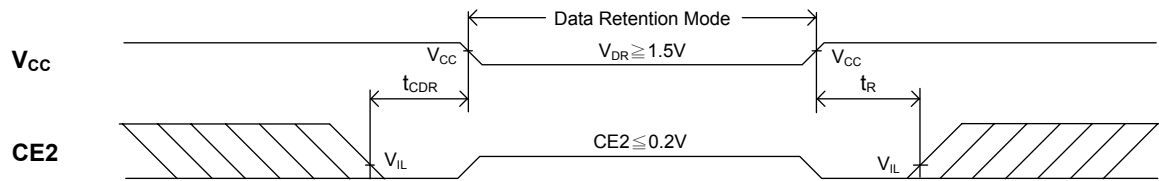
■ DATA RETENTION CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	1.5	--	--	V
$I_{CCDR}^{(3)}$	Data Retention Current	$\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	--	0.4	4.0	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		$t_{RC}^{(2)}$	--	--	ns

1. $V_{CC}=1.5\text{V}$, $T_A=25^{\circ}\text{C}$ and not 100% tested.
2. t_{RC} = Read Cycle Time.
3. $I_{CCDR}(\text{Max.})$ is 2.0 μA at $T_A=70^{\circ}\text{C}$.

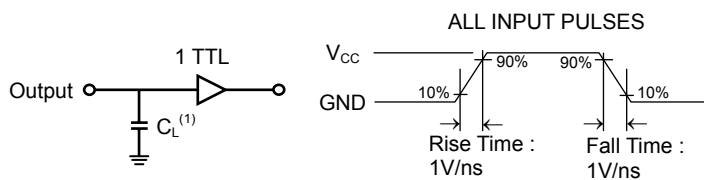
■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)


■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



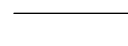
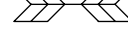
■ AC TEST CONDITIONS (Test Load and Input/Output Reference)

Input Pulse Levels	$V_{CC} / 0V$
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5 V_{CC}
Output Load	$t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}$
	$C_L = 5pF + 1TTL$
Output Load	Others
	$C_L = 30pF + 1TTL$



1. Including jig and scope capacitance.

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

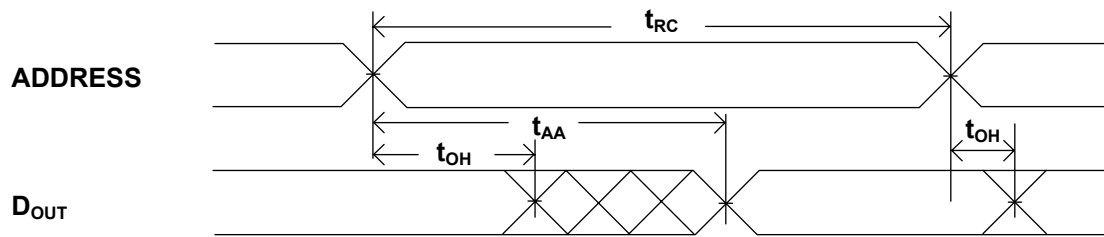
■ AC ELECTRICAL CHARACTERISTICS ($T_A = -40^{\circ}C$ to $+85^{\circ}C$)

READ CYCLE

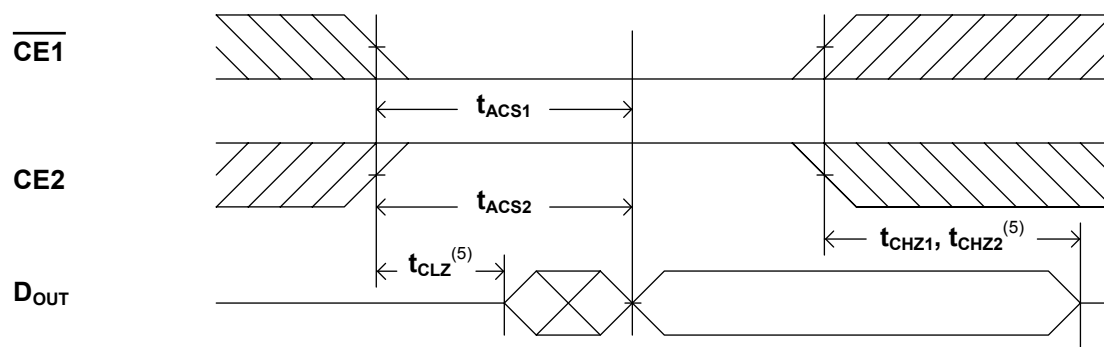
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns ($V_{CC} = 3.0 \sim 5.5V$)			CYCLE TIME : 70ns ($V_{CC} = 2.7 \sim 5.5V$)			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	70	--	--	ns
t_{AVQX}	t_{AA}	Address Access Time	--	--	55	--	--	70	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time (CE1)	--	--	55	--	--	70	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	55	--	--	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	25	--	--	30	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z (CE1)	10	--	--	10	--	--	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to Output Low Z (CE2)	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	10	--	--	10	--	--	ns
t_{E1HQZ}	t_{CHZ1}	Chip Select to Output High Z (CE1)	--	--	30	--	--	35	ns
t_{E2LQZ}	t_{CHZ2}	Chip Select to Output High Z (CE2)	--	--	30	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Enable to Output High Z	--	--	25	--	--	30	ns
t_{AVQX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

SWITCHING WAVEFORMS (READ CYCLE)

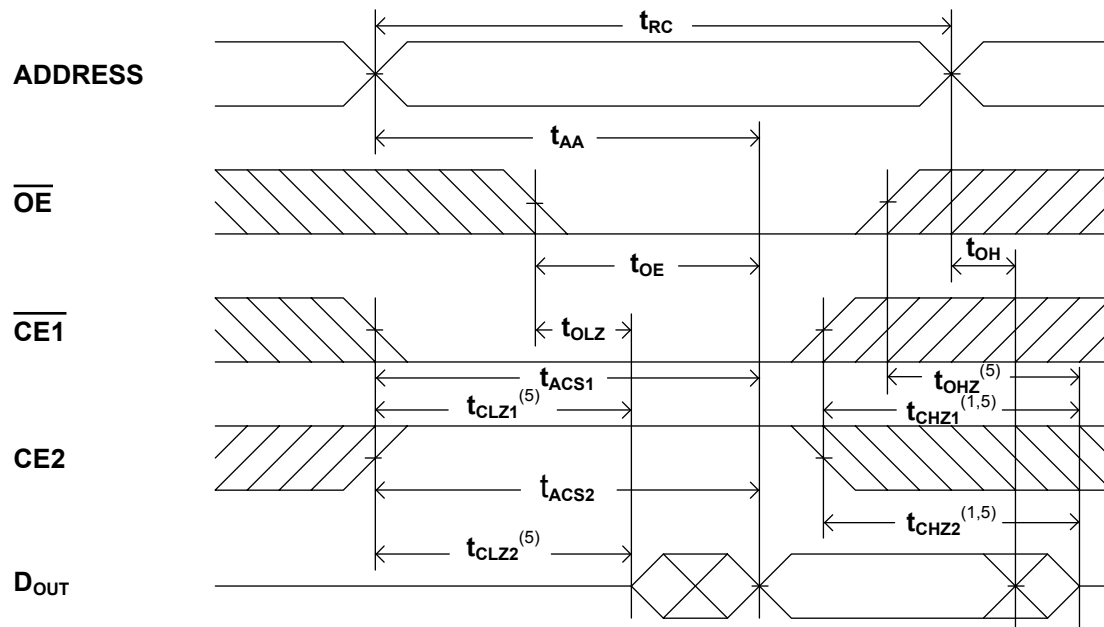
READ CYCLE 1 ^(1,2,4)



READ CYCLE 2 ^(1,3,4)



READ CYCLE 3 ^(1,4)



NOTES:

1. WE is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $\overline{CE2} = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or $\overline{CE2}$ transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$.
The parameter is guaranteed but not 100% tested.

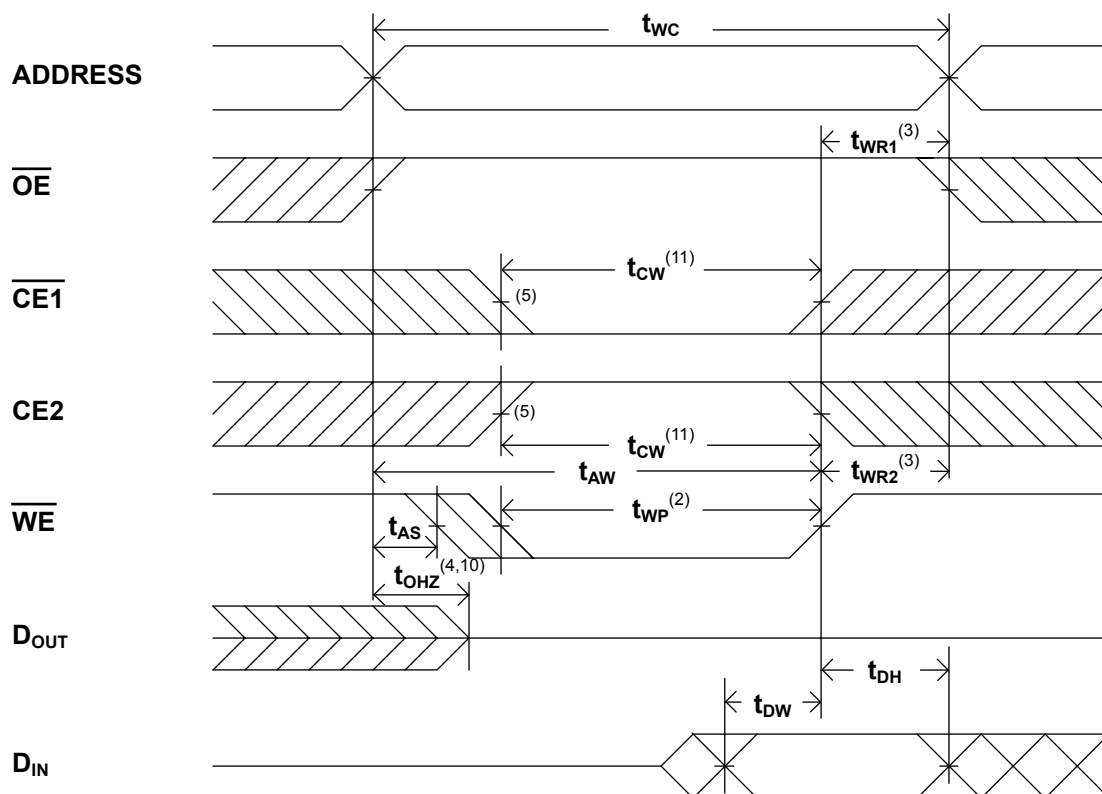
■ AC ELECTRICAL CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

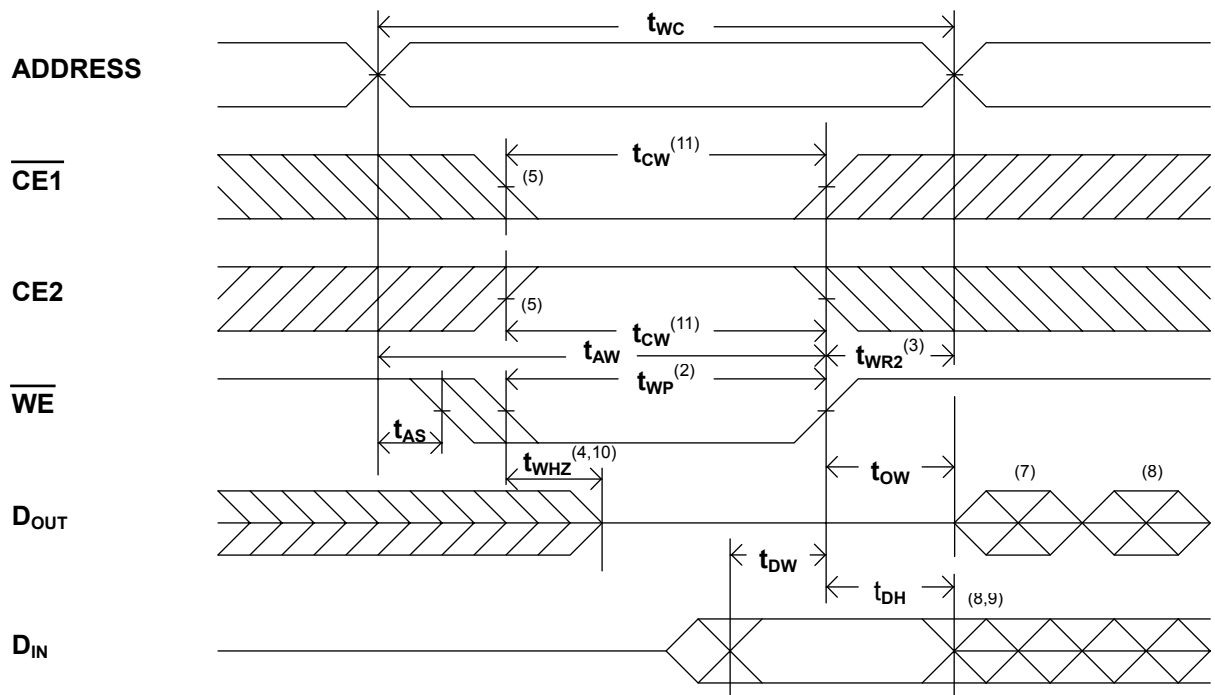
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns ($V_{CC} = 3.0\sim 5.5\text{V}$)			CYCLE TIME : 70ns ($V_{CC} = 2.7\sim 5.5\text{V}$)			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	70	--	--	ns
t_{AVWL}	t_{AS}	Chip Select to End of Write	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Set up Time	40	--	--	50	--	--	ns
t_{E1LWH}	t_{CW}	Address Valid to End of Write	40	--	--	50	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	30	--	--	35	--	--	ns
t_{WHAX}	t_{WR1}	Write Recovery Time ($\overline{CE1}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time ($\overline{CE2}$)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	25	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 ⁽¹⁾



WRITE CYCLE 2 ^(1,6)

NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{wr} is measured from the earlier of CE1 or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE1 low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$.
The parameter is guaranteed but not 100% tested.
11. t_{cw} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

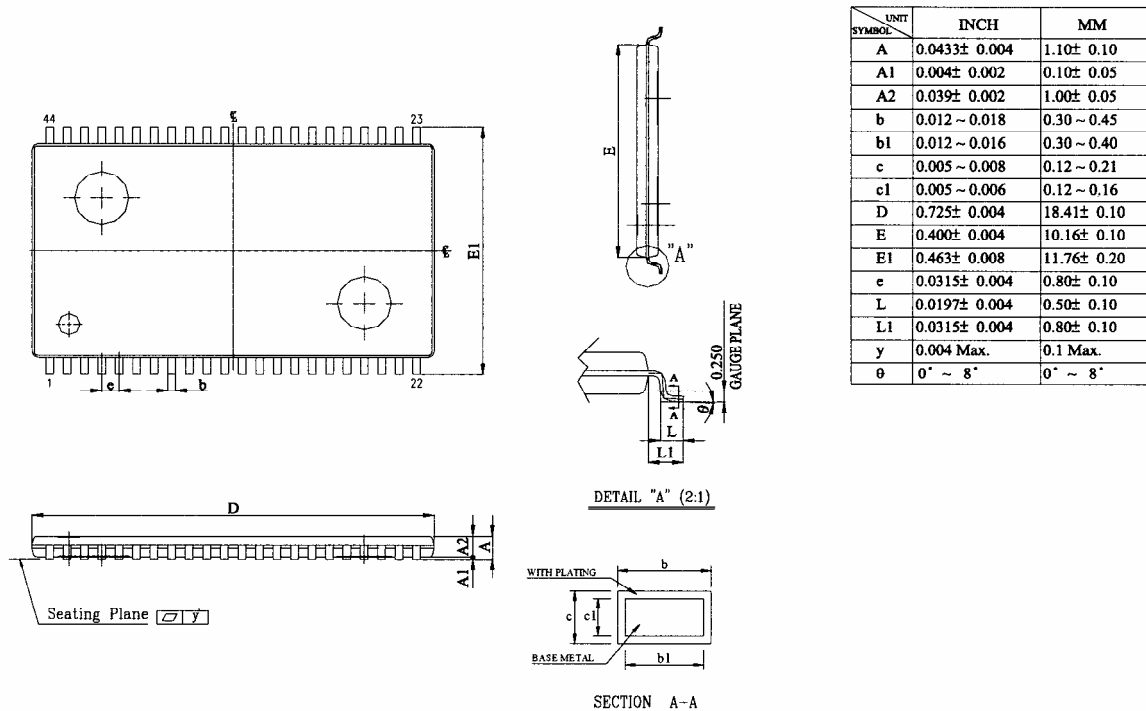
ORDERING INFORMATION

BS62LV8001	X	X	Z	YY	
					SPEED 55: 55ns 70: 70ns
					PKG MATERIAL G: Green, RoHS Compliant P: Pb free, RoHS Compliant
					GRADE C: +0°C ~ +70°C I: -40°C ~ +85°C
					PACKAGE D: DICE E: TSOP II-44 F: BGA-48-0912

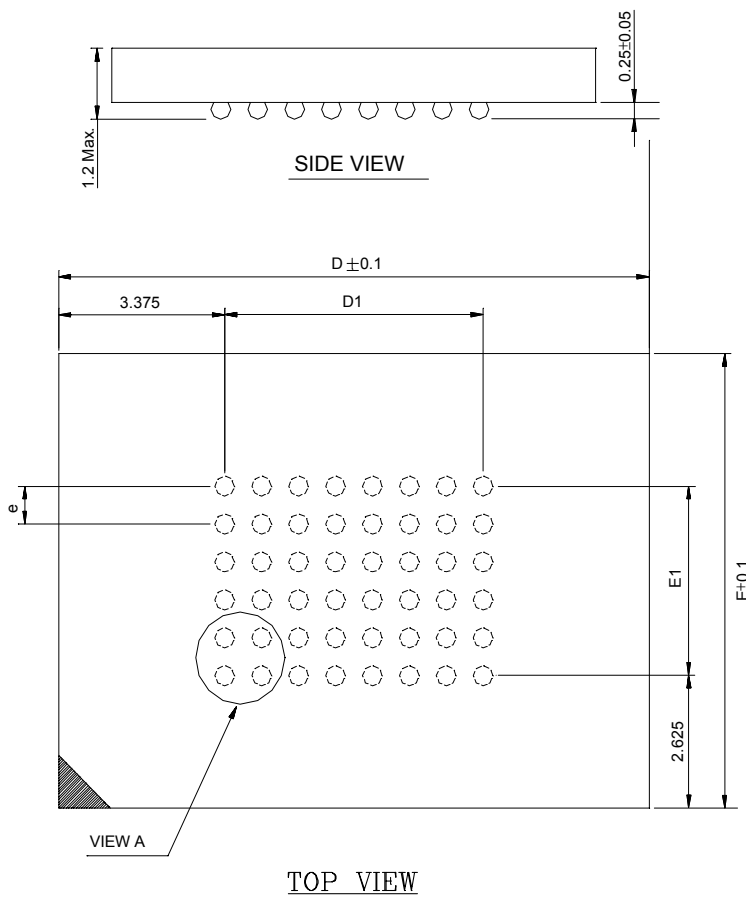
Note:

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PACKAGE DIMENSIONS

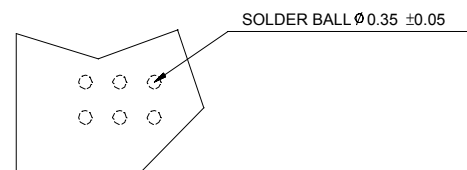


TSOP II-44

■ PACKAGE DIMENSIONS (continued)

NOTES:

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	12.0	9.0	5.25	3.75	0.75


VIEW A

TOP VIEW
48 mini-BGA (9mm x 12mm)

■ Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
2.2	Add lcc1 characteristic parameter Improve lccsb1 spec. I-grade from 110uA to 50uA at 5.0V 10uA to 8.0uA at 3.0V C-grade from 55uA to 25uA at 5.0V 5.0uA to 4.0uA at 3.0V	Jan. 13, 2006	
2.3	Change I-grade operation temperature range - from -25°C to -40°C Change lccdr spec. I-grade from 2.5uA to 4.0uA C-grade from 1.3uA to 2.0uA Typical from 0.8 to 0.4uA	May. 25, 2006	
2.4	Typical value of standby current is replaced by maximum value in Features and Description section Remove “-: Normal” (Leaded) PKG Material in ordering information	Oct. 31, 2008	