## M/A-COM

## Surface Mount Frequency Synthesizer CDMA 1720-1800 MHz

12 Lead Package

## Features

- Integrated VCO/PLL
- Miniature SMT Package
- Low Phase Noise
- +5 V Operation


## Description

The MLS9228-01760 synthesizer design integrates a high performance buffered VCO, PLL circuit and discrete loop filter in a surface mount package. The SMT packaging provides electrical shielding, easy PCB assembly and repeatable performance. The synthesizer is designed for use in PCS CDMA base stations and is optimised for coverage of the PCS band with 50 kHz step size and low phase noise and spurious.

M/A-COM synthesizers are manufactured in an ISO 9001 certified facility, incorporating surface mount assembly and automated electrical testing. This ensures consistent electrical performance and quality over volume production quantities.


Electrical Specifications ${ }^{1}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{cc}}=+5 \mathrm{~V}, \Delta \mathrm{~F}=50 \mathrm{kHz}, \mathrm{F}_{\mathrm{R}}=15 \mathrm{MHz}$ (unless otherwise stated)

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Range ( $\left.\mathrm{F}_{\text {OUT }}\right)^{2}$ | Over $\mathrm{T}_{\text {OP }}$ | MHz | 1720 | -- | 1800 |
| RF Output Power ( $\left.\mathrm{P}_{\text {out }}\right)^{3}$ | Over Top | dBm | -3.0 | - | +3.0 |
| Harmonic Output |  | dBc | - | -15 | -10 |
| Spurious Output | Phase comparison frequency ( $\left.\mathrm{F}_{\text {Out }} \pm \Delta \mathrm{F}\right)$ | dBc | -- | -75 | -60 |
|  | Reference breakthrough ( $\mathrm{F}_{\text {OUT }} \pm \mathrm{F}_{\mathrm{R}}$ ) | dBc | -- | -75 | -- |
| Phase Noise ${ }^{4}$ | SSB at 1 kHz offset from carrier | $\mathrm{dBc} / \mathrm{Hz}$ | - | -70 | -65 |
|  | SSB at 10 kHz offset from carrier | $\mathrm{dBc} / \mathrm{Hz}$ | - | -95 | -90 |
|  | SSB at 100 kHz offset from carrier | $\mathrm{dBc} / \mathrm{Hz}$ | -- | -115 | -110 |
|  | SSB at 1.25 MHz offset from carrier | $\mathrm{dBc} / \mathrm{Hz}$ | -- | -136 | -- |
| Integrated Phase Noise | 300 Hz to 3 kHz bandwidth | mrad rms | - | 26 | - |
| Frequency Switching Time ${ }^{5,6}$ | Over $\mathrm{F}_{\text {Out }}$, measured to within $\pm 500 \mathrm{~Hz}$ | ms | - | 35 | - |
| VCO Supply Current ( $\mathrm{ICC1}$ ) |  | mA | - | 19 | 21 |
| PLL Supply Current ( $\mathrm{I}_{\text {c2 } 2}$ ) |  | mA | - | 12 | 14 |
| VCO Supply Voltage ( $\mathrm{V}_{\mathrm{CC} 1}$ ) | Recommended operating limit | V | +4.75 | - | +5.25 |
| PLL Supply Voltage ( $\mathrm{V}_{\mathrm{C} 2}$ ) | Recommended operating limit | V | +4.75 | - | +5.25 |
| Step Size ( $\Delta \mathrm{F})^{7}$ | Recommended operating limit | kHz | -- | 50 | -- |
| Reference Frequency $\left(F_{\mathrm{R}}\right)^{8}$ | 0.5 to 2.0 Vpp sine wave into a.c. coupled CMOS. Recommended operating limit | MHz | 3 | - | 20 |

1. All specification limits are indicated values and apply over $\mathrm{F}_{\text {OUt }}$ and for $50 \Omega$ load impedance.
2. Programming control is 3 wire serial CMOS or TTL levels, in accordance with National Semiconductor LMX 2325.
3. Output power window includes variation over operating temperature range ( $\mathrm{T}_{\text {OP }}$ ) $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and output frequency range ( $\mathrm{F}_{\text {OUT }}$ ).
4. See plot for typical phase noise at other frequency offsets.
5. See plot for typical full band switching time measured to within other offsets from final frequency.
6. Integral PLL lock monitor output, TTL high locked, TTL low unlocked.
7. Device designed for loop bandwidth of 200 Hz .
8. Reference frequency input impedance $10 \mathrm{k} \Omega \mathrm{min}$.

## Functional Configuration

| Lead | Function | Lead | Function |
| :---: | :--- | :---: | :--- |
| 1 | Ground | 7 | Ground |
| 2 | Clock Input | 8 | Reference <br> Frequency Input |
| 3 | $\mathrm{~V}_{\mathrm{CC} 1}(\mathrm{VCO})$ | 9 | $\mathrm{~V}_{\mathrm{CC} 2}$ (PLL) |
| 4 | PLL Lock <br> Monitor Output | 10 | Data Input |
| 5 | RF Output | 11 | Strobe/Enable Input |
| 6 | Ground | 12 | Ground |

## Environmental Specifications

Devices are designed to function over the operating temperature range ( $\mathrm{T}_{\mathrm{OP}}$ ) of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and after exposure to the shock, vibration, thermal shock and moisture conditions typically encountered in base station and other infrastructure environments.

## Typical Performance



## Absolute Maximum Ratings ${ }^{1,2}$

| Parameter | Absolute Maximum |
| :--- | :--- |
| VCO Supply Voltage $\left(\mathrm{V}_{\mathrm{CC} 1}\right)^{3}$ | +6.5 V |
| PLL Supply Voltage $\left(\mathrm{V}_{\mathrm{CC} 2}\right)^{3}$ | +6.5 V |
| Reference Frequency Voltage | -0.3 V to +6.5 V |
| Data, Clock, Strobe Voltages | -0.3 V to +6.5 V |
| Storage Temperature $\left(\mathrm{T}_{\text {STOR }}\right)$ | $-45^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Solder Assembly Temperature | See App Note M2032 |

1. Exceeding these limits may cause permanent damage.
2. Static sensitive, observe appropriate handling precautions.
3. An external series resistor and bypass capacitor will allow operation at higher supply voltage and will improve power supply decoupling and noise suppression.

## Ordering Information

Synthesizers are available in either tape and reel or tube packaging. To order devices in tape and reel requires the suffix TR to be added to the part number, i.e. MLS9228-01760TR. Quantity 500 per 13 inch reel, see Application Note M2030.


Output Power vs Supply Voltage


## Reference Breakthrough Spurious



