

MOS INTEGRATED CIRCUIT $\mu PD444004L$

4M-BIT CMOS FAST SRAM 1M-WORD BY 4-BIT

Description

The μ PD444004L is a high speed, low power, 4,194,304 bits (1,048,576 words by 4 bits) CMOS static RAM.

Operating supply voltage is 3.3 V \pm 0.3 V.

★ The μ PD444004L is packaged in a 32-pin PLASTIC SOJ.

Features

- 1,048,576 words by 4 bits organization
- Fast access time: 8, 10, 12 ns (MAX.)
- Output Enable input for easy application
- Single +3.3 V power supply

★ Ordering Information

Part number	Package	Access time	Supply current	t mA (MAX.)
		ns (MAX.)	At operating	At standby
μPD444004LLE-A8	32-pin PLASTIC SOJ	8	180	5
μPD444004LLE-A10	(10.16 mm (400))	10	160	
μPD444004LLE-A12		12	150	

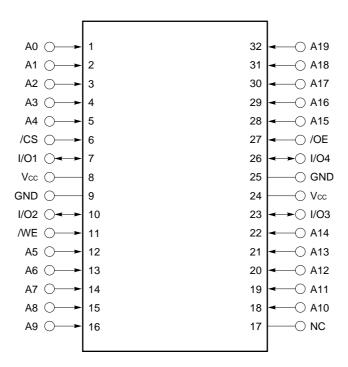
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ Pin Configuration (Marking Side)

/xxx indicates active low signal.

32-pin PLASTIC SOJ (10.16 mm (400))



A0 - A19 : Address Inputs

I/O1 - I/O4 : Data Inputs / Outputs

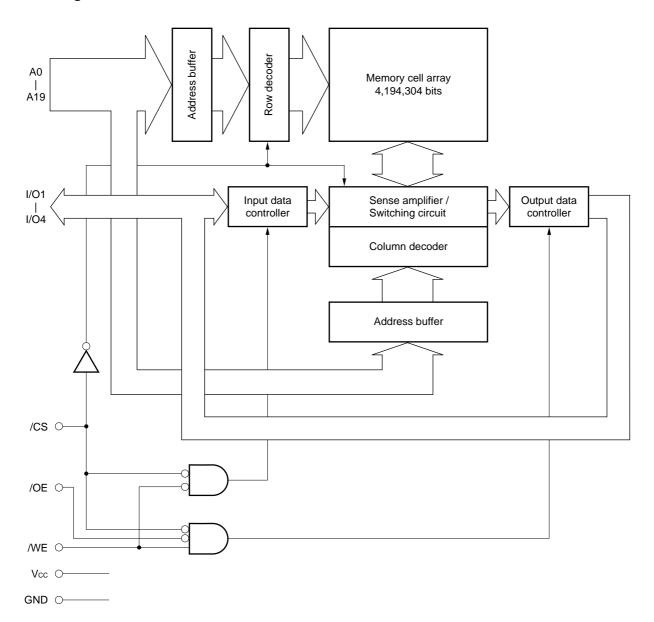
/CS : Chip Select
/WE : Write Enable
/OE : Output Enable
Vcc : Power supply

GND : Ground

NC : No connection

Remark Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
Н	×	×	Not selected	High impedance	Isв
L	L	Н	Read	D оит	Icc
L	×	L	Write	Write Din	
L	Н	Н	Output disable	High impedance	

Remark ×: Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	Vcc		-0.5 Note to +4.0	V
Input / Output voltage	VT		-0.5 ^{Note} to +4.0	V
Operating ambient temperature	TA		0 to 70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Note -2.0 V (MIN.) (pulse width: 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc+0.3	V
Low level input voltage	VIL		-0.3 Note		+0.8	V
Operating ambient temperature	TA		0		70	°C

Note -2.0 V (MIN.) (pulse width: 2 ns)



DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test con	MIN.	TYP.	MAX.	Unit	
Input leakage current	lu	VIN = 0 V to Vcc	-2		+2	μΑ	
Output leakage current	ILO	V _{I/O} = 0 V to Vcc,		-2		+2	μΑ
		/CS = VIH or /OE = VIH	or /WE = VIL				
Operating supply current	Icc	/CS = VIL,	Cycle time : 8 ns			180	mA
		I _{I/O} = 0 mA,	Cycle time : 10 ns			160	
		Minimum cycle time	Cycle time : 12 ns			150	
Standby supply current	Isa	/CS = VIH, VIN = VIH or	VIL			40	mA
	I _{SB1}	/CS ≥ Vcc - 0.2 V,	/CS ≥ Vcc - 0.2 V,			5	
		$V_{\text{IN}} \leq 0.2 \text{ V or } V_{\text{IN}} \geq V_{\text{C}}$					
High level output voltage	Vон	lон = −4.0 mA	2.4			V	
Low level output voltage	Vol	IoL = +8.0 mA				0.4	V

Remark Vin : Input voltage

Vi/o: Input / Output voltage

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cin	VIN = 0 V			6	pF
Input / Output capacitance	C _{I/O}	V _{1/0} = 0 V			8	pF

Remarks 1. VIN: Input voltage

Vi/o: Input / Output voltage

 $\textbf{2.} \ \ \text{These parameters are periodically sampled and not 100\% tested}.$

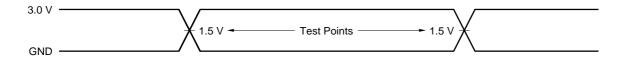
Data Sheet M14427EJ4V0DS

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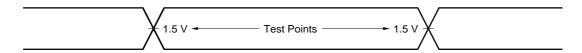
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)

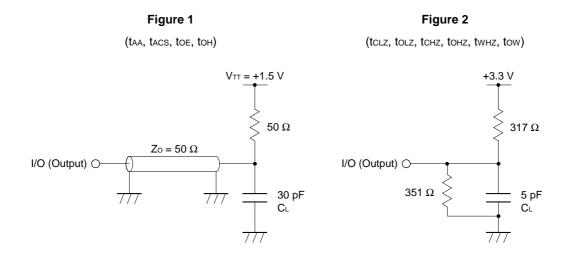


Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.



Remark CL includes capacitances of the probe and jig, and stray capacitances.

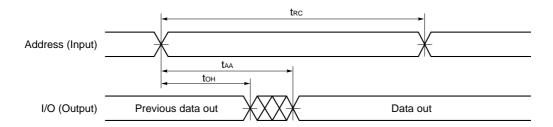
★ Read Cycle

Parameter	Symbol	-A8		-A10		-A12		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t RC	8		10		12		ns	
Address access time	taa		8		10		12	ns	1
/CS access time	tacs		8		10		12	ns	
/OE access time	t oe		4		5		6	ns	
Output hold from address change	tон	3		3		3		ns	
/CS to output in low impedance	tclz	3		3		3		ns	2, 3
/OE to output in low impedance	tolz	0		0		0		ns	
/CS to output in high impedance	t cHZ		4		5		6	ns	
/OE to output hold in high impedance	tонz		4		5		6	ns	

Notes 1. See the output load shown in Figure 1.

- 2. Transition is measured at \pm 200 mV from steady-state voltage with the output load shown in **Figure 2**.
- 3. These parameters are periodically sampled and not 100% tested.

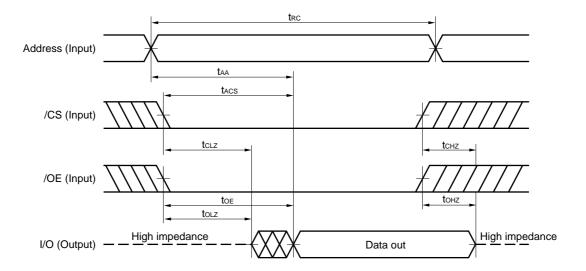
Read Cycle Timing Chart 1 (Address Access)



Remarks 1. In read cycle, /WE should be fixed to high level.

2. /CS = /OE = VIL

Read Cycle Timing Chart 2 (/CS Access)



Caution Address valid prior to or coincident with /CS low level input.

Remark In read cycle, /WE should be fixed to high level.

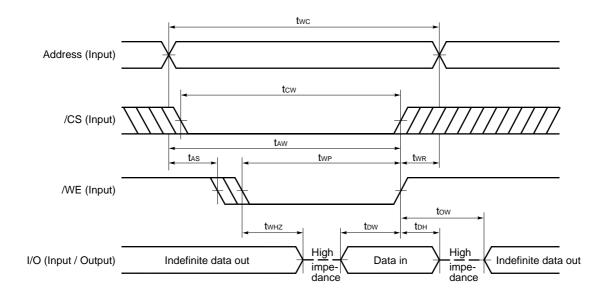
★ Write Cycle

Parameter	Symbol	-A8		-A10		-A12		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	twc	8		10		12		ns	
/CS to end of write	tcw	6		7		8		ns	
Address valid to end of write	taw	6		7		8		ns	
Write pulse width	twp	6		7		8		ns	
Data valid to end of write	tow	4		5		6		ns	
Data hold time	tон	0		0		0		ns	
Address setup time	t as	0		0		0		ns	
Write recovery time	twr	0		0		0		ns	
WE to output in high impedance	twнz		4		5		6	ns	1, 2
Output active from end of write	tow	3		3		3		ns	

Notes 1. Transition is measured at \pm 200 mV from steady-state voltage with the output load shown in **Figure 2**.

2. These parameters are periodically sampled and not 100% tested.

Write Cycle Timing Chart 1 (/WE Controlled)



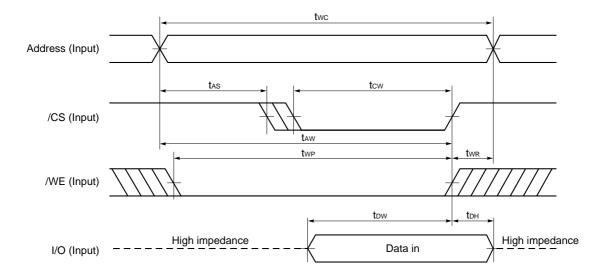
Cautions 1. /CS or /WE should be fixed to high level during address transition.

2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

2. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)



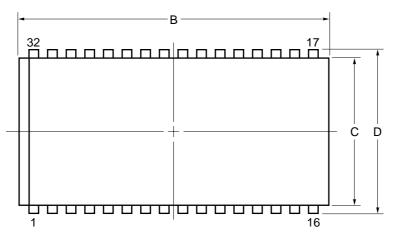
Cautions 1. /CS or /WE should be fixed to high level during address transition.

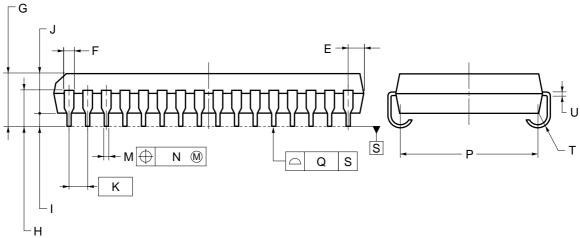
2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

Package Drawing

32-PIN PLASTIC SOJ (10.16 mm (400))





NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

MILLIMETERS
21.26±0.2
10.16
11.18±0.2
1.005±0.1
0.74
3.5±0.2
2.545±0.2
0.8 MIN.
2.6
1.27(T.P.)
0.40±0.10
0.12
9.4±0.20
0.1
R0.85
$0.20^{+0.10}_{-0.05}$

P32LE-400A-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD444004L.

★ Type of Surface Mount Device

 μ PD444004LLE : 32-pin PLASTIC SOJ (10.16 mm (400))

Revision History

Edition/	Pa	Page		Page		Location	Description
Date	This edition	Previous edition	revision		(Previous edition \rightarrow This edition)		
4th edition/	p.1, 2, 11, 12	p.1, 2, 12, 13	Deletion	Ordering Information,	32-pin PLASTIC TSOP (II)		
May 2002				Pin Configuration,			
				Package Drawing,			
				Type of Surface Mount Device			
	p.5	p.5	Deletion	DC Characteristics	Remark 2		
	p.7, 9	p.7, 9	Deletion	Read Cycle, Write Cycle	Remark		

NEC μ PD444004L

[MEMO]

NOTES FOR CMOS DEVICES -

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3 STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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