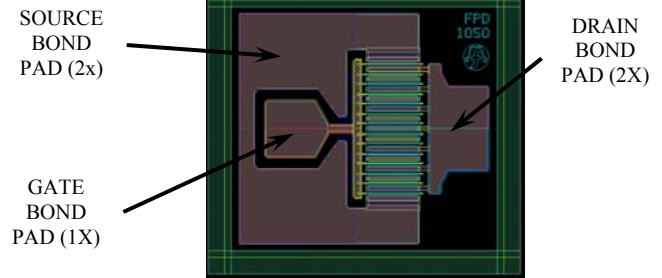


FEATURES

- ◆ 28.5 dBm Linear Output Power at 12 GHz
- ◆ 11 dB Power Gain at 12 GHz
- ◆ 14 dB Maximum Stable Gain at 12 GHz
- ◆ 41 dBm Output IP3
- ◆ 45% Power-Added Efficiency



DIE SIZE: 470 x 440 μm
DIE THICKNESS: 100 μm
BONDING PADS: >85 x 60 μm

DESCRIPTION AND APPLICATIONS

The FPD1050 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a 0.25 μm by 1050 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750 also features Si_3N_4 passivation and is also available in a low cost plastic SOT89 plastic package.

Typical applications include commercial and other narrowband and broadband high-performance amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT $f = 12 \text{ GHz}$ USING CW SIGNAL						
Power at 1dB Gain Compression	$P_{1\text{dB}}$	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	27.5	28.5		dBm
Maximum Stable Gain (S_{21}/S_{12})	MSG	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$		14.0		dB
Power Gain at $P_{1\text{dB}}$	$G_{1\text{dB}}$	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	10.0	11.0		dB
Power-Added Efficiency	PAE	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}};$ $P_{\text{OUT}} = P_{1\text{dB}}$		45		%
Output Third-Order Intercept Point (from 15 to 5 dB below $P_{1\text{dB}}$)	IP3	$V_{\text{DS}} = 10 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$ Matched for optimal power Tuned for best IP3		39 41		dBm
Saturated Drain-Source Current	I_{DSS}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	250	315	375	mA
Maximum Drain-Source Current	I_{MAX}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} \cong +1 \text{ V}$		520		mA
Transconductance	G_{M}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} = 0 \text{ V}$		280		mS
Gate-Source Leakage Current	I_{GSO}	$V_{\text{GS}} = -5 \text{ V}$		15		μA
Pinch-Off Voltage	$ V_{\text{P}} $	$V_{\text{DS}} = 1.3 \text{ V}; I_{\text{DS}} = 1 \text{ mA}$		1.0		V
Gate-Source Breakdown Voltage	$ V_{\text{BDGS}} $	$I_{\text{GS}} = 1 \text{ mA}$	16	18		V
Gate-Drain Breakdown Voltage	$ V_{\text{BDGD}} $	$I_{\text{GD}} = 1 \text{ mA}$	16	18		V
Thermal Resistivity (see Notes)	θ_{JC}	$V_{\text{DS}} > 6 \text{ V}$		45		$^{\circ}\text{C/W}$

• ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		10	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		10	mA
RF Input Power	P_{IN}	Under any acceptable bias state		175	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	°C
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	°C
Total Power Dissipation	P_{TOT}	See De-Rating Note below		3.4	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits**		2 or more Max. Limits		80	%

* $T_{Ambient} = 22^{\circ}C$ unless otherwise noted

**Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
 P_{DC} : DC Bias Power
 P_{IN} : RF Input Power
 P_{OUT} : RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above $22^{\circ}C$:
 $P_{TOT} = 3.4W - (0.022W/^{\circ}C) \times T_{HS}$
where T_{HS} = heatsink or ambient temperature above $22^{\circ}C$

Example: For a $85^{\circ}C$ heatsink temperature: $P_{TOT} = 3.4W - (0.022 \times (85 - 22)) = 2.01W$

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

• ASSEMBLY INSTRUCTIONS

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be $280-290^{\circ}C$; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be $250-260^{\circ}C$.

• APPLICATIONS NOTES & DESIGN DATA

Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

All information and specifications are subject to change without notice.