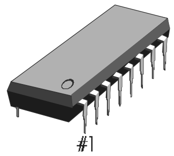
KS8620 1 Chip CODEC for Digital Answering phone

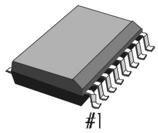
INTRODUCTION

The KS8620 consists of on-chip PCM encoders, decoders (PCM CODECs) and PCM line filter. This device provide all the functions required to interface a full-duplex voice telephone circuit, digital answering phone. This device is designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering function in PCM system. Also it is intended to be used at the analog termination of a PCM line / trunk. This device provide the Band pass filtering of the analog signals prior to encoding and after decoding. This combination device performs the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

16-DIP-300



16-SOP-BD300 - SG



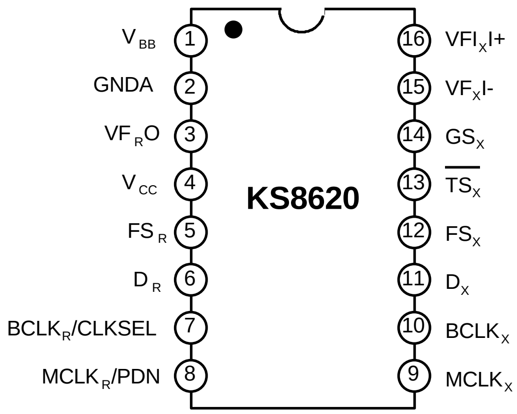
ORDERING INFORMATION

Device	Package	Operating Temperature
KS8620N	16-DIP-300	0ºC ~ + 70ºC
KS8620D	16-SOP- BD300 - SG	

FEATURES

- Complete CODEC and filtering system
- Encoding / Decoding : 8 bits µ-law PCM
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation : 60mW (operating)
  3mW (standby)
- ± 5V operation
- TTL or CMOS compatible
- Automatic power down

PIN CONFIGURATION



BLOCK DIAGRAM

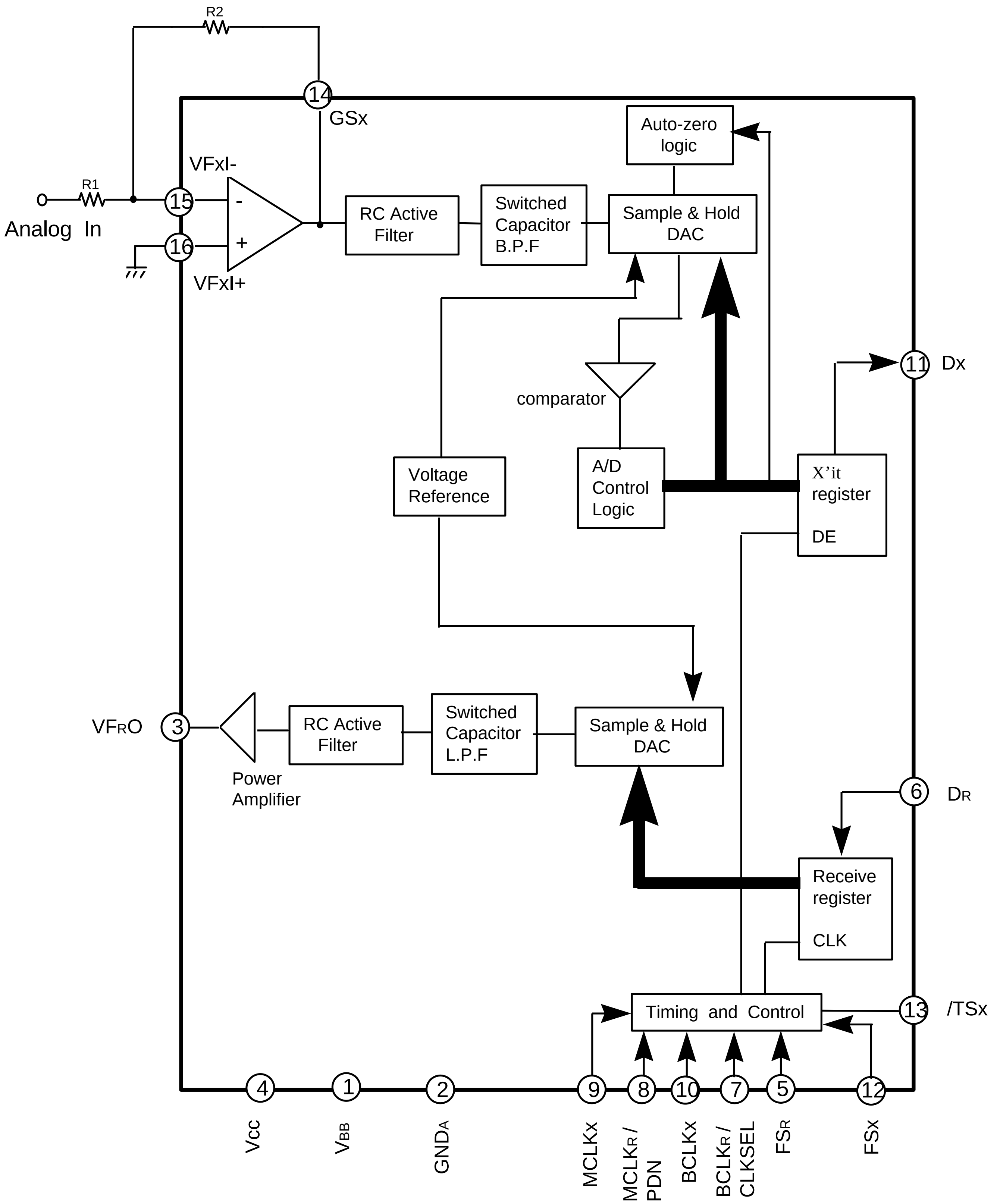


Fig 1. Block Diagram

PIN DESCRIPTION

Pin No	Symbol	Description
1	V_{BB}	VBB = -5V ± 5%
2	GNDA	Analog ground
3	VF_RO	Analog output of the receiver filter
4	V_{CC}	Vcc = +5V ± 5%
5	FS_R	Receive frame sync pulse. 8KHz pulse train.
6	D_R	PCM data input
7	$BCLK_R$ / CLKSEL	Logic input which selects either 1.536MHz / 1.544MHz or 2.048MHz for master clock in normal operation and BCLKx is used for both TX and RX directions. Alternately direct clock input available, vary from 64KHz to 2.048MHz.
8	$MCLK_R$ / PDN	When $MCLK_R$ is connected continuously high, the device goes powered down . Normally connected continuously low, MCLKx is selected for all DAC timing. Alternately direct 1.536MHz / 1.544MHz or 2.048MHz clock input is available.
9	$MCLK_X$	1.536MHz / 1.544MHz or 2.048MHz clock input is available
10	$BCLK_X$	May be vary from 64KHz 2.048MHz, but BCLKx is externally tied with MCLKx in normal operation.
11	D_X	PCM data output.
12	FS_X	TX frame sync pulse. 8KHz pulse train.
13	TS_X	Changed from high to low during the encoder timeslot. Open drain output.
14	GS_X	Analog output of the TX input amplifier. Used to set gain through external resistor between pin 14 to pin 15.
15	VF_XI-	Inverting input stage of the TX analog signal.
16	VF_XI+	Non-inverting input stage of the TX analog signal.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	Vcc	+7	V
Negative Supply Voltage	VBB	-7	V
Voltage at any Analog Input or Output	$V_{I(A)}$	Vcc + 0.3 to VBB - 0.3	V
Voltage at any Digital Input or Output	$V_{I(D)}$	Vcc + 0.3 to GNDA - 0.3	V
Operating Temperature Range	Ta	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature Range (soldering , 10 sec)	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified : Ta = 0ºC to 70ºC , Vcc = 5V ±5%, V_{BB} = -5V ±5%, GND_A = 0V)

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Power Dissipation						
Power down Current	$I_{CC(down)}$	No Load		0.5	3.0	mA
	$I_{BB(down)}$	No Load		0.05	1.0	
Active Current	$I_{CC(A)}$	No Load		6.0	10	mA
	$I_{BB(A)}$	No Load		6.0	10	
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Input Low Current	I_{IL}	$GND_A < V_{IN} < V_{IL}$, all digital input	-15		15	uA
Input High Current	I_{IH}	$V_{IH} < V_{IN} < Vcc$	-15		15	uA
Output Low Voltage	V_{OL}	D_X , I_L = 3.2 mA			0.4	V
		SIG_R , I_L = 1.0 mA			0.4	
		/TS_X , I_L = 3.2 mA , open drain			0.4	
Output High Voltage	V_{OH}	D_X , I_H = -3.2 mA	2.4			V
		SIG_R , I_H = -1.0 mA	2.4			
Output Current in High impedance state (Tri - state)	$I_{OH(HZ)}$	D_X , $GND_A < V_O < Vcc$	-15		15	uA
Analog Interface with Receiver Filter						
Output Resistance	R_O	pin VF_RO		1	3	Ω
Load Resistance	R_L	VF_RO = + / - 2.5V	600			Ω
Load Capacitance	C_L				500	pF
Output DC offset voltage	$V_{OO(RX)}$		-200		200	mV
Analog Interface with Transmit input Amp						
Input Leakage Current	I_{LKG}	-2.5V< V<+2.5V , VF_XI+ or VF_XI-	-200		200	nA
Input Resistance	R_I	-2.5V< V<+2.5V , VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_O	closed loop , unity gain		1	3	Ω
Load Resistance	R_L	GSx	10			KΩ
Load Capacitance	C_L	GSx			50	pF
Output Dynamic Range	$V_{OD(TX)}$	GSx , R_L < 10KΩ	+/-2.8			V
Voltage Gain	G_V	VF_XI+ to GS_X	5,000			V / V
Unity Gain bandwidth	B W		1	2		MHz
Offset Voltage	$V_{IO(TX)}$		-20		20	mV
Common - mode Voltage	$V_{CM(TX)}$	$CMRR_XA$ > 60dB	-2.5		2.5	V
Common mode rejection ratio	CMRR	DC test	55			dB
Power supply rejection ratio	PSRR	DC test	55			dB

TIMING CHARACTERISTICS

(Unless otherwise specified : Ta = 0ºC to 70ºC, Vcc = 5V ±5%, V_{BB} = -5V ±5%, GND_A = 0V)

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Frequency of Master Clock	f_{MCK}	Depends on the device used and the $BCLK_R$ /CLKSEL pin. MCLKx and $MCLK_R$		1.536 1.544 2.048		MHz
Rise time of Bit Clock	$t_{R(BCK)}$	t_{PB} = 488ns			50	nS
Fall Time of Bit Clock	$t_{F(BCK)}$	t_{PB} = 488ns			50	nS
Hold Time for Bit Clock low to Frame sync	$t_{H(LFS)}$	Long Frame only	0			nS
Hold Time for Bit Clock High to Frame sync	$t_{H(HFS)}$	Short Frame only	0			nS
Set-up Time from Frame sync to Bit Clock low	$t_{SU(FBCL)}$	Long Frame only	80			nS
Delay time from BCLKx High to data valid	$t_{D(HDV)}$	Load = 150pF + 2 LSTTL loads	0		180	nS
Delay time to /TSx low	$t_{D(/TSXL)}$	Load = 150pF + 2 LSTTL loads			140	nS
Delay time from BCLKx low to data output disable	$t_{D(LDD)}$		50		165	nS
Delay Time to valid data from FSx or BCLKx.	$t_{D(VD)}$	CL = 0 pF to 150 pF Whichever comes later.	20		165	nS
Set-up Time from D_R valid to BCLK x/R low	$t_{SU(DRBL)}$		50			nS
Hold time from BCLK x/R low to D_R invalid	$t_{H(BLDR)}$		50			nS
Set-up time from FS x/R to BCLK x/R low	$t_{SU(FBLS)}$	Short Frame sync pulse (1 or 2 bit clock periods long) : note1	50			nS
Width of master clock High	$t_{W(MCKH)}$	MCLKx and $MCLK_R$	160			nS
Width of master clock Low	$t_{W(MCKL)}$	MCLKx and $MCLK_R$	160			nS
Rise Time of Master clock	$t_{R(MCK)}$	MCLKx and $MCLK_R$			50	nS
Fall Time of Master clock	$t_{F(MCK)}$	MCLKx and $MCLK_R$			50	nS
Set-up time from BCLKx High (FSx in Long Frame Sync mode) to MCLKx falling edge	$t_{SU(BHMF)}$	1`st bit clock after the leading edge of FSx	50			nS
Period of Bit Clock	t_{CK}		485	488	15,725	nS
Width of Bit clock High	$t_{W(BCKH)}$	V_{IH} = 2.2V	160			nS
Width of Bit clock Low	$t_{W(BCKL)}$	V_{IL} = 0.6V	160			nS
Hold time from BCLK x/R to FS x/R low	$t_{H(BLFL)}$	Short Frame sync pulse (1 or 2 bit clock periods long) : note1	100			nS

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified : Ta = 0°C to 70°C, Vcc = 5V ±5%, V_{BB} = -5V ±5%, GND_A = 0V, f = 1.02KHz
Vin = 0dBm0, transmit input amplifier connected for unity-gain, non-inverting)

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Amplitude Response						
Receive Gain, Absolute	$G_{V(ARX)}$	Ta=25°C,V_{CC} = 5V, V_{BB} = -5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	-1.5		1.5	dB
Receive Gain, Relative to Gv(RRX)	$G_{V(RRX)}$	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	-0.6 -0.55 -1.5		0.5 0.5 1.5	dB
Absolute Receive Gain Variations with temperature	$\Delta G_{V(ARX)}$ / Δ T	Ta = 0°C to 70°C			± 0.1	dB
Receive Gain Variations with level	$\Delta G_{V(RXL)}$	Sinusoidal test method; reference input PCM code correspond to an ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0	-0.4 -0.8		0.4 0.8	dB
Receive output drive level		R_L = 600Ω	-2.5		2.5	V
Absolute level	$V_{O(RX)}$ V_{AL}	Norminal 0dBm0 level is same as 4 dBm (600Ω)		1.2276		Vrms
Max overload level	$V_{OL(MAX)}$	Max overload level (3.17dBm0)		2.501		V_{PK}
Transmit gain, absolute	$G_{V(ATX)}$	Ta = 25°C,Vcc =5V, V_{BB} = -5V Input at GSx = 0dBm0 at 1020Hz	-1.5		1.5	dB
Transmit gain, relative to Gv(ATX)	$G_{V(RTX)}$	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz - 3000Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and above, mesaure response from 0 Hz to 4 KHz	 -2 -0.5 -0.55 -1.5		-35 -25 -21 -0.5 0.5 0.5 -1.5 -10 -25	dB

TRANSMISSION CHARACTERISTICS *(Continued)*

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Absolute trasmit gain variations with temperature	$\Delta G_{V(ATX)} / \Delta T$	Ta = 0ºC to 70ºC			± 0.1	dB
Transmit gain variations with level	$\Delta G_{V(TXL)}$	Sinusoldal test method ; Reference level = -10dBm0 VF_XI + = -40dBm0 to +3dB0 VF_XI + = -50dBm0 to -40dB0	 -0.4 -0.8		 0.4 0.8	dB
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	$t_{D(ARX)}$	f = 1600Hz			200	µs
Receive Delay, Relative to $t_{D\ (ARX)}$	$t_{D(RRX)}$	f = 500Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz	-40 -30		 90 125 175	µs
Transmit Delay, Absolute	$t_{D(ATX)}$	f = 1600Hz			315	µs
Transmit Delay, Relative to $t_{D(ATX)}$	$t_{D(RTX)}$	f = 500Hz - 600Hz f = 600Hz - 800Hz f = 800Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz			220 145 75 40 75 105 155	µs
Noise						
Receive Noise, C Message Weighted	N_{RXC}	PCM code equals alternating positive and negative zero, KS8620			18	dBrnC0
Transmit Noise, C Message Weighted	N_{TXC}	KS8620			15	dBrnC0

TRANSMISSION CHARACTERISTICS *(Continued)*

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Noise, Single Frequency	NSF	f = 0KHz to 100KHz, loop around measurement, VF_XI+ = 0Vrms			-53	dBm0
Positive Power Supply Rejection, Transmit	$PSRR_{(PTX)}$	VF_XI+ = 0 Vrms, Vcc = 5.0 V_{DC} + 100mVms f = 0KHz - 50KHz	25			dBC
Negative Power Supply Rejection, Transmit	$PSRR_{(NTX)}$	VF_XI+ = 0 Vrms, V_{BB} = -5.0 V_{DC} + 100mVrms f = 0KHz - 50KHz	25			dBC
Positive Power Supply Rejection, Receive	$PSRR_{(PRX)}$	PCM code equals positive zero Vcc = 5.0V_{DC} + 100mVrms f = 0Hz - 4000Hz f = 4KHz - 25KHz	 25 25			 dBC dB
Negative Power Supply Rejection, Receive	$PSRR_{(NRX)}$	PCM code equals positive zero V_{BB} = -5.0V_{DC} + 100mVrms f = 0Hz - 4000Hz f = 4KHz - 25KHz	 25 25			 dBC dB
Spurious Out-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz - 3400Hz input PCM applied to D_R, Measure individual image signals at VF_RO 4600Hz -7600Hz 7600Hz - 100,000Hz			 -28 -35	dB
Distortion						
Signal to Total Distortion Transmit or Receive Half-Channel	THD_{TX} THD_{RX}	Sinusoidal test method ; level = 3.0dBm0 = 0dBm0 to 30dBm0 = -40dBm0 XMT RCV	 28 30 25 25			dBC

TRANSMISSION CHARACTERISTICS *(Continued)*

Characteristic	System	Test Conditions	Min	Typ	Max	Unit
Single Frequency Disotrtion, Transmit	$THD_{SF(TX)}$				-41	-dB
Single Frequency Distortion, Receive	$THD_{SF(RX)}$				-41	-dB
Intermodulation Distortion	THD_{IMD}	Loop around measurement, VFxI+ = -4dBm0 to -21dBm0, two frequencies in the range 300Hz - 3400Hz			-35	-dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit level	$CT_{(TX-RX)}$	f = 300Hz - 3400Hz D_R = Steady PCM code		-90	-75	dB
Reveive to Transmit Crosstalk, 0dBm0 Receive level	$CT_{(RX-TX)}$	f = 300Hz - 3400Hz, VFXI = 0V		-90	-70 (note1)	dB

Note 1. $CT_{(RX-TX)}$ is measured with a -40dBm0 activating signal applied at VF_XI+

ENCODING FORMAT AT D_X OUTPUT

	µ -Law PCM : KS8620
V_{IN} (at GS_X) = + Full Scale	1 0 0 0 0 0 0 0
V_{IN} (at GSx) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GSx) = - Full Scale	0 0 0 0 0 0 0 0