

MOS FIELD EFFECT TRANSISTOR 2SK2826

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance $R_{DS(on)1} = 6.5 \text{ m}\Omega$ (MAX.) (Ves = 10 V, ID = 35 A) $R_{DS(on)2} = 9.7 \text{ m}\Omega$ (MAX.) (Ves = 4.0 V, ID = 35 A)
- Low Ciss : Ciss = 7200 pF (TYP.)
- Built-in Gate Protection Diode

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK2826	TO-220AB		
2SK2826-S	TO-262		
2SK2826-ZJ	TO-263		

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (V _{DS} = 0 V)	VGSS(AC)	±20	V
Gate to Source Voltage (Vps = 0 V)	VGSS(DC)	+20, -10	V
Drain Current (DC)	I _{D(DC)}	±70	Α
Drain Current (Pulse) Note1	D(pulse)	±280	Α
Total Power Dissipation (Tc = 25°C)	PT	100	W
Total Power Dissipation (T _A = 25°C)	Рт	1.5	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C
Single Avalanche Current Note2	IAS	70	Α
Single Avalanche Energy Note2	Eas	490	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Starting Tch = 25 °C, RA = 25 Ω , VGS = 20 V \rightarrow 0 V

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.25	°C/W	
Channel to Ambient	Rth(ch-A)	83.3	°C/W	

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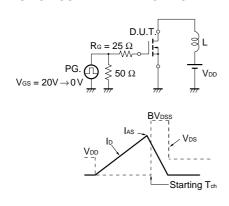
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

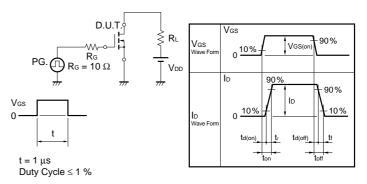
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
*	Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 35 A		5.5	6.5	mΩ
		RDS(on)2	Vgs = 4.0 V, Ip = 35 A		7.0	9.7	mΩ
	Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
	Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 35 A	20	94		S
	Drain Leakage Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
	Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
	Input Capacitance	Ciss	V _{DS} = 10 V		7200		pF
	Output Capacitance	Coss	V _G S = 0 V		2000		pF
	Reverse Transfer Capacitance	Crss	f = 1 MHz		700		pF
*	Turn-on Delay Time	td(on)	ID = 35 A		100		ns
*	Rise Time	tr	V _{GS(on)} = 10 V		1200		ns
*	Turn-off Delay Time	td(off)	V _{DD} = 30 V		440		ns
*	Fall Time	tf	$R_G = 10 \Omega$		520		ns
	Total Gate Charge	QG	ID = 70 A		150		nC
	Gate to Source Charge	Qgs	V _{DD} = 48 V		20		nC
	Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		40		nC
	Body Diode Forward Voltage	V _F (S-D)	IF = 70 A, VGS = 0 V		0.97		V
	Reverse Recovery Time	trr	IF = 70 A, VGS = 0 V		80		ns
	Reverse Recovery Charge	Qrr	di/dt = 100A/μ s		250		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME

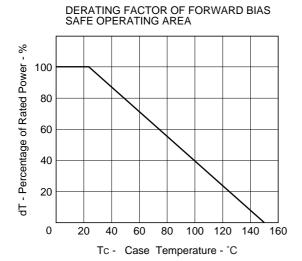




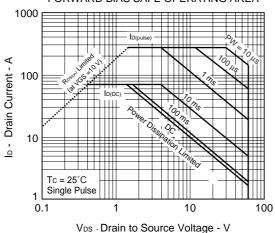
TEST CIRCUIT 3 GATE CHARGE



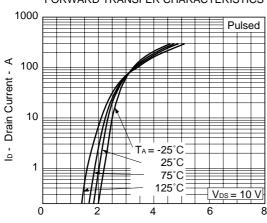
TYPICAL CHARACTERISTICS (TA = 25 °C)



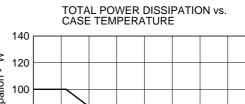


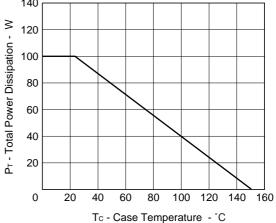


FORWARD TRANSFER CHARACTERISTICS

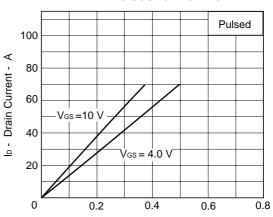


V_{GS} - Gate to Source Voltage - V



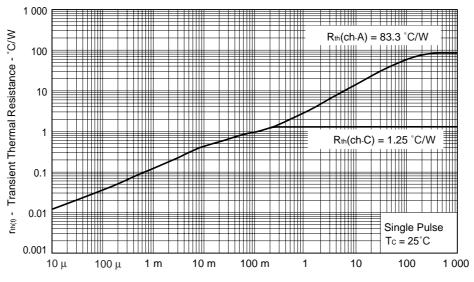


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



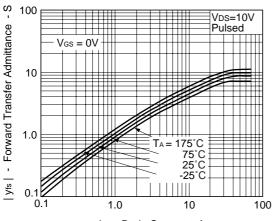
V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

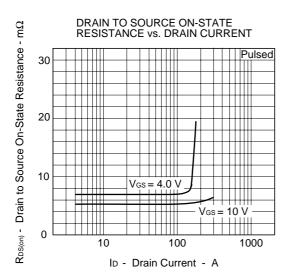


PW - Pulse Width - s

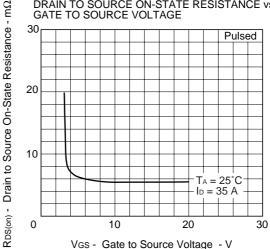
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

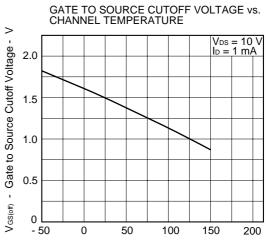


ID - Drain Current - A



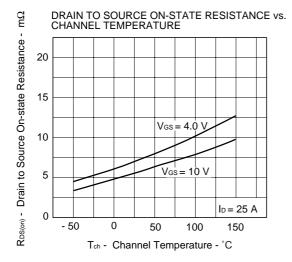
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE





Tch - Channel Temperature - °C





Pulsed Poly Pulsed V_s = 10 V V_s = 0 V V_s = 0 V

1.0

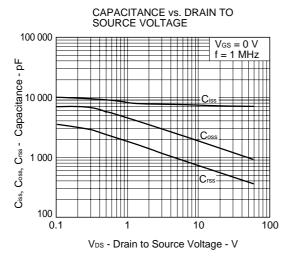
Vsp - Source to Drain Voltage - V

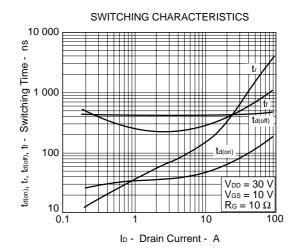
1.5

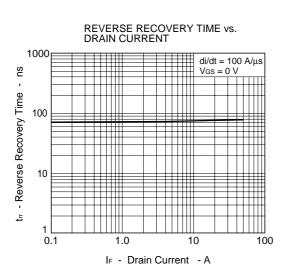
0.5

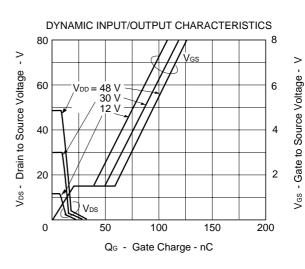
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SOURCE TO DRAIN DIODE FORWARD VOLTAGE

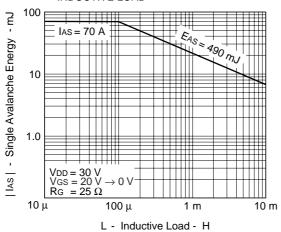




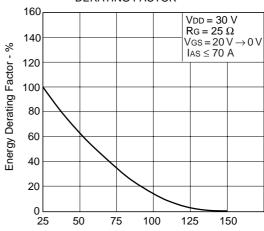




SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR

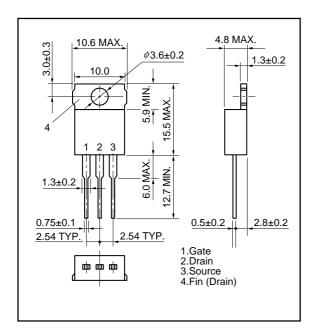


Starting Tch - Starting Channel Temperature - °C

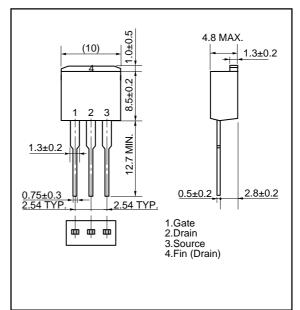


PACKAGE DRAWINGS (Unit:mm)

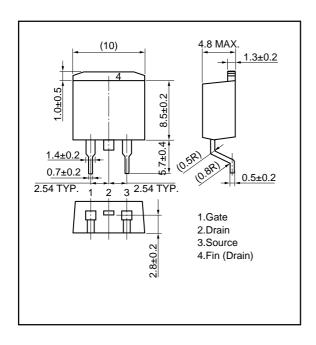
1)TO-220AB (MP-25)



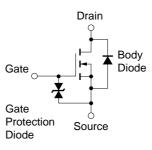
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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