AsahiKASEI
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AKD5388-A
AK5388 Evaluation Board Rev.4

GENERAL DESCRIPTION

AKD5388 is an evaluation board for the digital audio 24bit 216kHz 4ch A/D converter, AK5388. The AKD5388-A includes the input circuit and also has a digital interface transmitter. Further, the AKD5388-A can achieve the interface with digital audio systems via opt-connector.

AKD5388-A is an evaluation board for AK5388, of 216kHz sampling 24bit 4ch A/D converter for professional audio. AKD5388-A has analog input buffer circuits, clock generator circuits, and digital audio interfaces. Therefore it can achieve the interface with digital audio systems via optical connector. And it can achieve the direct interface with AKEMD's D/A converter evaluation boards of via 10-line flat cable.

■ Ordering guide

AKD5388-A --- AK5388 Evaluation Board

FUNCTION

- **DIT with optical output**
- **BNC connector for an external clock input**

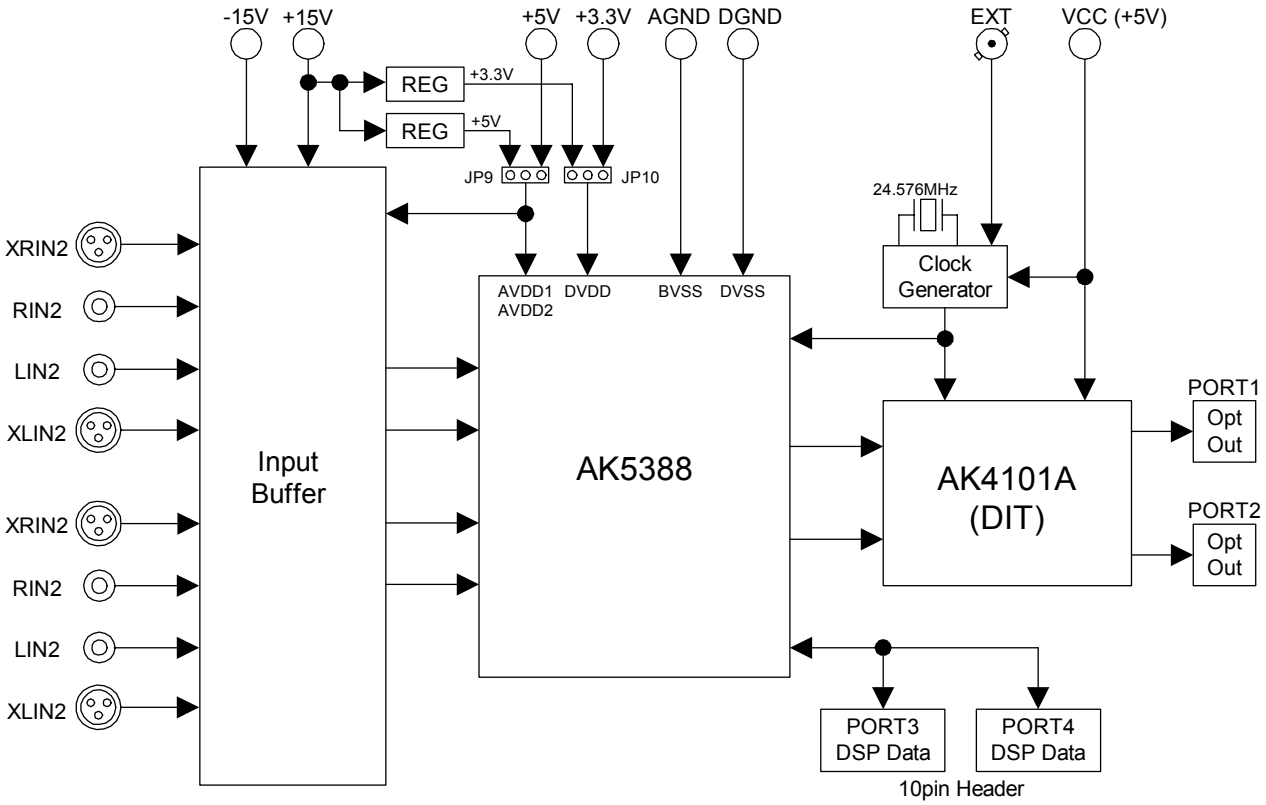


Figure 1. AKD5388-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supplies lines.

Name of connector	Color of connector	Voltage	Used for	Comment and attention	Default Setting
+15V	Red	+12~15V	Regulator T1, Regulator T2. OP-Amplifier	This connector should be connected. And this connector is used when AVDD of AK5388 is supplied from regulator T1 and DVDD of AK5388 is supplied from regulator T2. In this case, JP9 and JP10 should be REG side. When this is REG side, +5V and +3.3V connector should be open. (Default)	+15V
-15V	Blue	-12~-15V	OP-Amplifier	This connector should be connected.	-15V
+5V	Orange	+4.75~+5.25V	AVDD of AK5388, Analog input buffer circuit	This connector is used when AVDD of AK5388 is supplied from +5V connector without regulator T1. In this case, JP9 should be +5V side.	Open
+3.3V	Green	+3.0~+3.6V	DVDD of AK5388	This connector is used when DVDD of AK5388 is supplied from +3.3V connector without regulator T2. In this case, JP10 should be +3.3V side.	Open
VCC	Orange	+4.75~+5.25V	AK4101A, Logic circuit	This connector should be connected.	+5V
AGND	Black	0V	Analog ground	This connector should be connected.	0V
DGND	Black	0V	Digital ground	This connector is used when DGND is supplied besides AGND. In this case, JP15 should be open. (Default)	0V

Table 1. Power supply lines

(Note) Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK5388 and AK4101A should be reset once bringing SW3 = "L" upon power-up.

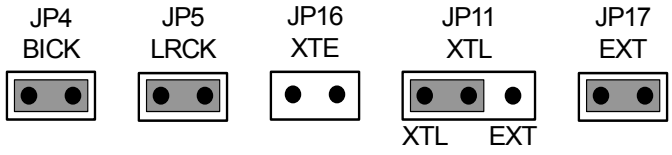
Note: When AK5388 is TDM mode, the AK4101A does not support the TDM mode. Therefore, PORT1 and PORT2 cannot be used. Also, when the sampling frequency is used by 96kHz or more, PORT1 and PORT2 cannot be used. Please use PORT3 (DSP1) and PORT4 (DSP2).

■ Evaluation mode

(1) Slave mode

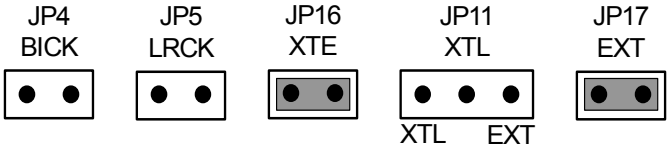
(1-1) A/D evaluation using DIT function of AK4101A

PORT1 and PORT2 are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX197). It is possible to connect AKEMD's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP1) and PORT4 (DSP2). In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



(1-2) Feeding all clocks from PORT3 (DSP1)

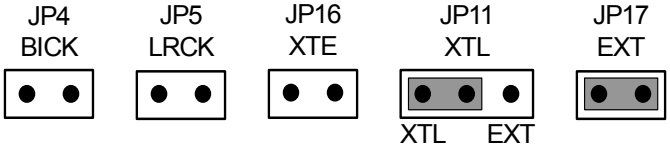
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT3 (DSP1). The A/D converted data is output from SDTO1/SDTO2 of PORT3 (DSP1). Also, the A/D converted data is output through optical connector (TOTX197).



(2) Master mode

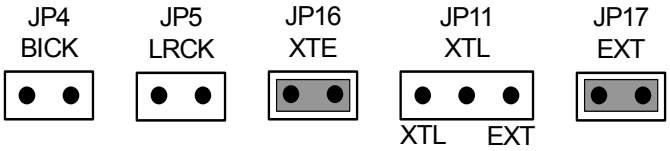
(2-1) A/D evaluation using DIT function of AK4101A

PORT1 and PORT2 are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX197). It is possible to connect AKEMD's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP1) and PORT4 (DSP2). In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



(2-2) Feeding all clocks from PORT3 (DSP1)

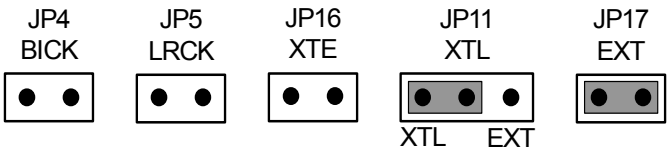
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT3 (DSP1). The A/D converted data is output from SDTO1/SDTO2 of PORT3 (DSP1). Also, the A/D converted data is output through optical connector (TOTX197).



(3) Cascade TDM mode

(3-1) Evaluation of cascade TDM mode that uses two AKD5388-A

PORT3 (DSP1) and PORT4 (DSP2) are used. In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



■ Default configuration of switch and jumper pins

	Name	Setting
SW1-1	M_SN	OFF
SW1-2	CKS2	ON
SW1-3	CKS1	OFF
SW1-4	CKS0	OFF
SW1-5	TDM1	OFF
SW1-6	TDM0	OFF
SW1-7	MONO	OFF
SW1-8	HPFE	OFF

	Name	Setting
SW2-1	DIF	OFF
SW2-2	CKS1	ON
SW2-3	CKS0	ON

Table 2. Switch setting

	Name	Setting
JP1	TEST1	Short
JP2	TEST2	Short
JP3	TEST3	Short
JP4	BICK	Short
JP5	LRCK	Short
JP6	TDMIN	GND
JP7	D-SEL1	SDTO1
JP8	D-SEL2	SDTO1
JP9	AVDD	REG
JP10	DVDD	REG

	Name	Setting
JP11	MCLK	XTL
JP12	CLK	X/2
JP13	BCFS	X2/4
JP14	LRFS	X2/256
JP15	GND	Open
JP16	XTE	Open
JP17	EXT	Short
JP18	LIN1-BNC	Short
JP19	LIN1-BNC	Short
JP20	RIN1-BNC	Short

	Name	Setting
JP21	RIN1-BNC	Short
JP22	LIN2-BNC	Short
JP23	LIN2-BNC	Short
JP24	RIN2-BNC	Short
JP25	RIN2-BNC	Short

Table 3. Jumper pins setting

■ Other jumper pins set up

1. JP6 (TDMIN) : Input data selection to TDMIN
   - EXT : Select data of SDTO1 of PORT3(DSP1) or PORT4(DSP2) is input.
     In this case, either JP7 or JP8 is set to TDMIN. Separated.
   - GND : 0V is input. <Default>

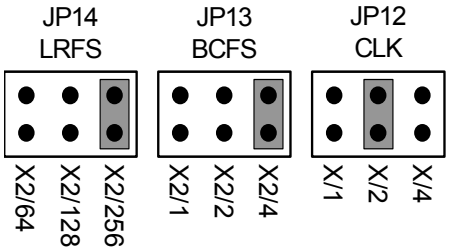
2. JP7 (D-SEL1) : Selection to SDTO1 of PORT3
   - SDTO1 : Connects with SDTO1 of AK5388. <Default>
   - TDMIN : Connects with TDMIN of AK5388.

3. JP8 (D-SEL2) : Selection to SDTO1 of PORT4
   - SDTO1 : Connects with SDTO1 of AK5388. <Default>
   - TDMIN : Connects with TDMIN of AK5388.

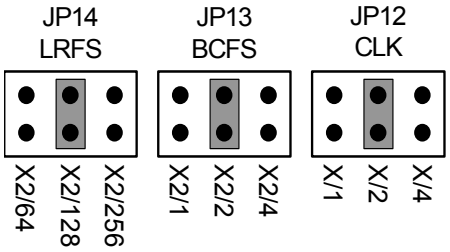
4. JP9 (AVDD) : Select AVDD for AK5388
   - +5V : Supply from +5V connector.
   - REG : Supply from regulator T1. In this case, +5V connector should be open. <Default>

5. JP10 (DVDD): Select DVDD for AK5388
   - +3.3V : Supply from +3.3V connector.
   - REG : Supply from regulator T2. In this case, +3.3V connector should be open. <Default>

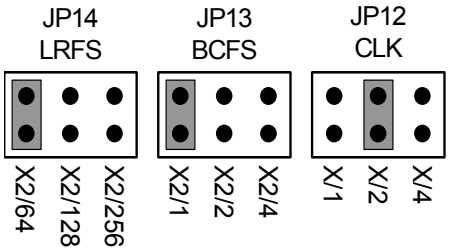
6. JP12 (CLK), JP13 (BCFS), JP14 (LRFS) : Select clock frequency
fs=48kHz : <Default>



fs=96kHz :



fs=192kHz:



Other frequency: Please set JP12, JP13, and JP14 properly.

7. JP15 (GND) : Analog ground and Digital ground
OPEN : Separated. <Default>
SHORT : Common. (The connector "DGND" can be open.)

8. JP18, JP19 (LIN1-BNC) : Input terminal selection of LIN1
OPEN : Select to XLR connector (J1).
SHORT : Select to RCA connector (J5). <Default>

9. JP20, JP21 (RIN1-BNC) : Input terminal selection of RIN1
OPEN : Select to XLR connector (J2).
SHORT : Select to RCA connector (J6). <Default>

10. JP22, JP23 (LIN2-BNC) : Input terminal selection of LIN2
OPEN : Select to XLR connector (J3).
SHORT : Select to RCA connector (J7). <Default>

11. JP24, JP25 (RIN2-BNC) : Input terminal selection of RIN2
OPEN : Select to XLR connector (J4).
SHORT : Select to RCA connector (J8). <Default>

■ DIP Switch Setting

[SW1] (MODE1): Setting the evaluation mode for AK5388
ON is "H", OFF is "L".

No.	Name	OFF ("L")	ON ("H")	Default
1	M_SN	Slave mode	Master mode	OFF ("L")
2	CKS2	See Table 6		ON ("H")
3	CKS1			OFF ("L")
4	CKS0			OFF ("L")
5	TDM1	See Table 7		OFF ("L")
6	TDM0			OFF ("L")
7	MONO	MONO mode OFF	MONO mode ON	OFF ("L")
8	HPFE	High pass filter OFF	High pass filter ON	OFF ("L")

Table 4. Mode setting of AK5388

[SW2] (MODE2): Setting the evaluation mode for AK5388 and AK4101A
ON is "H", OFF is "L".

No.	Name	OFF ("L")	ON ("H")	Default
1	DIF	MSB justified	I^2S Compatible	OFF ("L")
3	CKS1	See Table 8		ON ("H")
4	CKS0			ON ("H")

Table 5. Mode setting of AK5388 and AK411A

M_SN	CKS2	CKS1	CKS0	MCLK Frequency	
L	L	L	L	128fs (108KHz < fs ≤ 216KHz)	
	L	L	H	192fs (108KHz < fs ≤ 216KHz)	
	L	H	L	256fs (8KHz ≤ fs ≤ 54KHz)	
	L	H	H	256fs (54KHz < fs ≤ 108KHz)	
	H	L	L	Auto (8KHz ≤ fs ≤ 216KHz)	Default
	H	L	H	384fs (8KHz ≤ fs ≤ 54KHz)	
	H	H	L	512fs (8KHz < fs ≤ 54KHz)	
	H	H	H	768fs (8KHz ≤ fs ≤ 54KHz)	
H	L	L	L	128fs (108KHz < fs ≤ 216KHz)	
	L	L	H	192fs (108KHz < fs ≤ 216KHz)	
	L	H	L	256fs (8KHz ≤ fs ≤ 54KHz)	
	L	H	H	256fs (54KHz < fs ≤ 108KHz)	
	H	L	L	384fs (54KHz ≤ fs ≤ 108KHz)	
	H	L	H	384fs (8KHz ≤ fs ≤ 54KHz)	
	H	H	L	512fs (8KHz < fs ≤ 54KHz)	
	H	H	H	768fs (8KHz ≤ fs ≤ 54KHz)	

Table 6. MCLK Frequency Setting of AK5388

TDM1	TDM0	Mode	BICK	
L	L	Normal	48 ~ 128fs	Default
L	H	TDM256	256fs	
H	L	N/A	N/A	
H	H	TDM128	128fs	

Table 7. Mode setting of AK5388

CKS1	CKS0	MCLK	fs	
L	L	128fs	28k ~ 192kHz	
L	H	256fs	28k ~ 108kHz	
H	L	384fs	28k ~ 54kHz	
H	H	512fs	28k ~ 54kHz	Default

Table 8. MCLK Frequency Setting of AK4101A

Note: AK4101A does not support MCLK=768fs.

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW3] (PDN): Resets of AK5388 and AK4101A. Keep “H” during normal operation.

■ Analog input buffer circuit

An analog input buffer circuit example (1st order HPF; fc=0.70Hz, 2nd order LPF; fc=304kHz, gain=-14.5dB) is shown in Figure 2. The analog signal is able to input through XLR or RCA connectors. (For RCA input, jumper should be short. For XLR input, jumper should be open.) The input level of this circuit is +/-15.4Vpp (AK5388: +/-2.9Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=118dB, S/(N+D)=TBDdB.

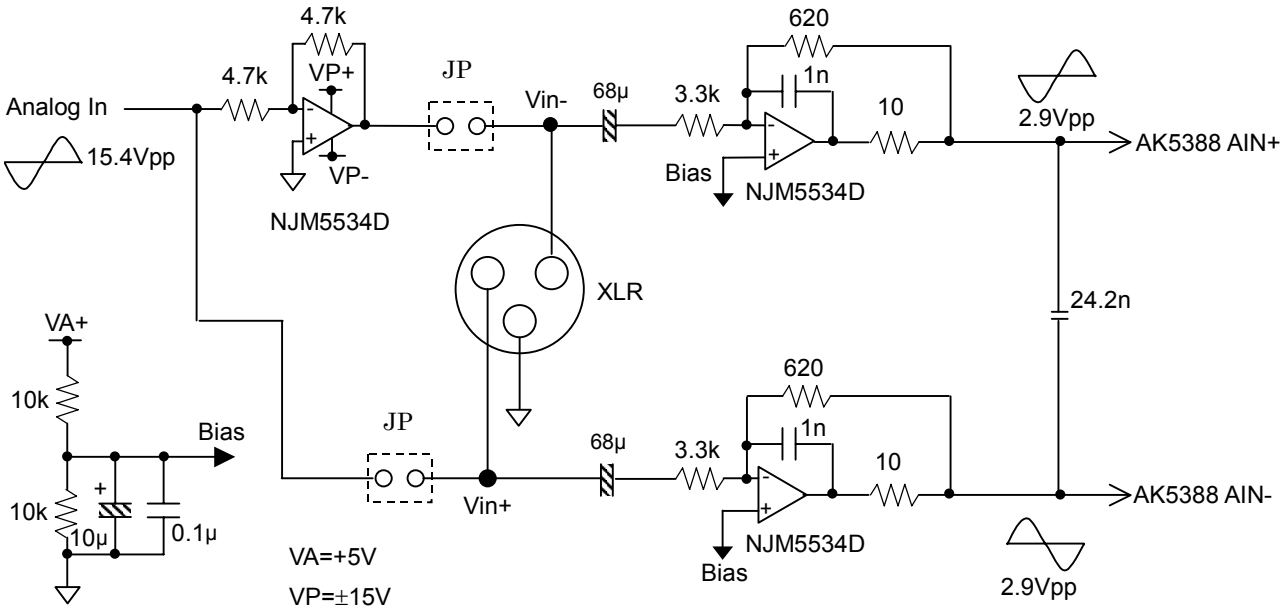


Figure 2. Analog input buffer circuits examples

Fin	1Hz	10Hz
Frequency Response	-1.56dB	-0.02dB

Table 9. Frequency Response of HPF

Fin	20kHz	40kHz	6.144MHz
Frequency Response	-0.005dB	-0.02dB	-15.6dB

Table 10. Frequency Response of LPF

* AKEMD assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- MCLK : 512fs (fs=48kHz), 256fs (fs=96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD = 5.0V(REG), DVDD = 3.3V(REG)
- Interface : DSP Data (10pin Header : PSIA)
- Temperature : Room

[Measurement Results]

Parameter	Result		Unit
	L1ch / R1ch	L2ch / R2ch	
ADC Analog Input Characteristics:			
S/(N+D): Filter=none			
(fs=48kHz, -1dBFS, BW=20kHz)	112.3 / 110.2	110.0 / 111.0	dB
(fs=96kHz, -1dBFS, BW=40kHz)	108.8 / 107.4	107.4 / 107.9	dB
(fs=192kHz, -1dBFS, BW=40kHz)	108.8 / 107.4	107.3 / 108.3	dB
D-Range: Filter=A-weighted			
(fs=48kHz, -60dBFS, BW=20kHz)	120.0 / 119.9	119.9 / 120.0	dB
(fs=96kHz, -60dBFS, BW=40kHz)	119.4 / 119.5	119.5 / 119.5	dB
(fs=192kHz, -60dBFS, BW=40kHz)	119.5 / 119.7	119.6 / 119.6	dB
S/N: Filter=A-weighted			
(fs=48kHz, -60dBFS, BW=20kHz)	120.2 / 120.0	120.1 / 120.1	dB
(fs=96kHz, -60dBFS, BW=40kHz)	119.3 / 119.5	119.5 / 119.4	dB
(fs=192kHz, -60dBFS, BW=40kHz)	119.5 / 119.6	119.7 / 119.6	dB
S/N MONO mode: Filter=A-weighted			
(fs=48kHz, BW=20kHz)	123.0 / 123.0	123.1 / 123.1	dB
(fs=96kHz, BW=40kHz)	122.4 / 122.5	122.5 / 122.5	dB
(fs=192kHz, BW=40kHz)	122.6 / 122.6	122.6 / 122.6	dB

[ADC Plot: fs=48kHz]

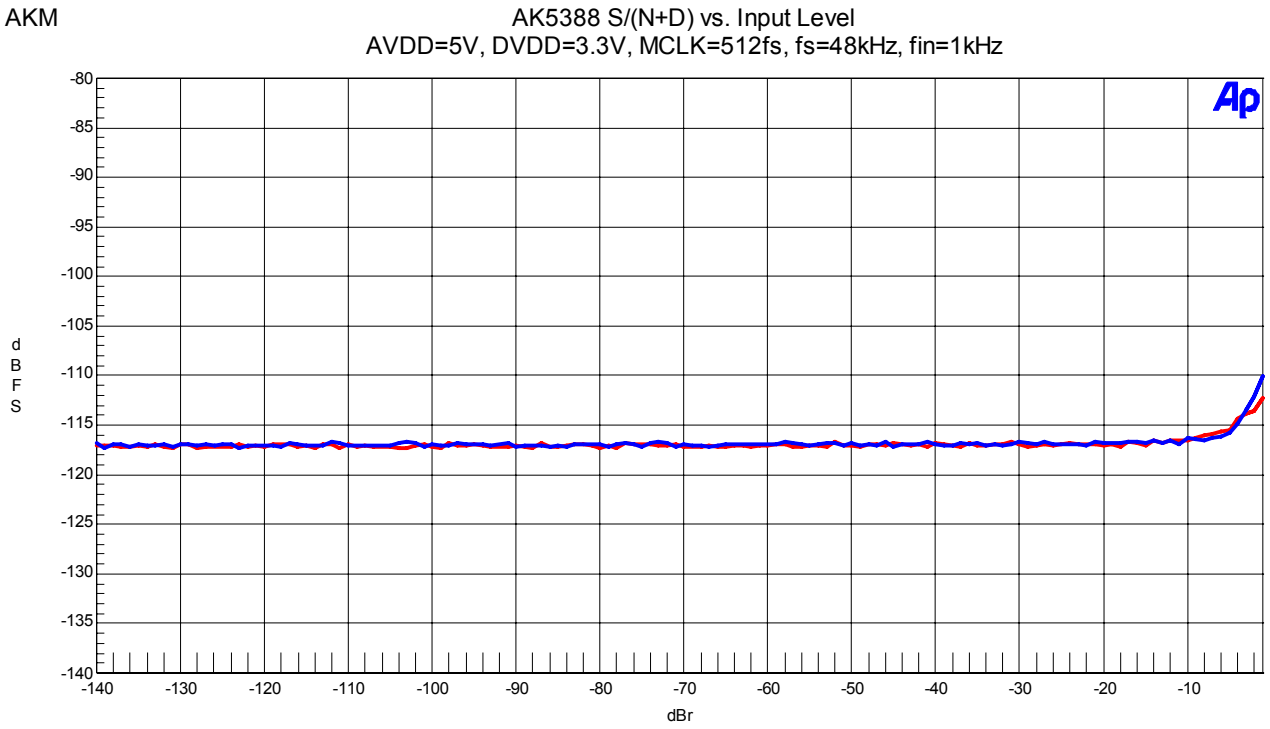


Figure 3. S/(N+D) vs. Input Level

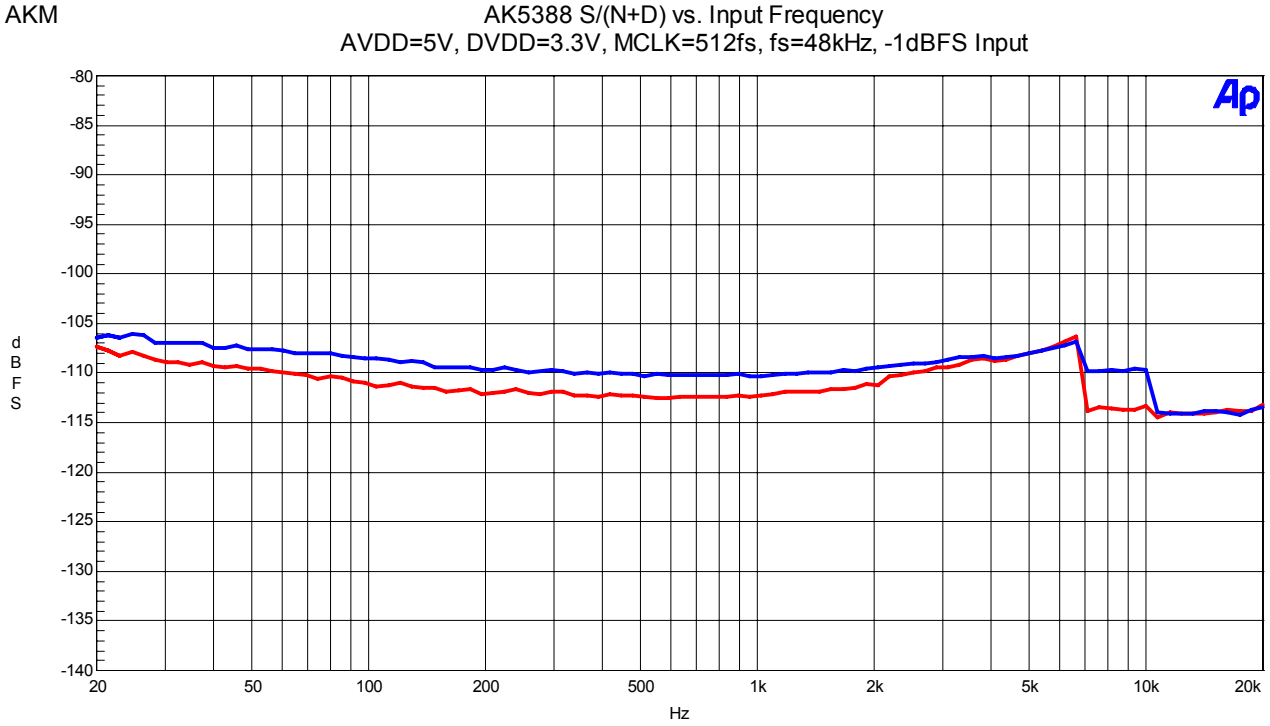


Figure 4. S/(N+D) vs. Input Frequency

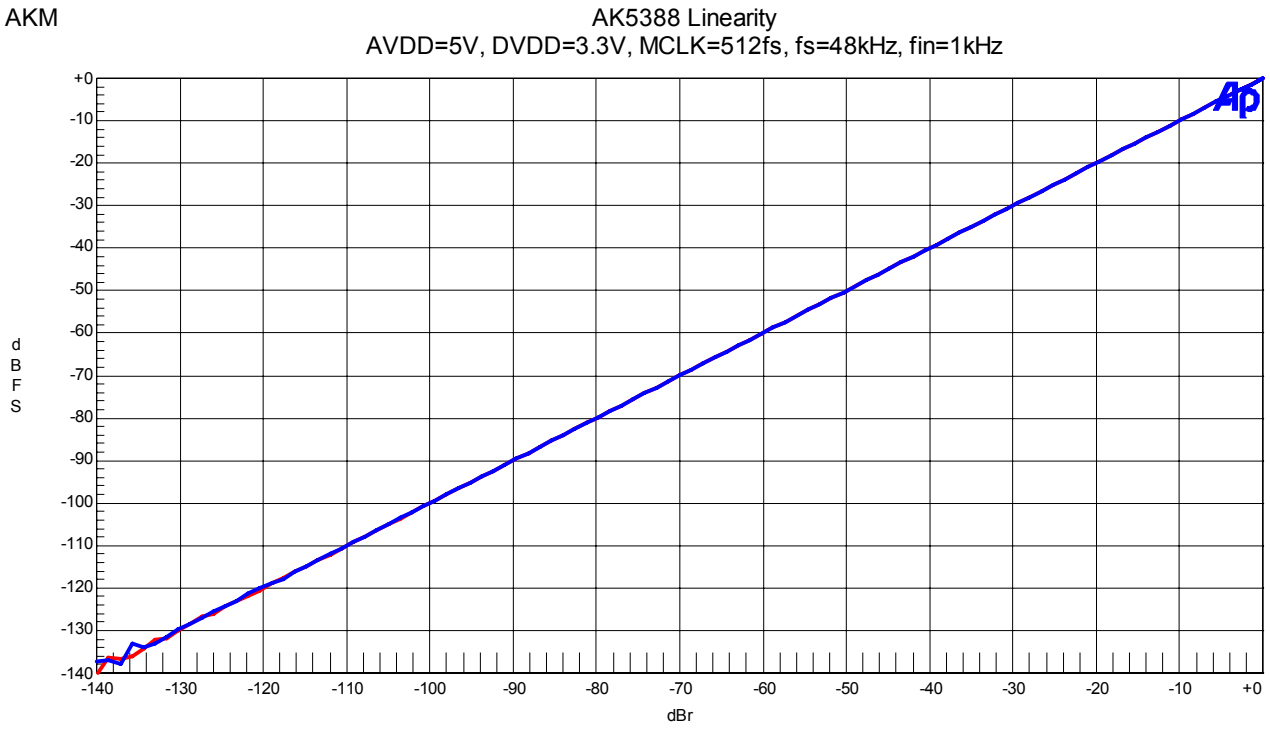


Figure 5. Linearity

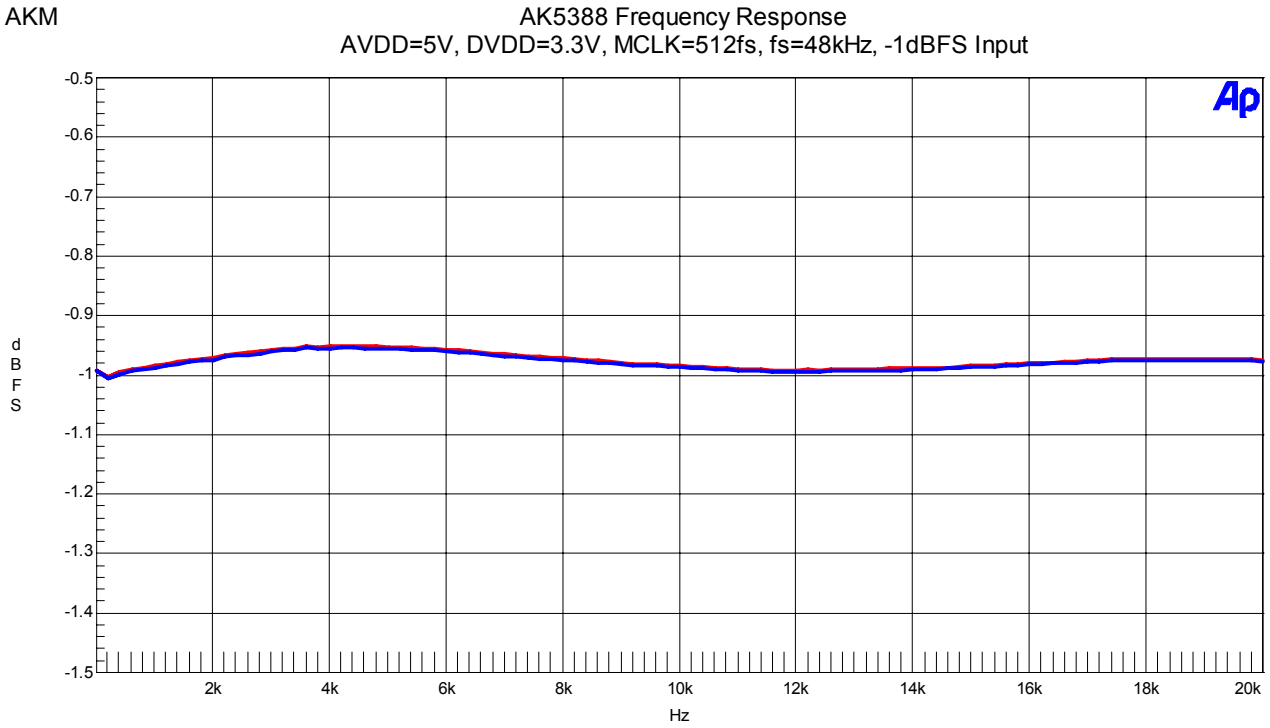


Figure 6. Frequency Response

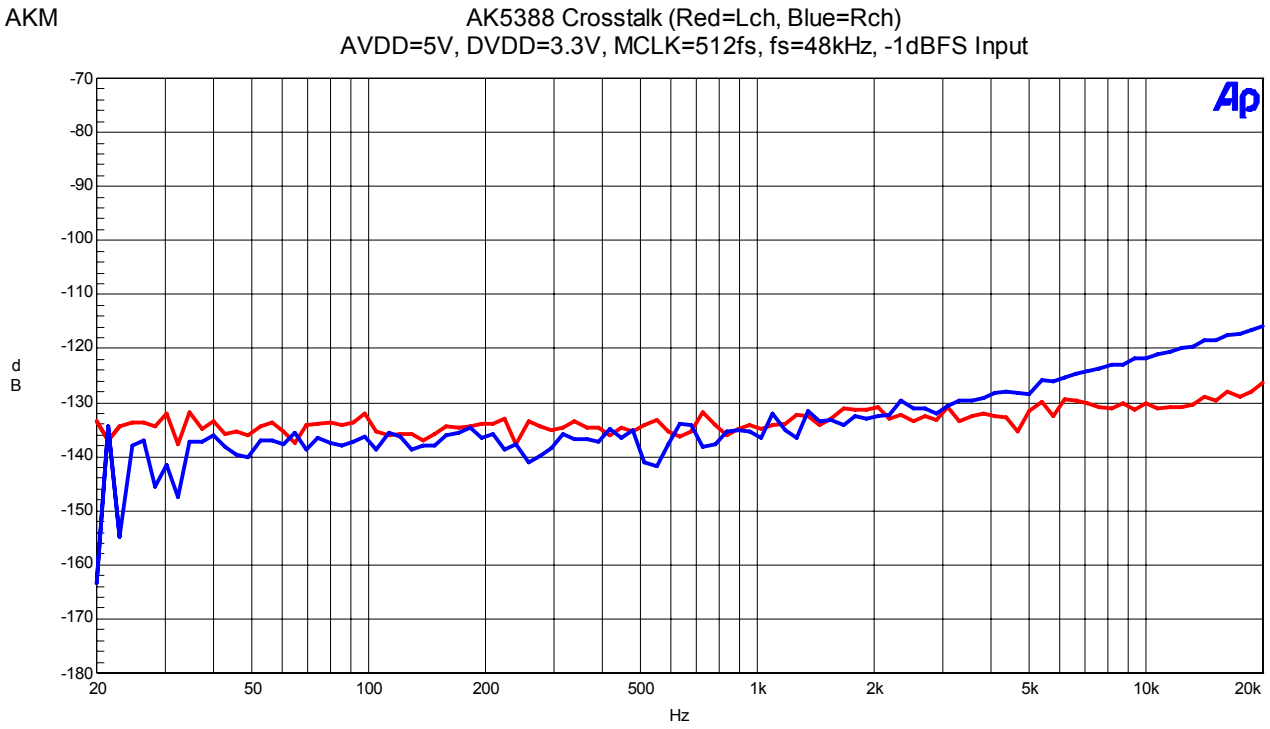


Figure 7. Crosstalk

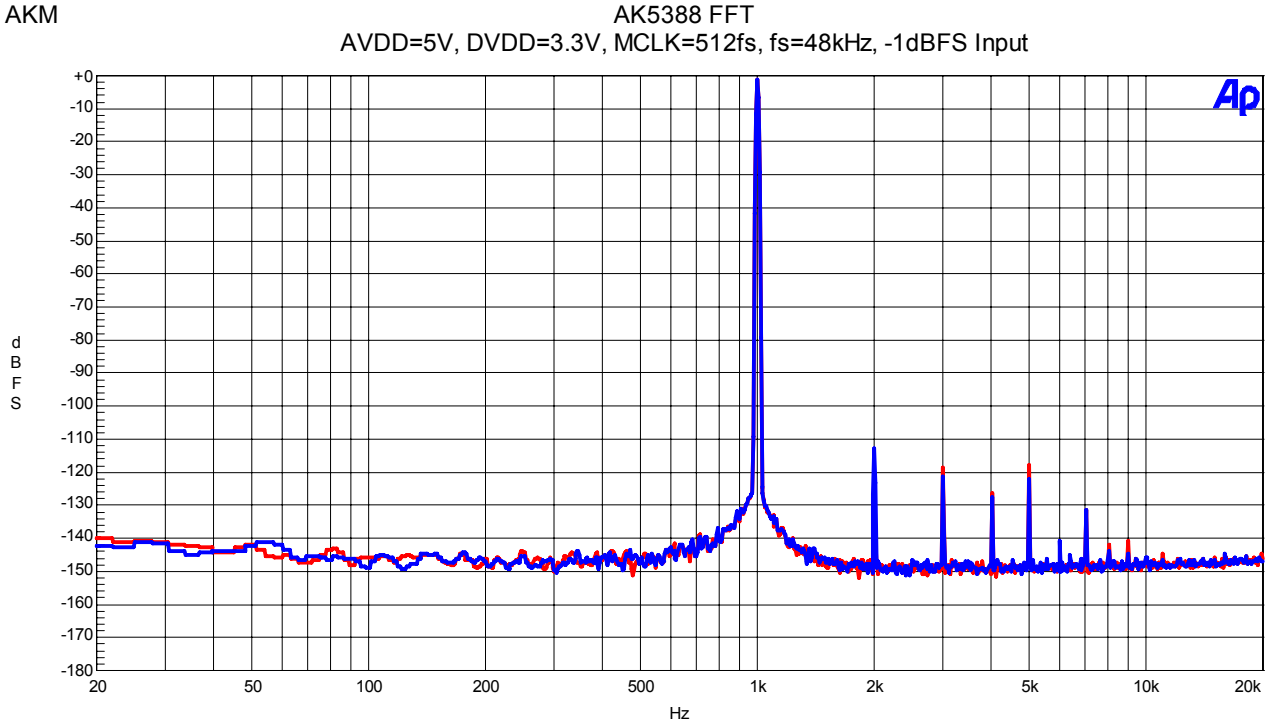


Figure 8. FFT Plot

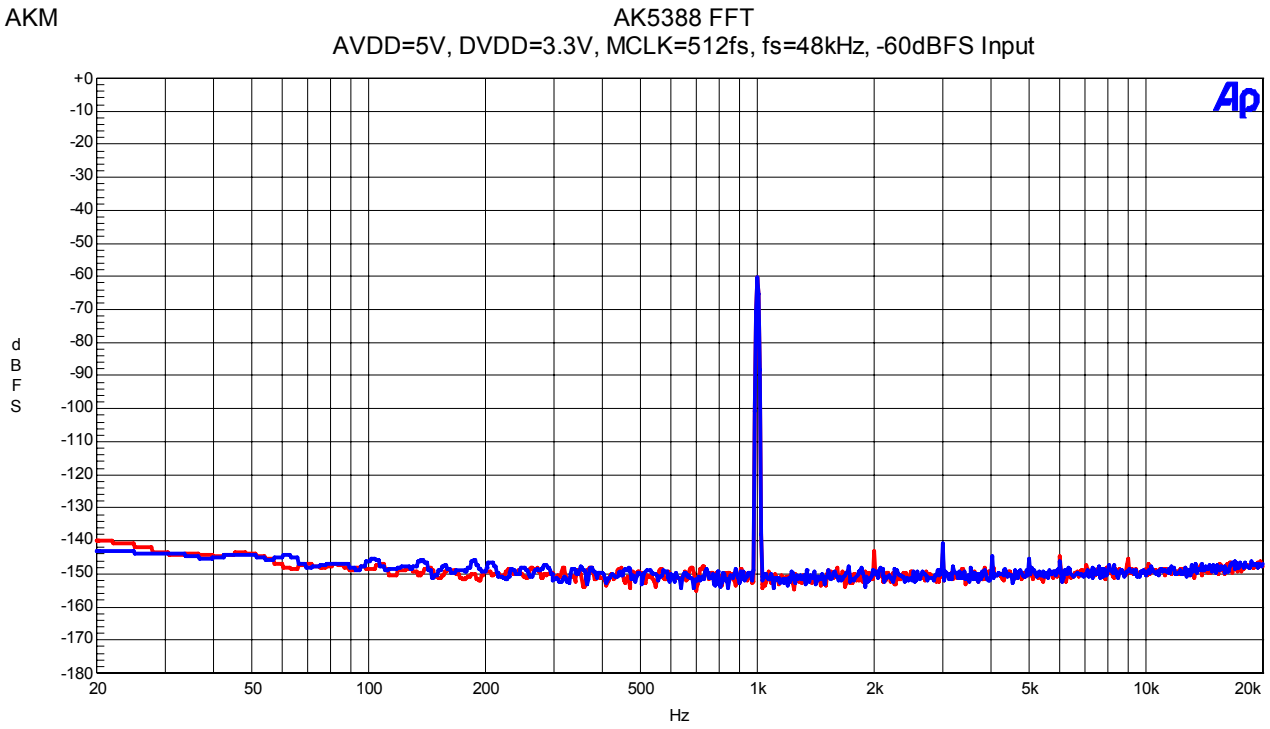


Figure 9. FFT Plot

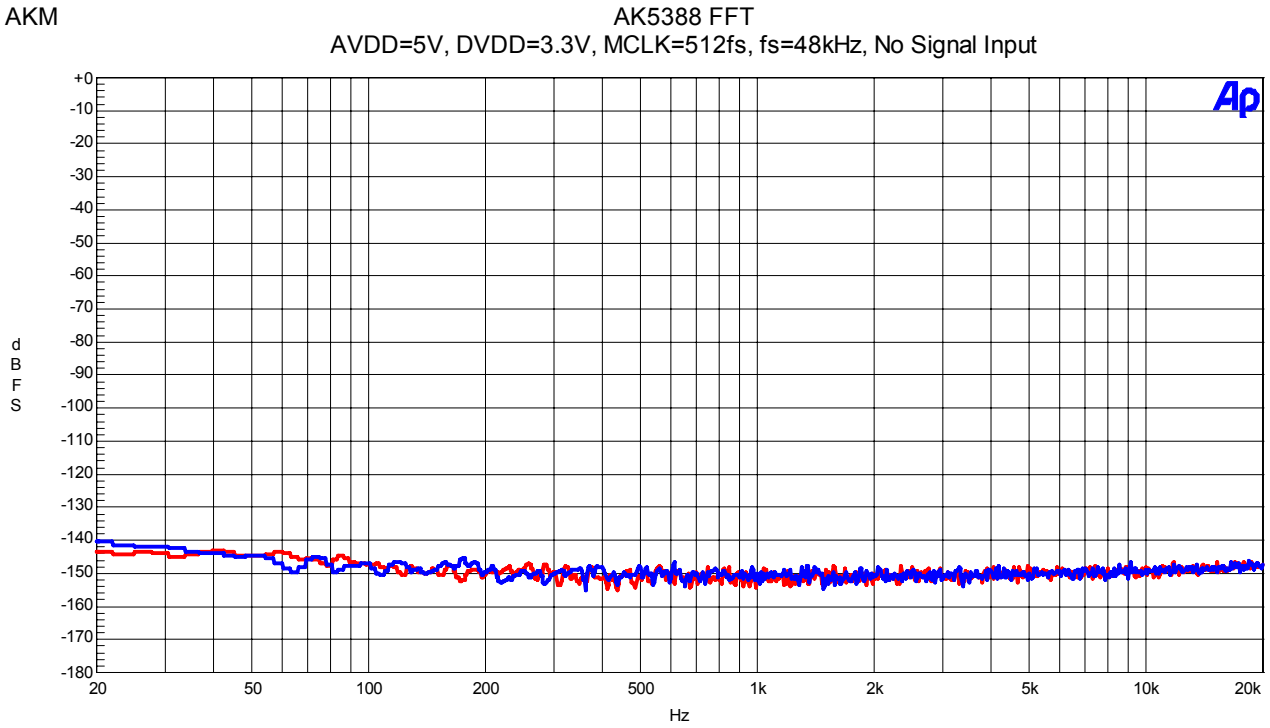


Figure 10. FFT Plot

[ADC Plot: fs=96kHz]

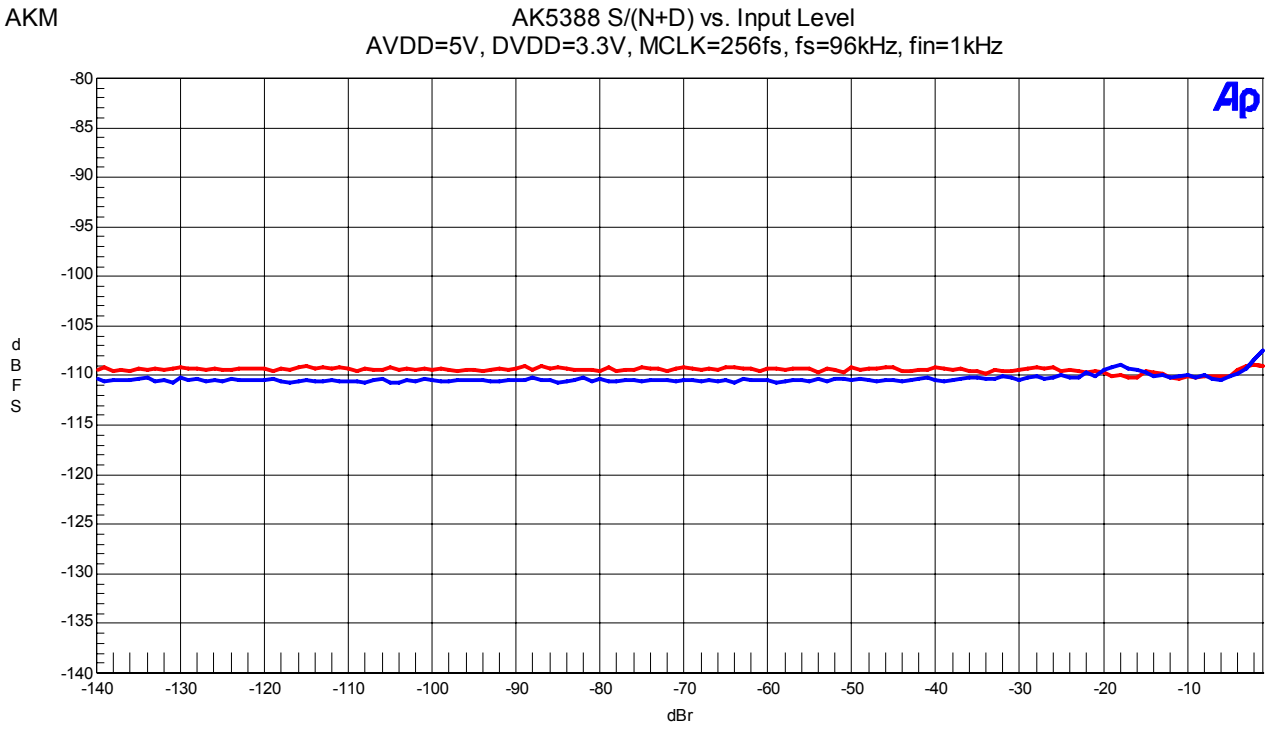


Figure 11. S/(N+D) vs. Input Level

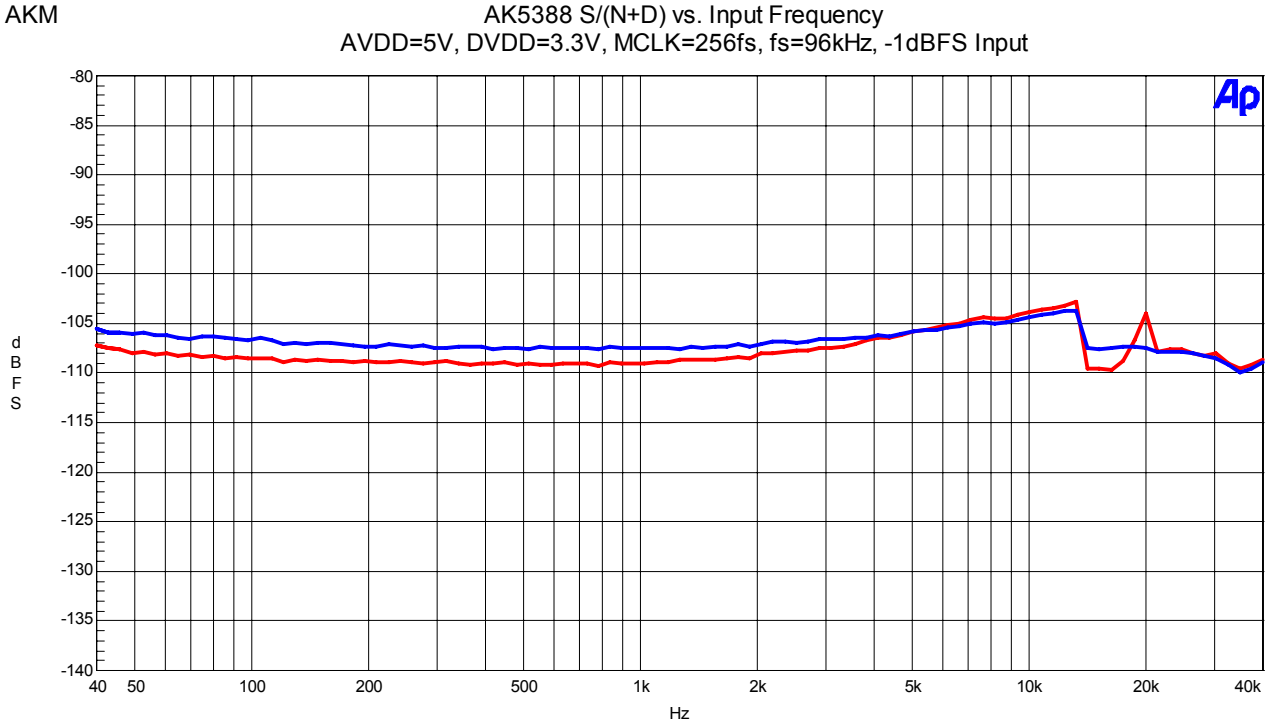


Figure 12. S/(N+D) vs. Input Frequency

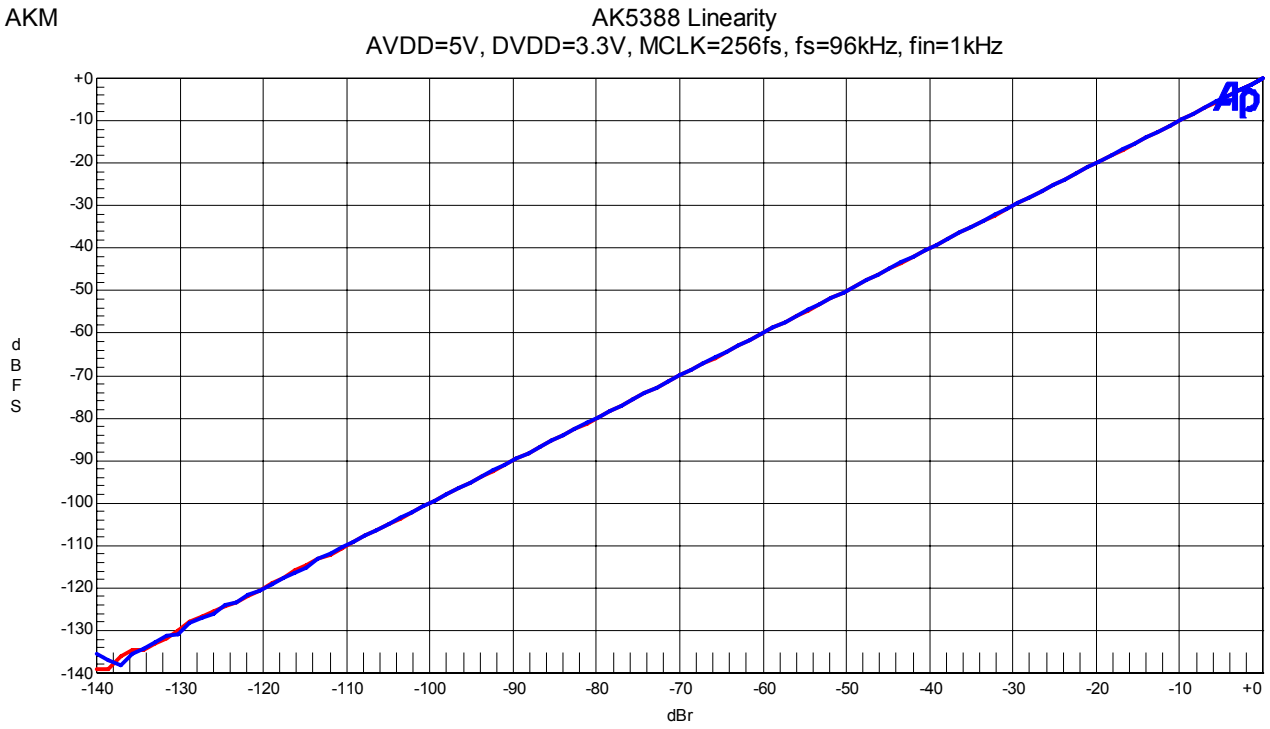


Figure 13. Linearity

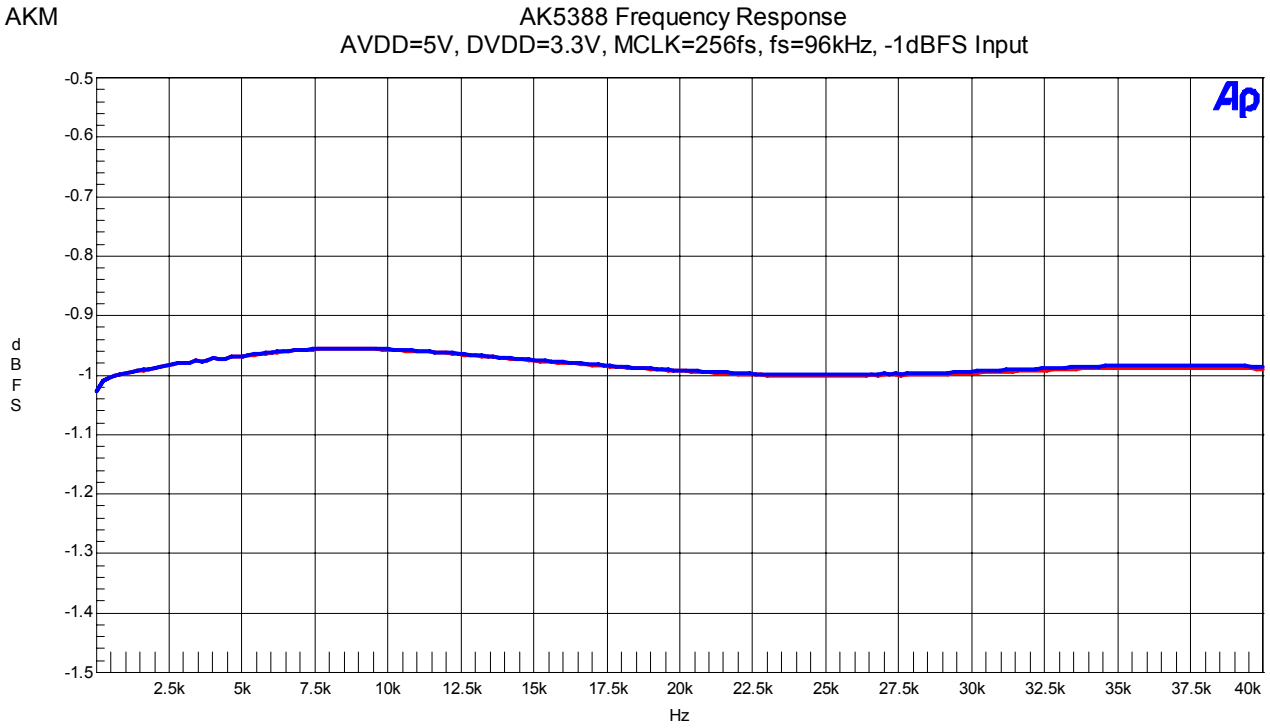


Figure 14. Frequency Response

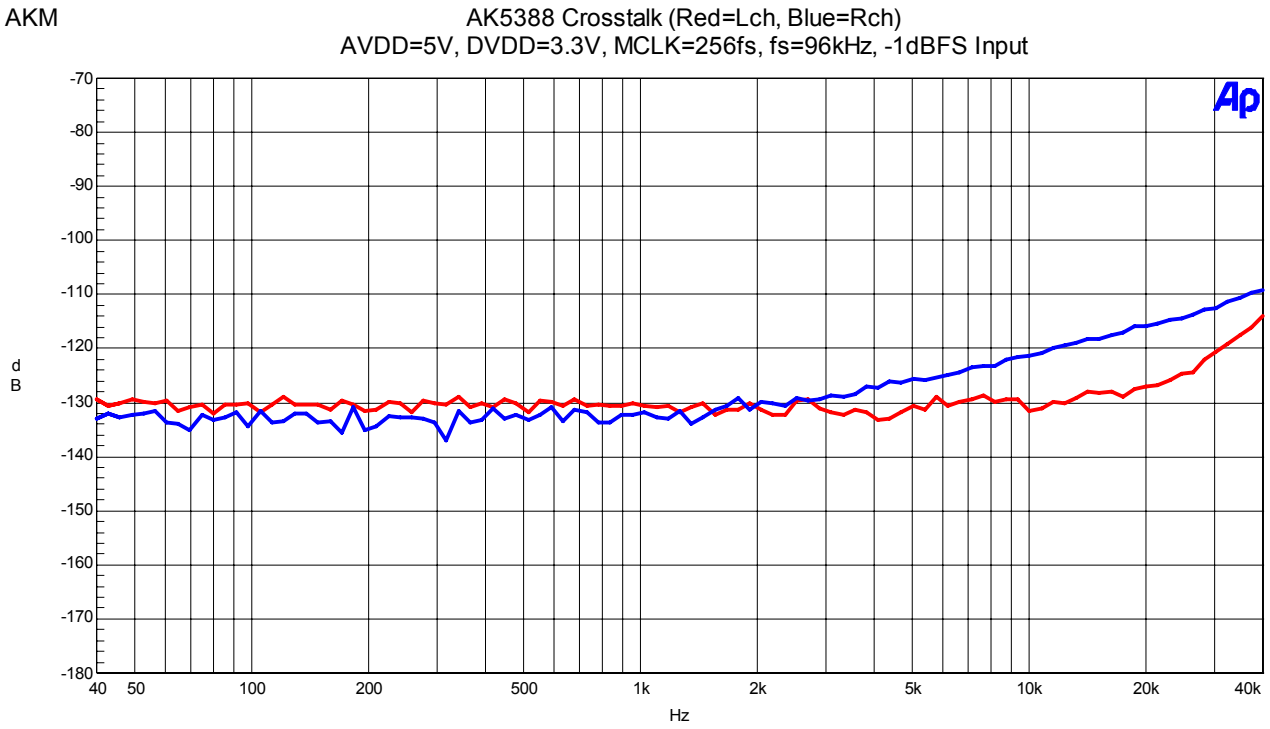


Figure 15. Crosstalk

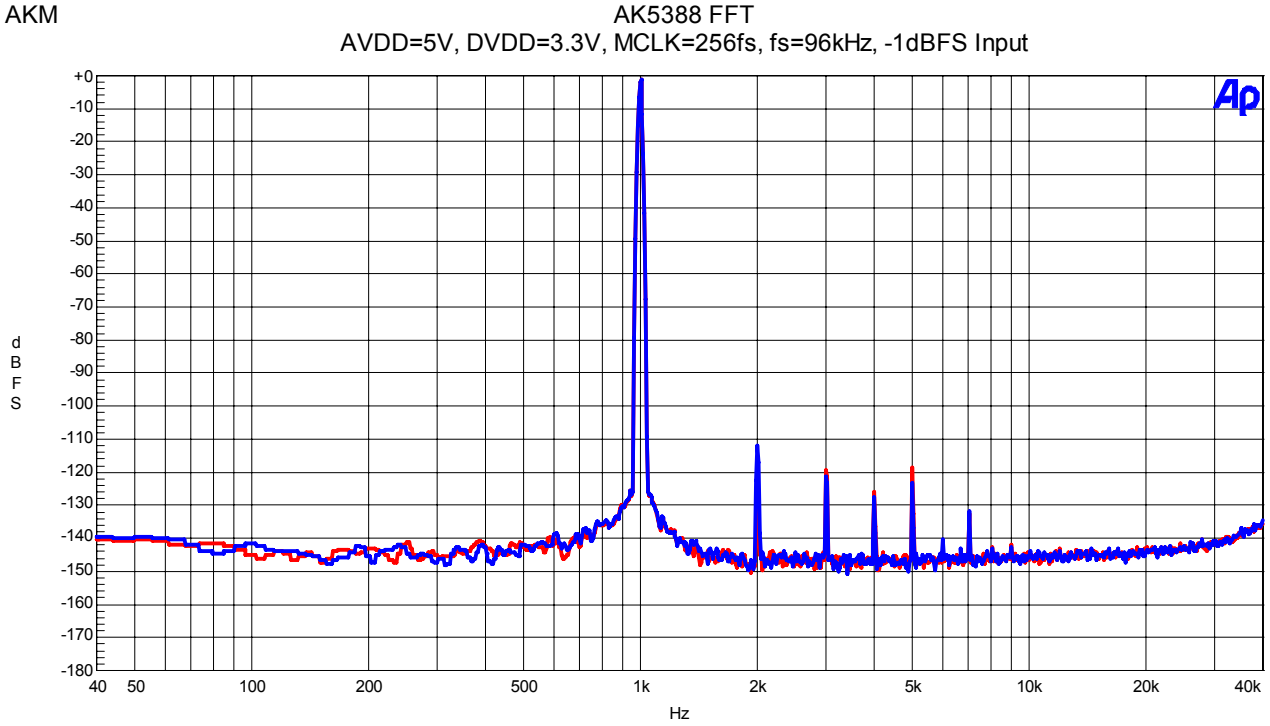


Figure 16. FFT Plot

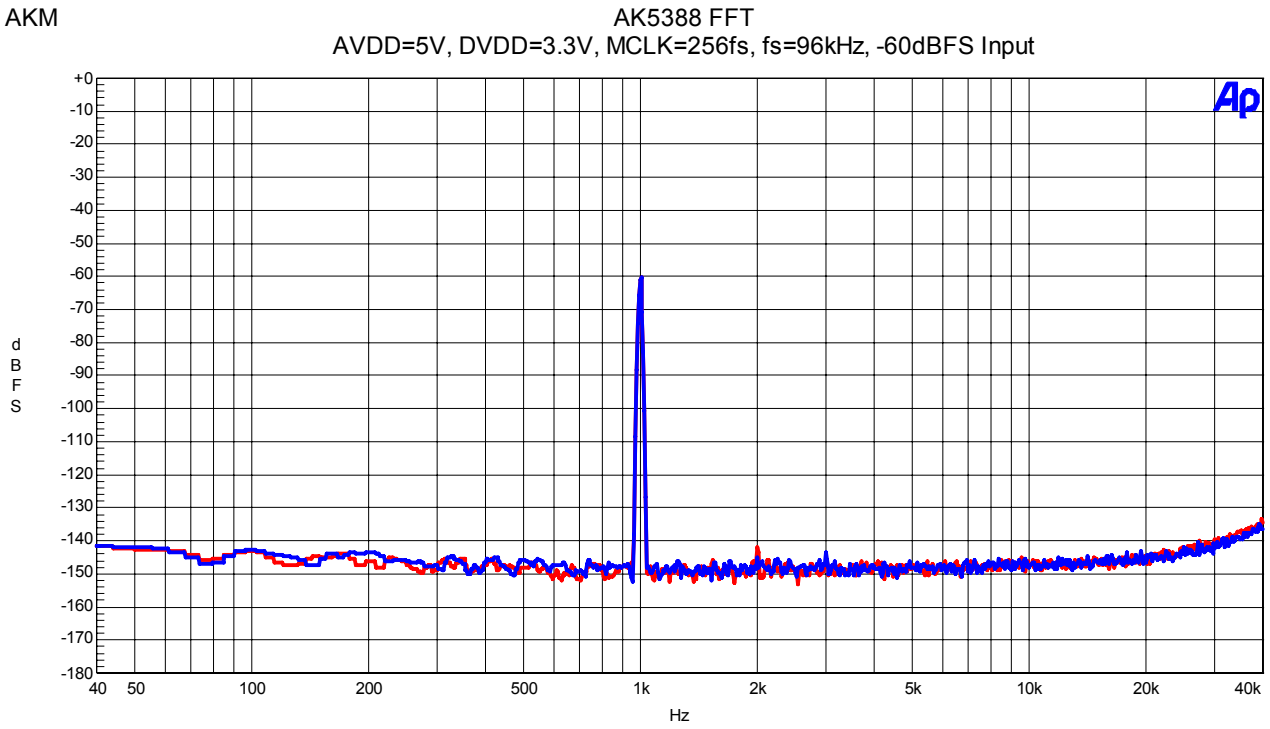


Figure 17. FFT Plot

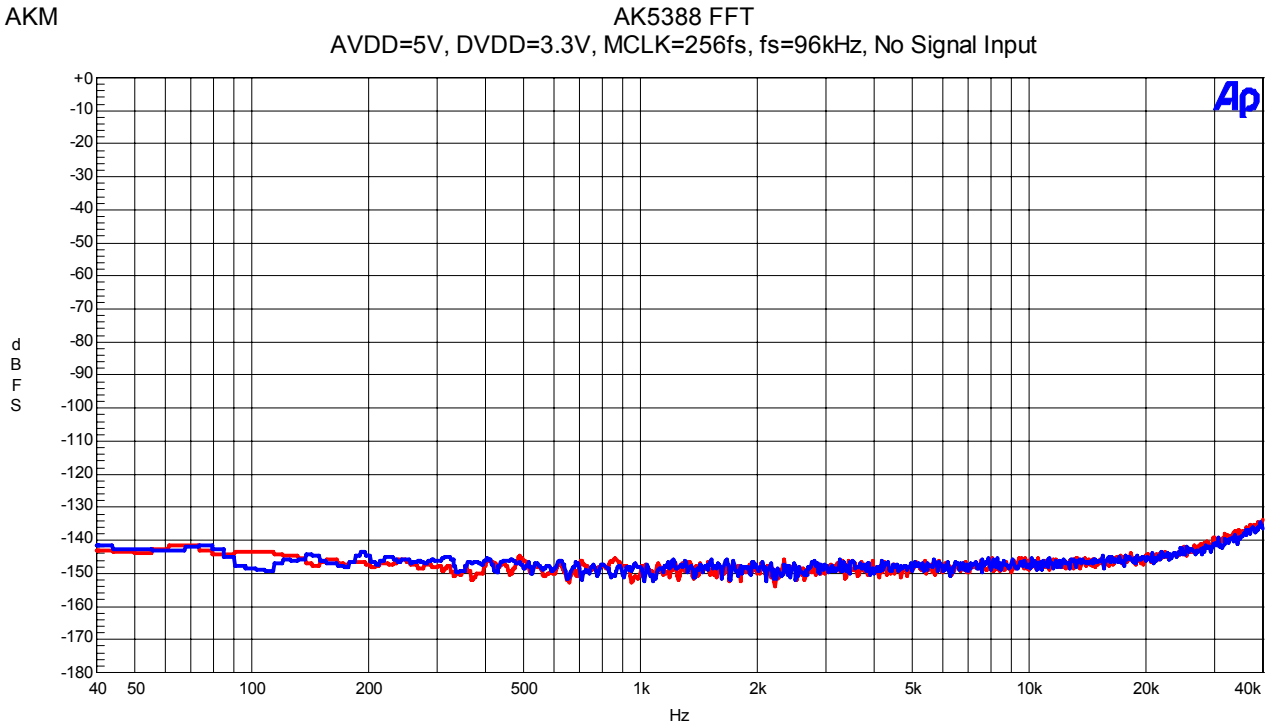


Figure 18. FFT Plot

[ADC Plot: fs=192kHz]

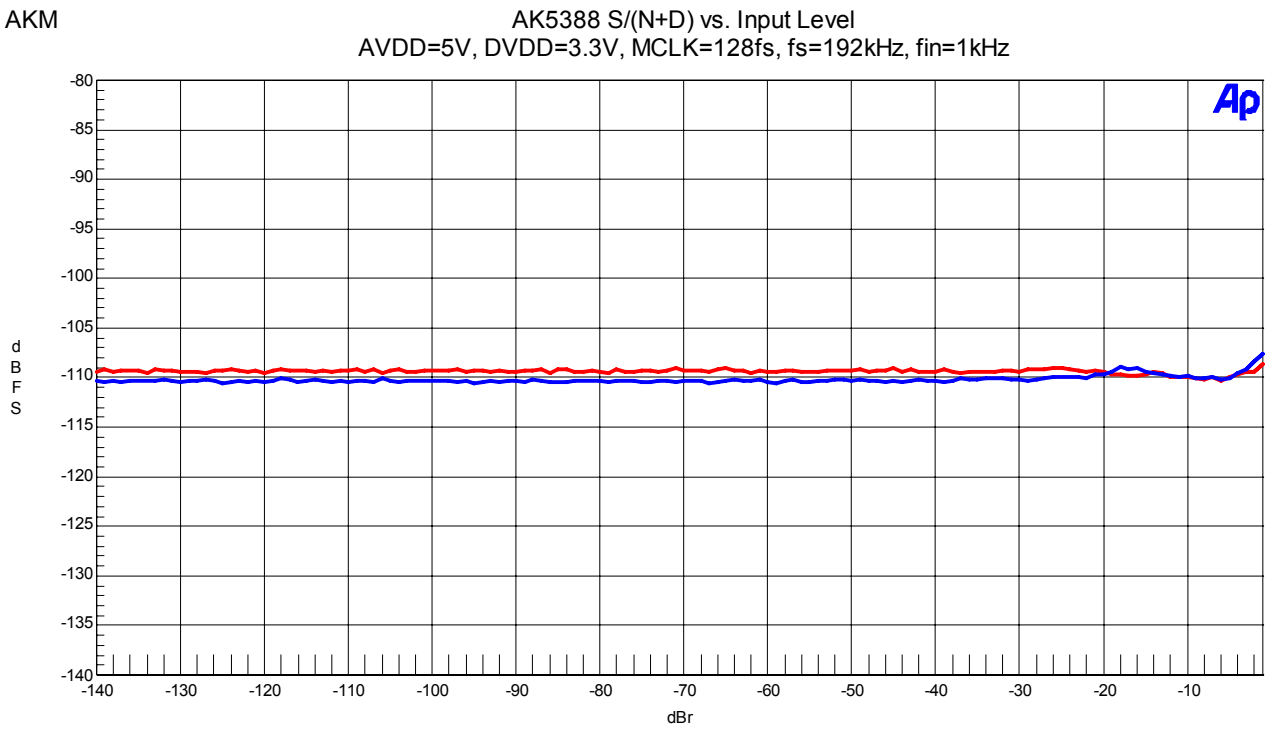


Figure 19. S/(N+D) vs. Input Level

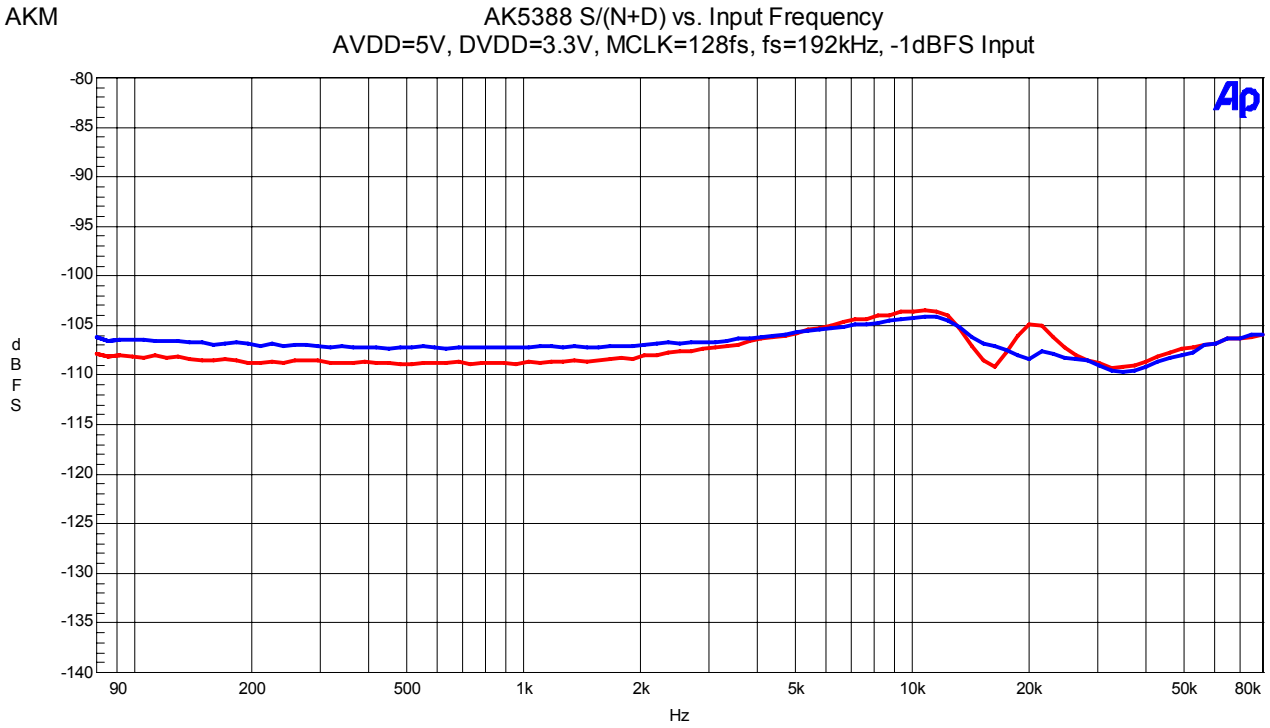


Figure 20. S/(N+D) vs. Input Frequency

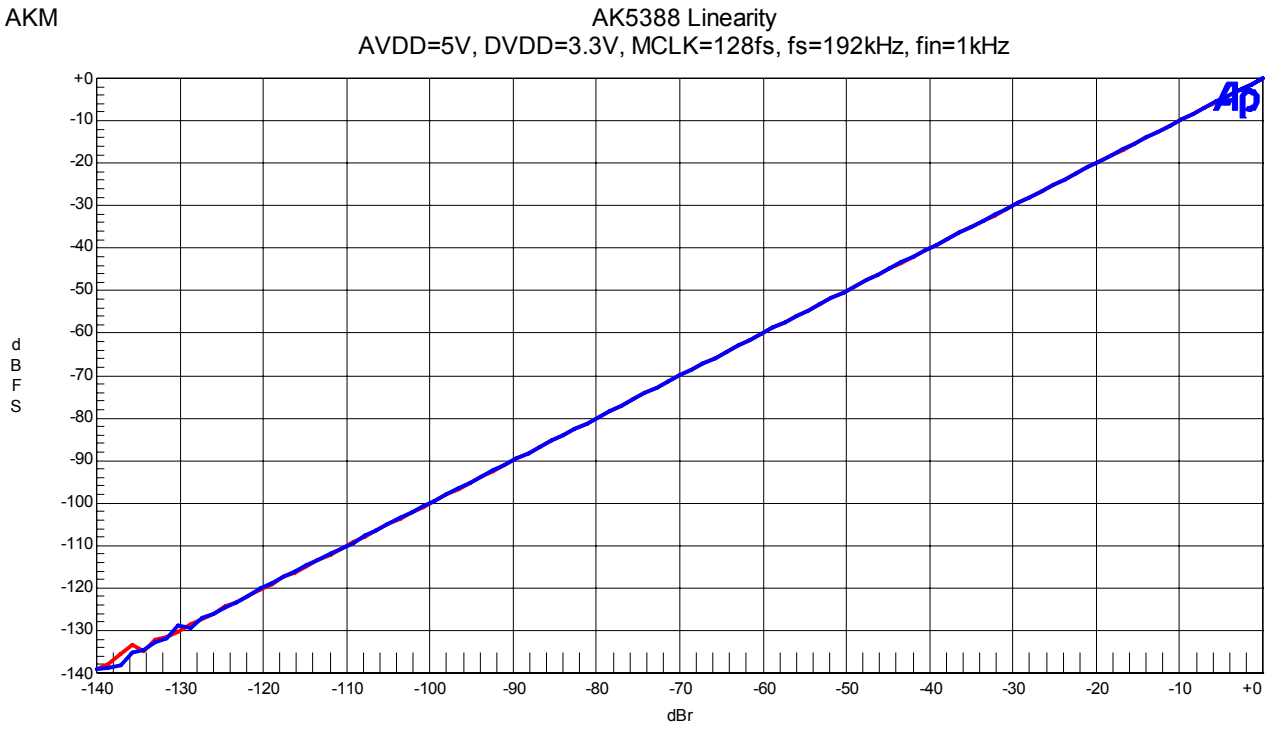


Figure 21. Linearity

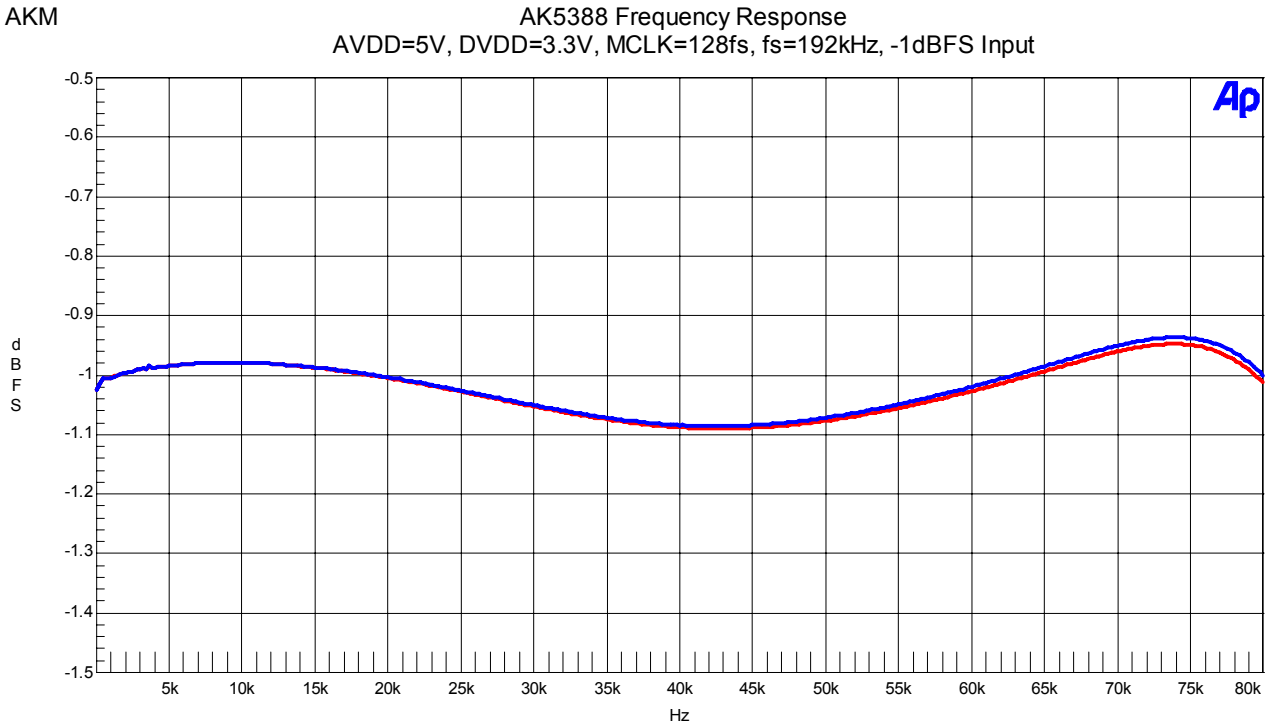


Figure 22. Frequency Response

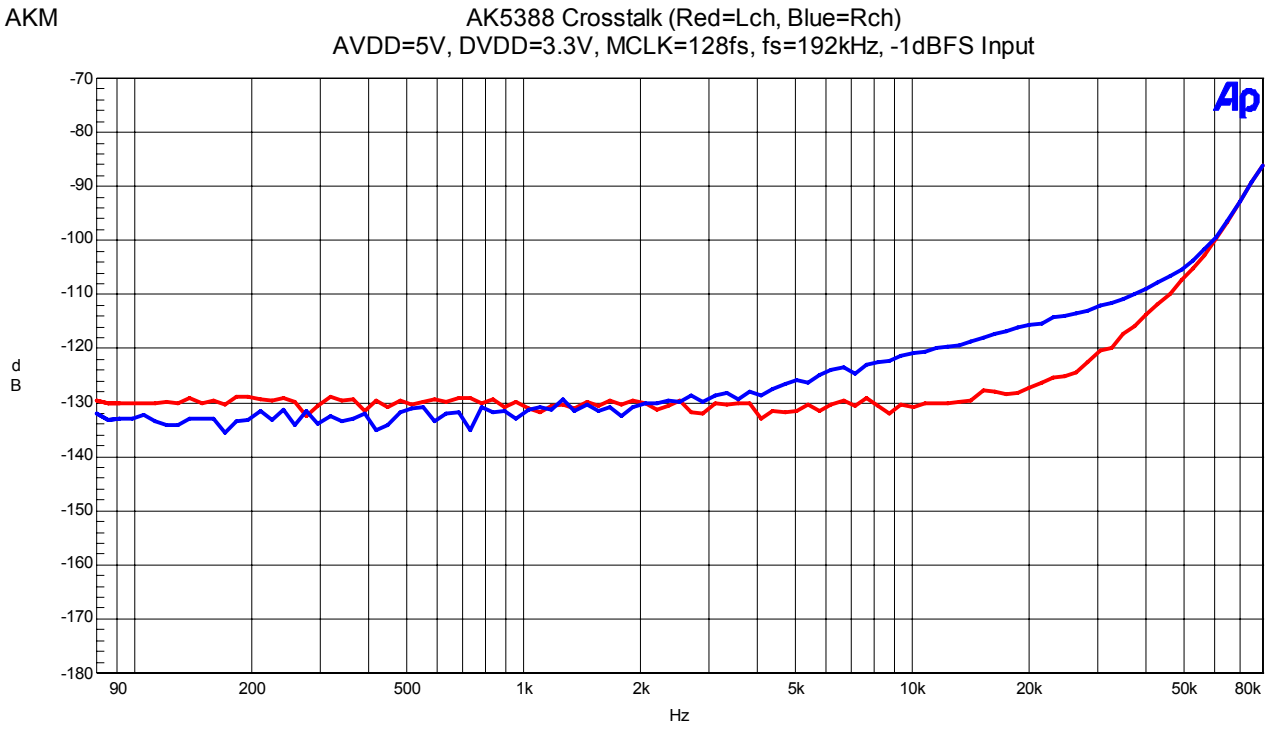


Figure 23. Crosstalk

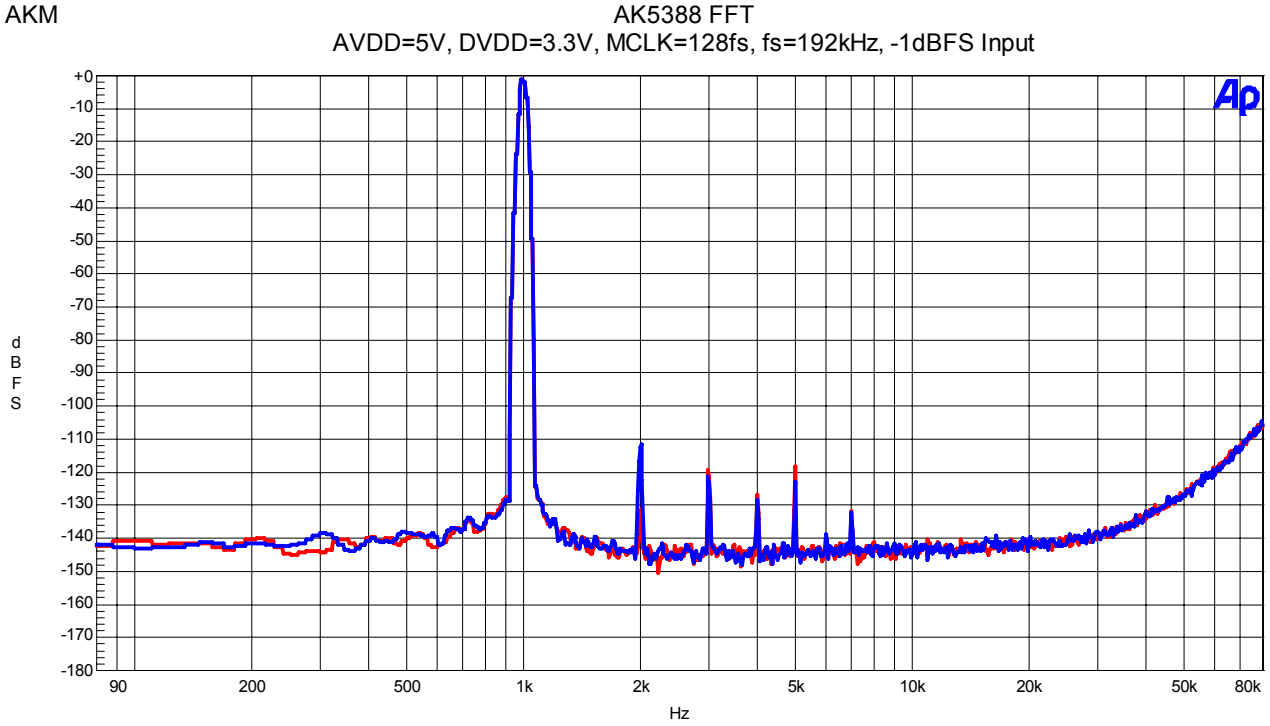


Figure 24. FFT Plot

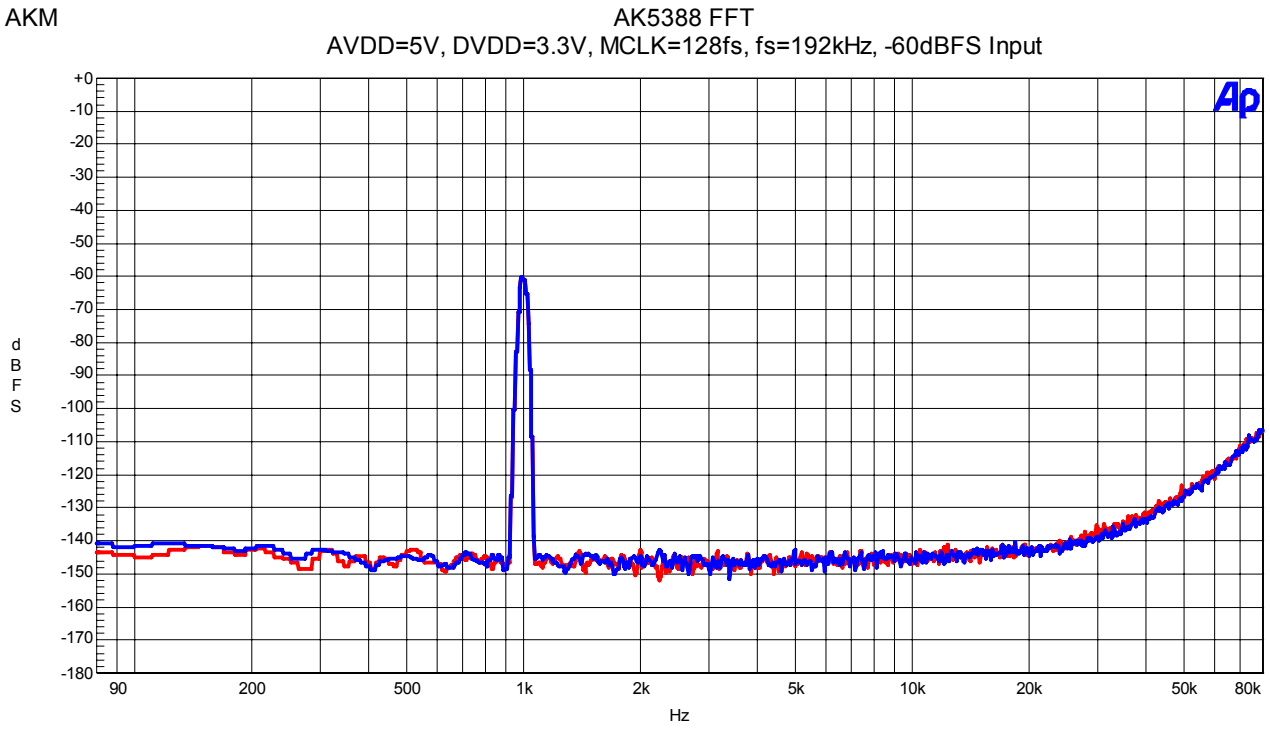


Figure 25. FFT Plot

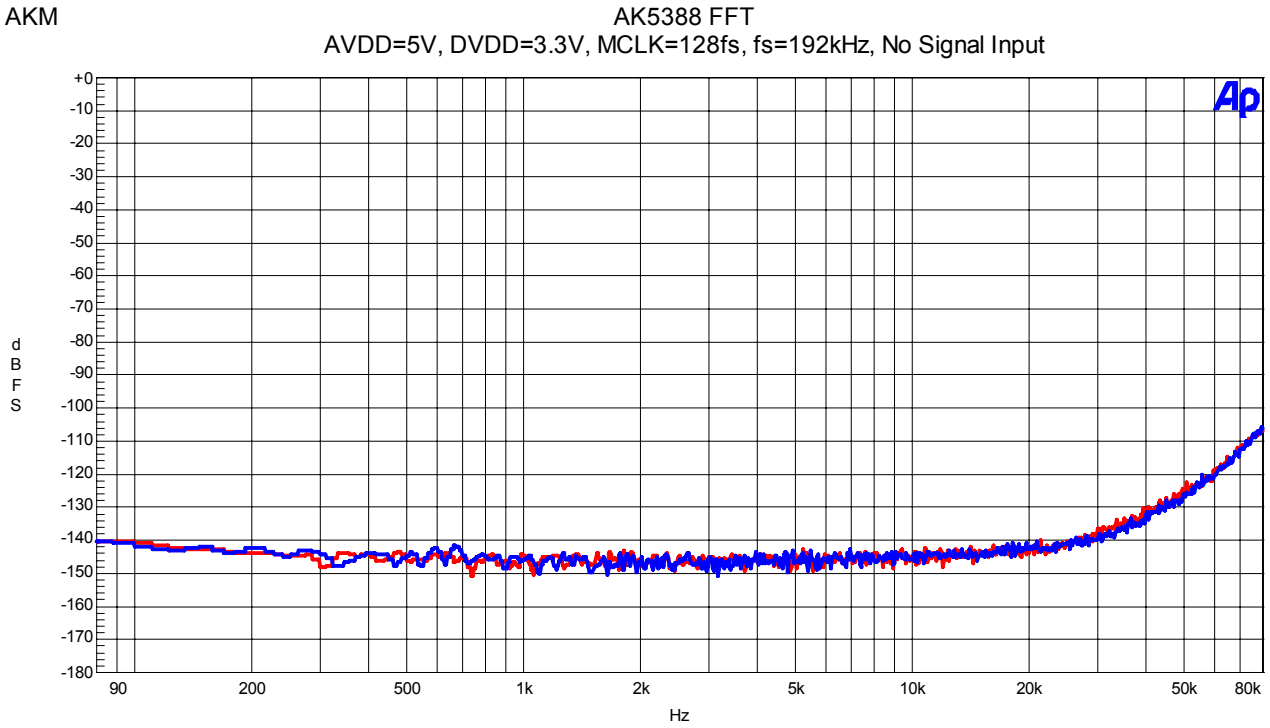
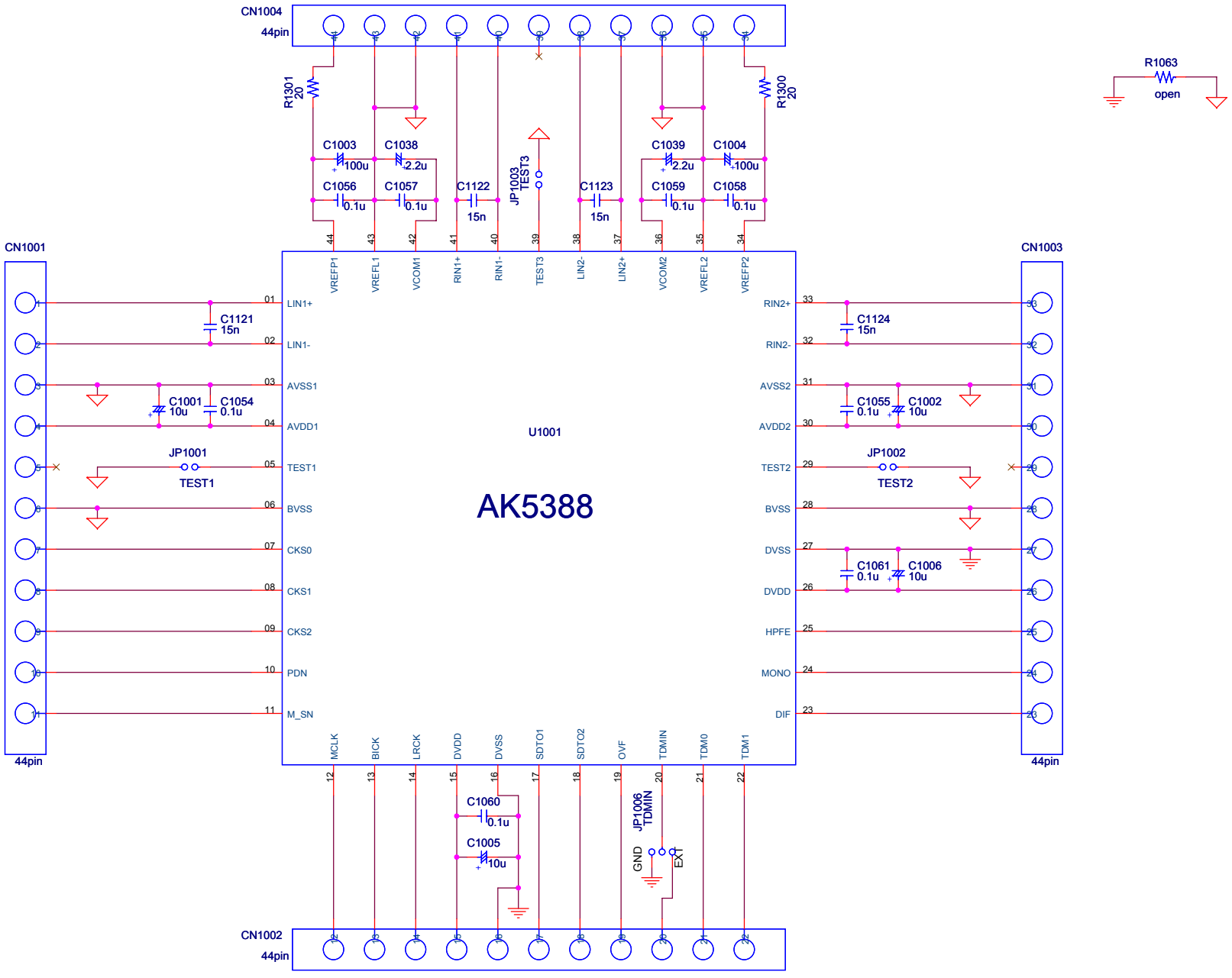


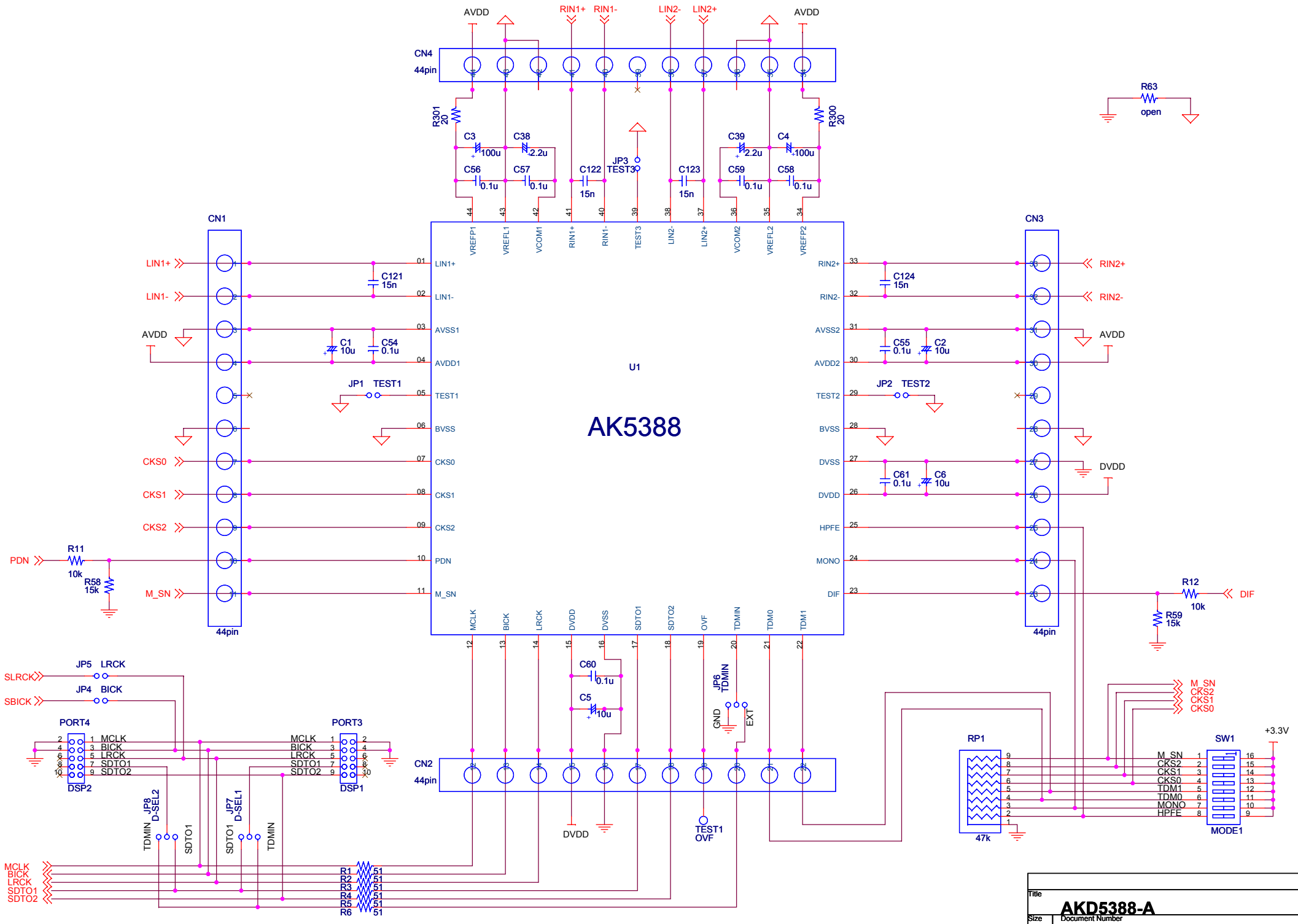
Figure 26. FFT Plot

Revision History

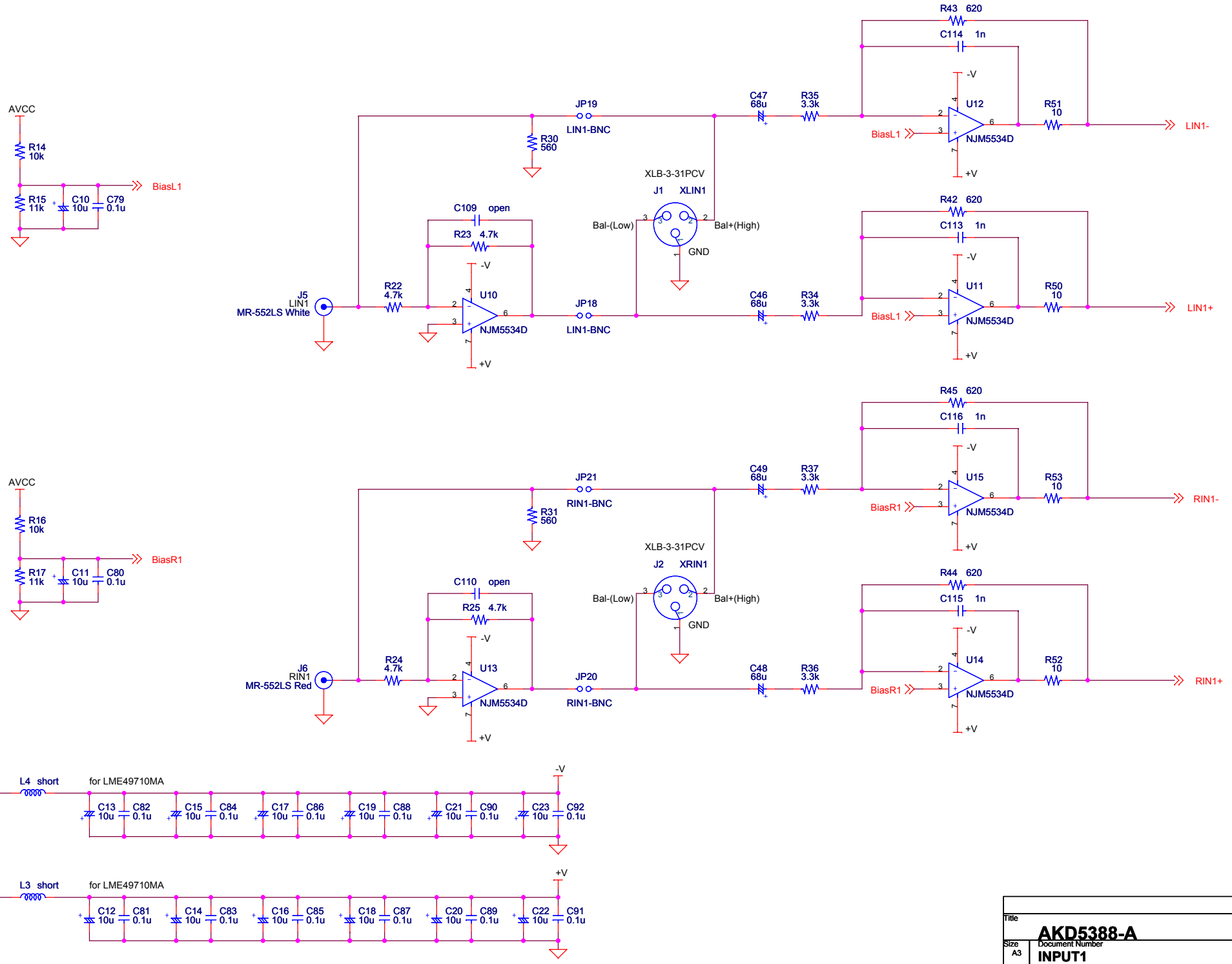
Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
07/06/27	KM090200	0	First Edition		
08/02/12	KM090201	1	Change		Device revision was changed. Rev. A -> Rev. C
			Change	8	Circuit diagram was changed. R: 91ohm -> 10ohm, OP-amp: LME49710-> NJM5534D PORT1, PORT2: TOTX197-> TOTX176
			Modification	9-21	Update of measurement results
08/07/07	KM090202	2	Change		Device revision was changed. Rev. C -> Rev. D
			Modification	9-21	Update of measurement results
08/11/04	KM090203	3	Change		Device revision was changed. Rev. D -> Rev. E
			Change		Circuit diagram was changed. R300, R301:Add 20ohm, C300, C301:Add 220pF. R1300, R1301:Add 20ohm, C1300, C1301:Add 220pF.
			Modification	9-21	Update of measurement results
09/01/05	KM090204	3	Modification	10,14, 18	Update of Plots. Figure 3, Figure 11, Figure 19
09/03/02	KM090205	4	Modification	9-21	Update of measurement results
			Change		Circuit diagram was changed. C300,C301,C1300,C1301:Deleted C121,C122,C123,C124,C1121,C1122,C1123,C1124 :24.2nF -> 15nF C3,C4,C1003,C1004: 10uF -> 100uF R15,R17,R19,R21: 10kohm -> 11kohm



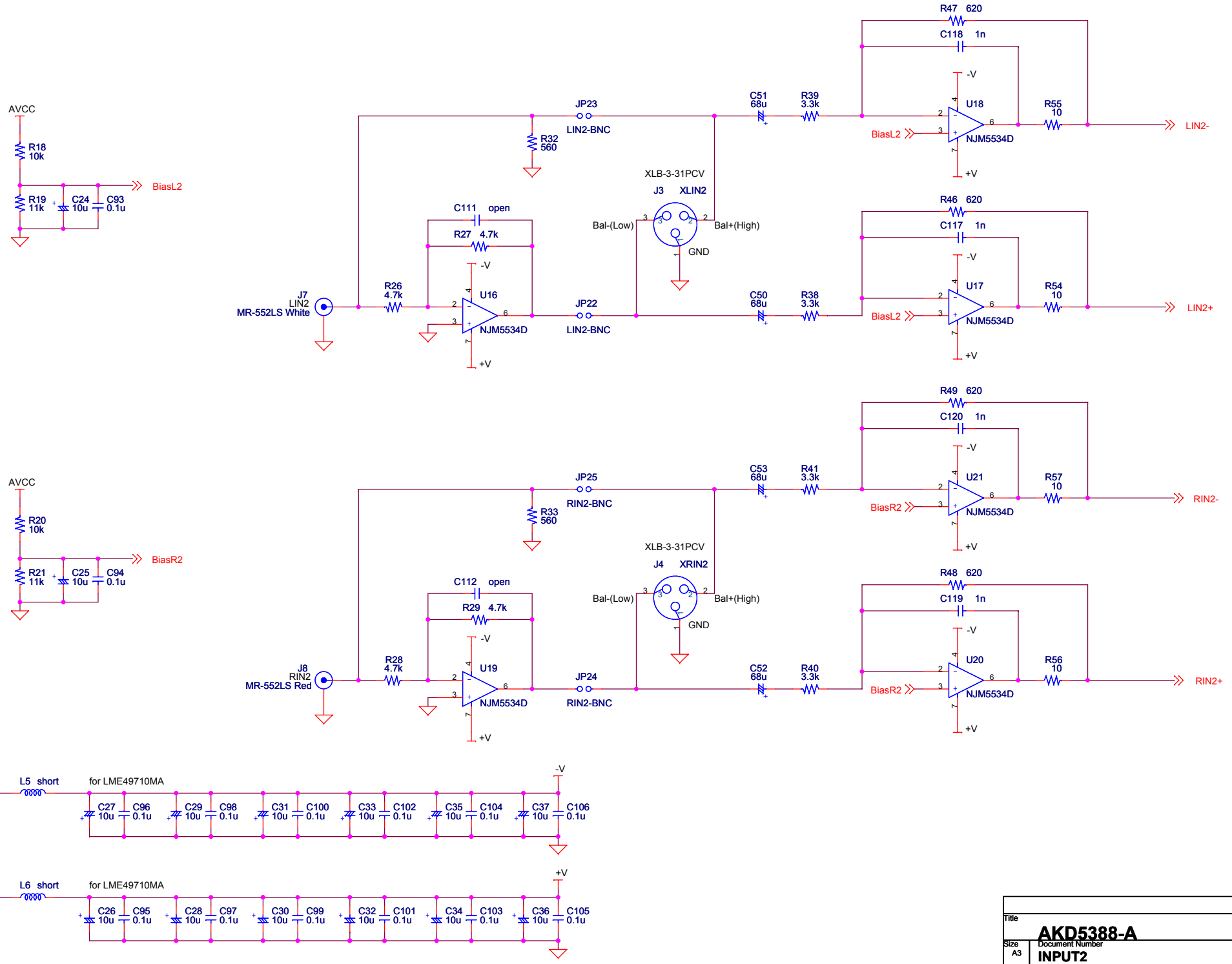
Title	AKD5388-A 44LQFP-SUB	
Size A3	Document Number AK5388	Rev 4
Date: Thursday, February 12, 2009	Sheet 1 of 1	



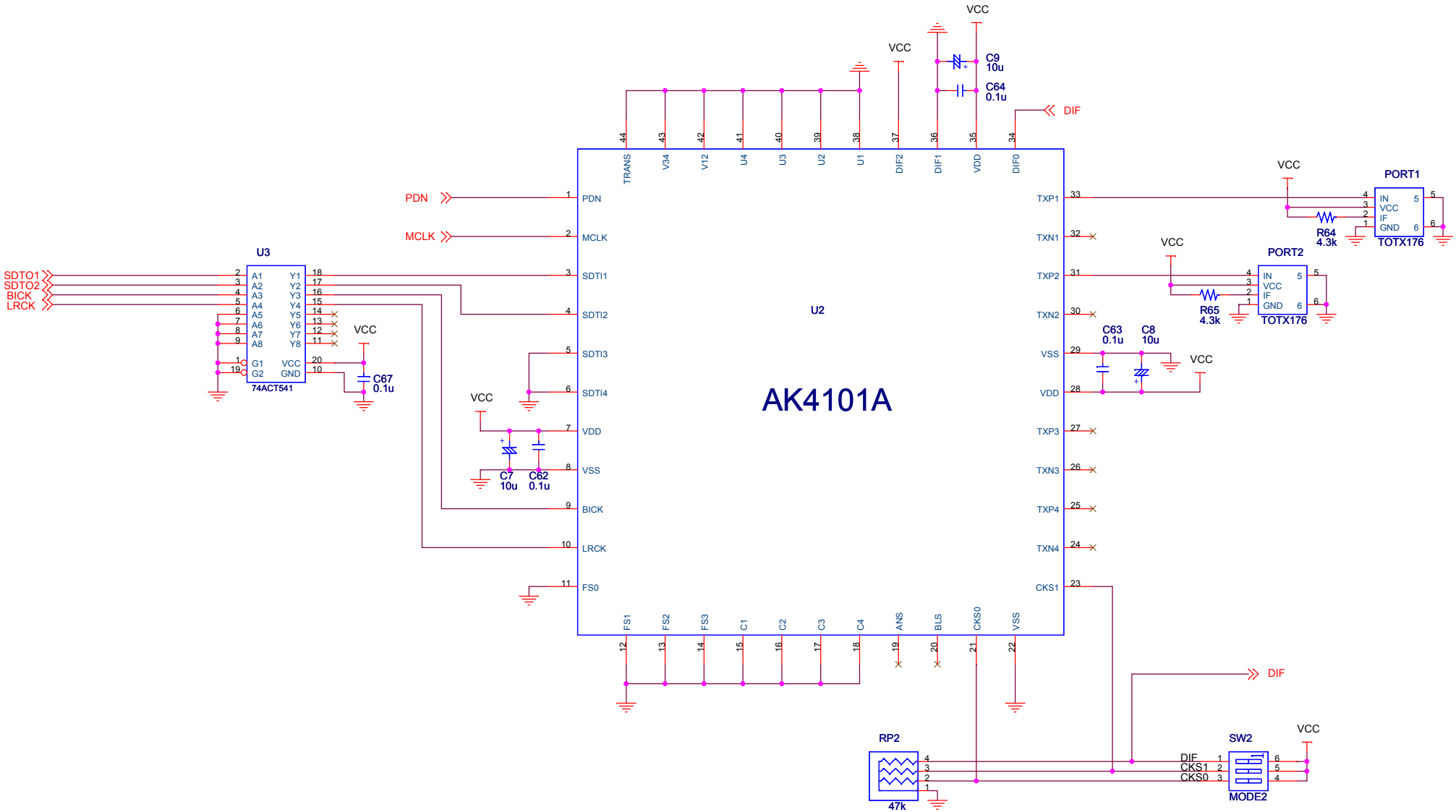
Title	AKD5388-A		
Size A3	Document Number AK5388		Rev 4
Date: Thursday, February 12, 2009	Sheet 1 of 5		



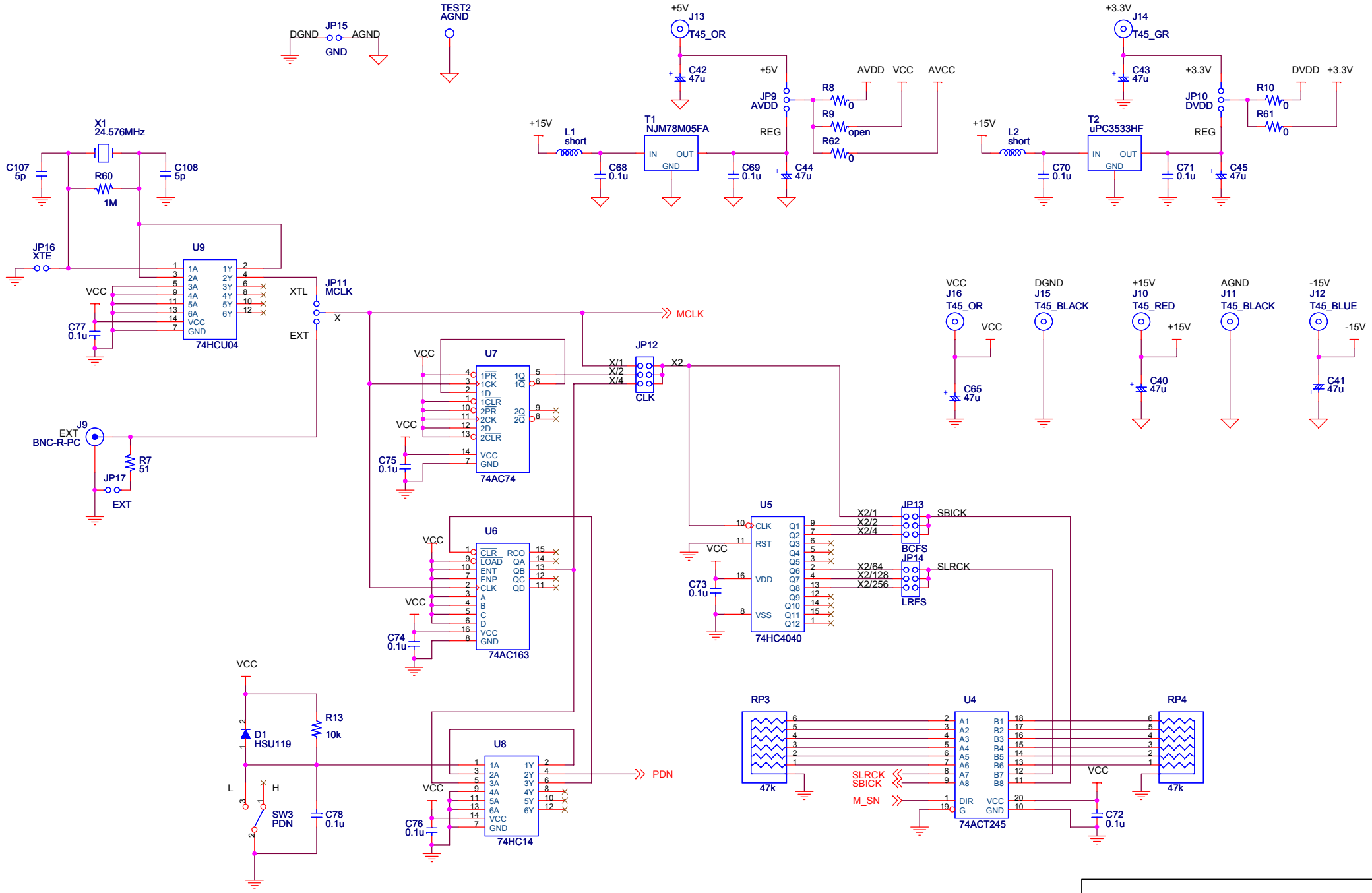
Title	AKD5388-A	
Size A3	Document Number INPUT1	Rev 4
Date: Tuesday, February 10, 2009	Sheet 2 of 5	



Title	AKD5388-A	
Size A3	Document Number INPUT2	Rev 4
Date: Tuesday, February 10, 2009	Sheet 3 of 5	



Title	AKD5388-A	
Size: A3	Document Number: AK4101A	Rev: 4
Date: Tuesday, February 10, 2009	Sheet 4 of 5	


DGND
JP15
AGND
GND
TEST2
AGND
+5V
J13
T45_OR
C42
47u
+5V
JP9
AVDD
R8
0
R9
open
R62
0
AVDD
VCC
AVCC
REG
+15V
L1
short
T1
NJM78M05FA
IN
OUT
GND
C68
0.1u
C69
0.1u
C44
47u
+3.3V
J14
T45_GR
C43
47u
+3.3V
JP10
DVDD
R10
0
R61
0
DVDD
+3.3V
REG
+15V
L2
short
T2
uPC3533HF
IN
OUT
GND
C70
0.1u
C71
0.1u
C45
47u
X1
24.576MHz
C107
5p
C108
5p
R60
1M
JP16
XTE
U9
1A
2A
3A
4A
5A
6A
VCC
GND
1Y
2Y
3Y
4Y
5Y
6Y
74HCU04
VCC
C77
0.1u
XTL
JP11
MCLK
X
EXT
MCLK
J9
EXT
BNC-R-PC
R7
51
JP17
EXT
U7
1PR
1CK
1D
1CLR
2PR
2CK
2D
2CLR
1Q
1Q
2Q
2Q
74AC74
C75
0.1u
JP12
X/1
X/2
X/4
CLK
X2
U6
CLR
LOAD
ENT
ENP
CLK
A
B
C
D
RCO
QA
QB
QC
QD
74AC163
C74
0.1u
U5
CLK
RST
VDD
VSS
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
74HC4040
C73
0.1u
X2/1
X2/2
X2/4
X2/64
X2/128
X2/256
JP13
BCFS
JP14
LRFS
SBICK
SLRCK
VCC
J16
T45_OR
C65
47u
DGND
J15
T45_BLACK
+15V
J10
T45_RED
C40
47u
AGND
J11
T45_BLACK
-15V
J12
T45_BLUE
C41
47u
D1
HSU119
R13
10k
L
H
SW3
PDN
C78
0.1u
U8
74HC14
C76
0.1u
PDN
RP3
47k
U4
74ACT245
SLRCK
SBICK
M_SN
RP4
47k
C72
0.1u
Title
AKD5388-A
Size
A3
Document Number
LOGIC
Rev
4
Date:
Tuesday, February 10, 2009
Sheet
5
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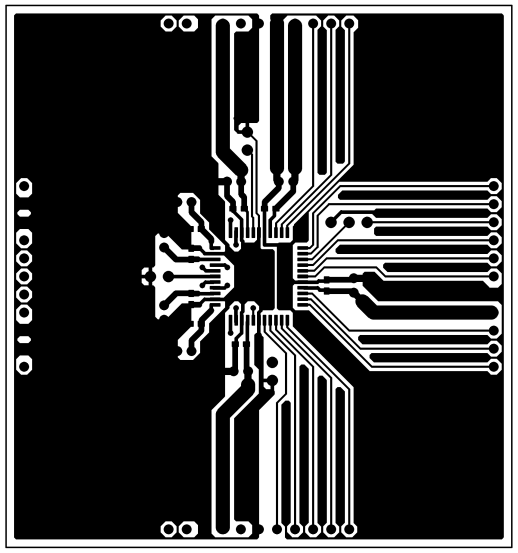
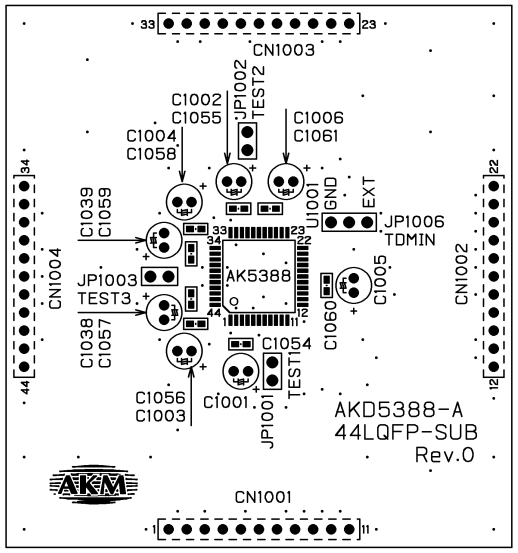
5



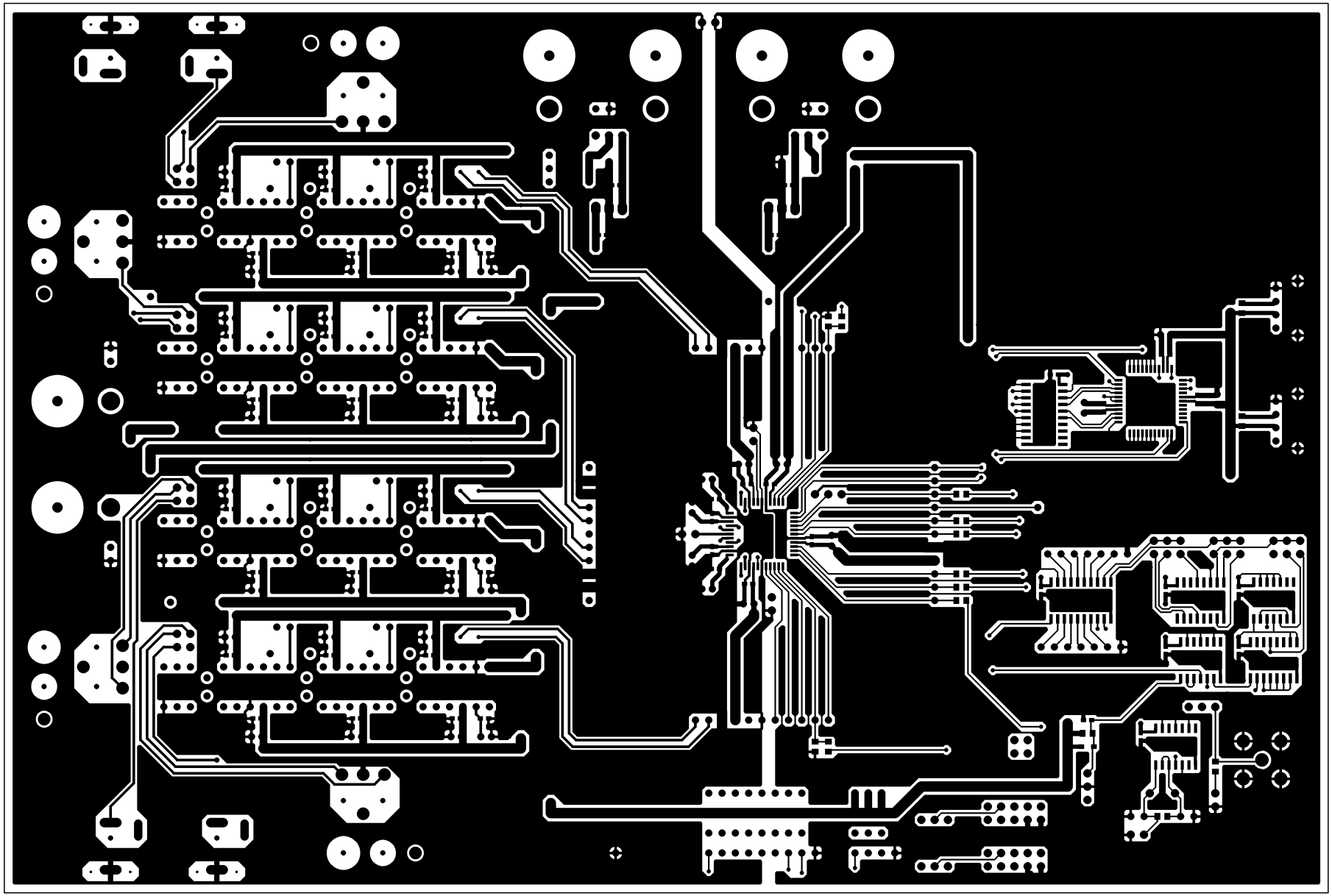
22540B L1

L2 BOARD



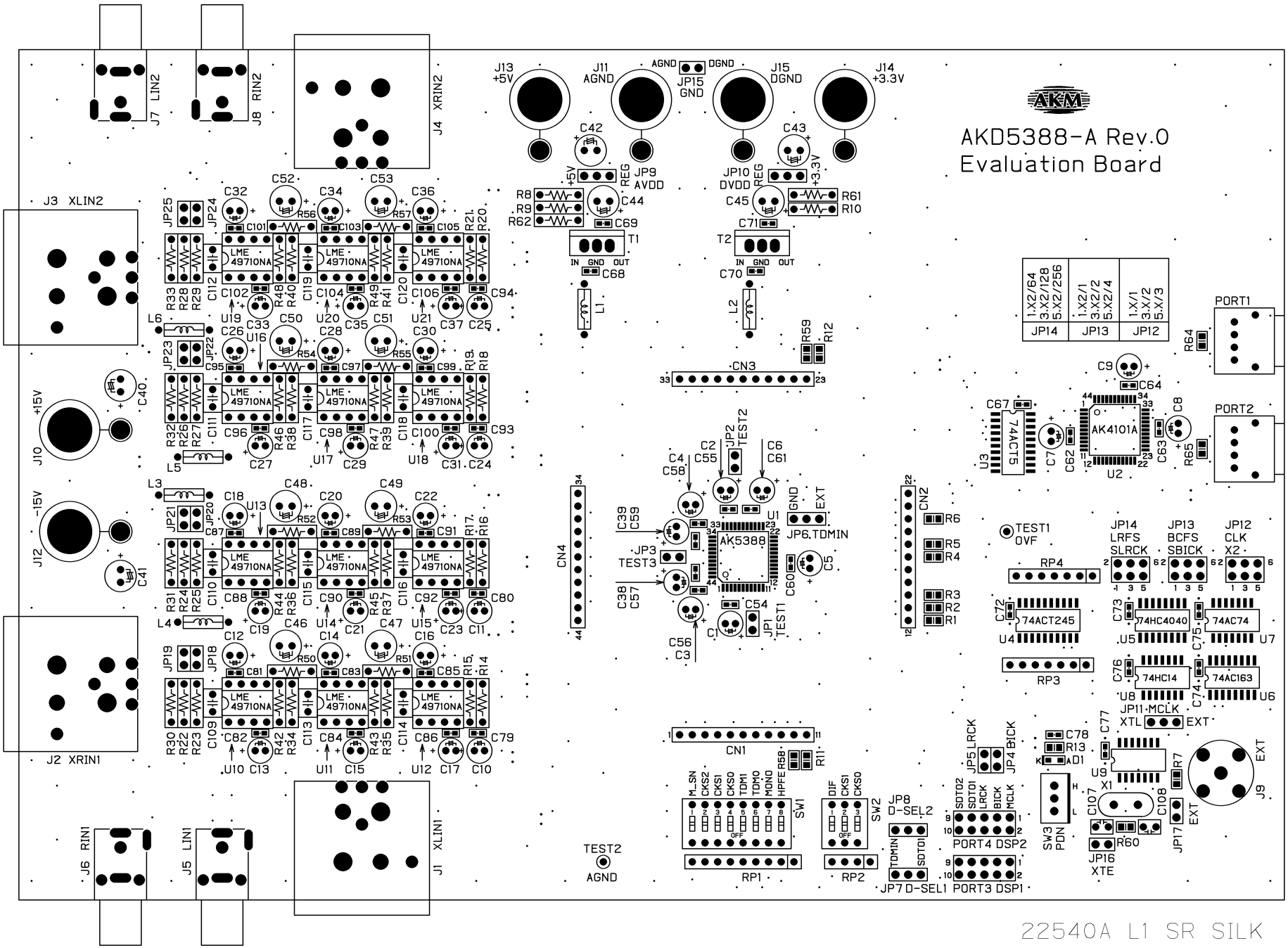
22540B L1 SR SILK

22540B LZ SR SILK



22540A L1

L2 A04522


AKD5388-A Rev.0
Evaluation Board
AKM
J1 XLIN1
J2 XRIN1
J3 XLIN2
J4 XRIN2
J5 LIN1
J6 RIN1
J7 LIN2
J8 RIN2
J9 EXT
J10 +15V
J11 AGND
J12 -15V
J13 +5V
J14 +3.3V
J15 DGND
JP15 GND
JP9 AVDD
JP10 DVDD
REG
AK5388
AK4101A
LME 49710NA
74ACT15
74ACT245
74HC4040
74AC74
74HC14
74AC163
PORT1
PORT2
PORT3 DSP1
PORT4 DSP2
JP14 LRFS SLRCK
JP13 BCFS SBICK
JP12 CLK X2
JP11 MCLK XTL EXT
JP5 LRCK
JP4 BICK
JP6 TDMIN
JP7 D-SEL1
JP8 D-SEL2
JP16 XTE
JP17 EXT
SW1
SW2
SW3 PDN
TEST1 OVF
TEST2 AGND
TEST3
1.X2/64 3.X2/128 5.X2/256
1.X2/1 3.X2/2 5.X2/4
1.X/1 3.X/2 5.X/3
22540A L1 SR SILK

225404 L2 SR