FAIRCHILD SEMICONDUCTOR TM

January 2001

Si4539DY
Dual N & P-Channel Enhancement Mode Field Effect Transistor

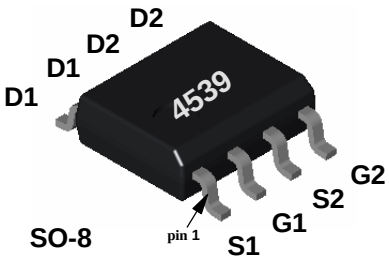
General Description

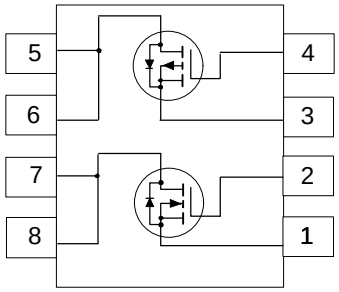
These dual N- and P -Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 7.0 A,30 V, $R_{DS(ON)}$=0.028 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$=0.040 Ω @ V_{GS}= 4.5 V.
  P-Channel -5.0 A,-30 V,$R_{DS(ON)}$=0.052 Ω @ V_{GS}=-10 V
  $R_{DS(ON)}$=0.080Ω @ V_{GS}=-4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a)	7	-5	A
	- Pulsed		20	-20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C	N-Ch		30		mV/°C
		I_D = -250 µA, Referenced to 25 °C	P-Ch		-25		
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-1	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.7	3	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.5	-3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C	N-Ch		-4.4		mV/°C
		I_D = -250 µA, Referenced to 25 °C	P-Ch		3.2		
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.0 A	N-Ch		0.024	0.028	Ω
		V_{GS} = 4.5 V, I_D = 6.0 A			0.035	0.04	
		V_{GS} = -10 V, I_D = -5.0 A	P-Ch		0.044	0.052	
		V_{GS} = -4.5 V, I_D = - 4.0 A			0.068	0.08	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-20			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = -7 A	N-Ch		15		S
		V_{DS} = -5 V, I_D = -5 A	P-Ch		8		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		650		pF
			P-Ch		730		
C_{oss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		345		pF
			P-Ch		400		
C_{rss}	Reverse Transfer Capacitance		N-Ch		90		pF
			P-Ch		90		

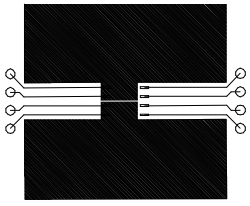
Electrical Characteristics (continued)

SWITCHING CHARACTERISTICS (Note 2)

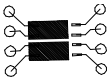
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = 10 V, I_D = 1 A	N-Ch		8	16	ns
		V_{GS} = 10 V, R_{GEN} = 6 Ω	P-Ch		11	20	
t_r	Turn - On Rise Time		N-Ch		14	25	ns
			P-Ch		10	18	
$t_{D(off)}$	Turn - Off Delay Time	V_{DS} = -10 V, I_D = -1 A	N-Ch		23	37	ns
		V_{GS} = -10 V, R_{GEN} = 6 Ω	P-Ch		90	125	
t_f	Turn - Off Fall Time		N-Ch		9	18	ns
			P-Ch		55	80	
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 7 A,	N-Ch		18	26	nC
		V_{GS} = 10 V	P-Ch		19	27	
Q_{gs}	Gate-Source Charge		N-Ch		3.2		nC
		V_{DS} = -10 V, I_D = -5 A,	P-Ch		3.5		
Q_{gd}	Gate-Drain Charge	V_{GS} = -10 V	N-Ch		4.3		nC
			P-Ch		3.6		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.3	A
			P-Ch			-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	N-Ch		0.75	1.2	V
		V_{GS} = 0 V, I_S = -1.3 A (Note 2)	P-Ch		-0.75	-1.2	V

Notes:

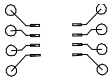
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics: N-Channel

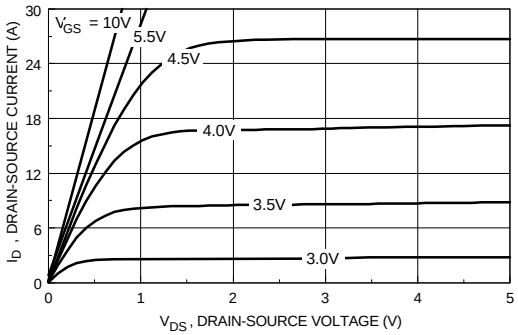


Figure 1. On-Region Characteristics.

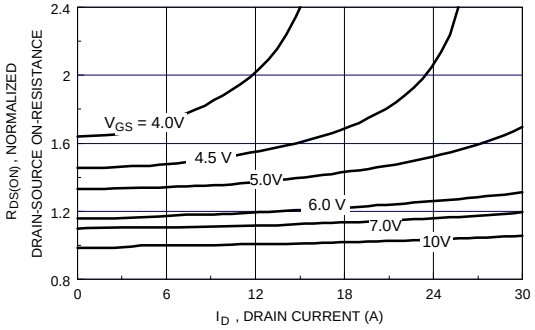


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

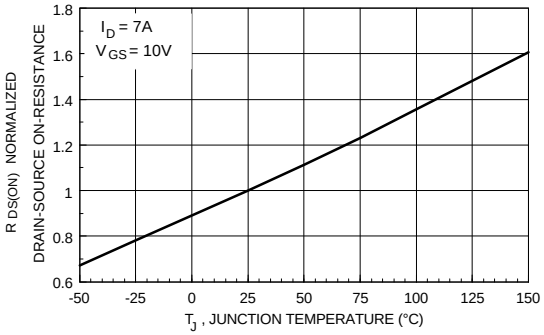


Figure 3. On-Resistance Variation with Temperature.

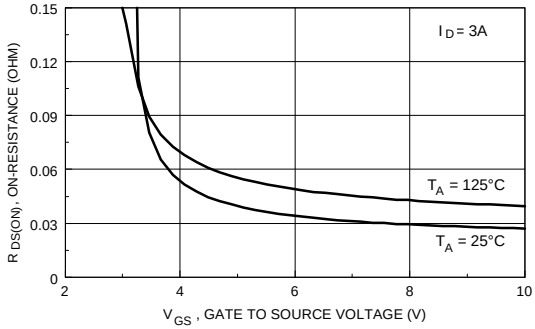


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

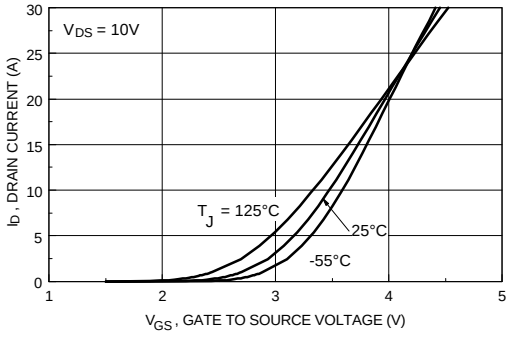


Figure 5. Transfer Characteristics.

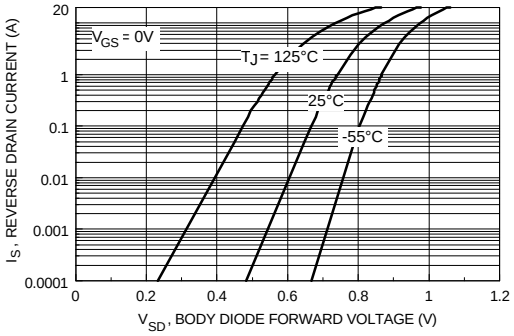


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

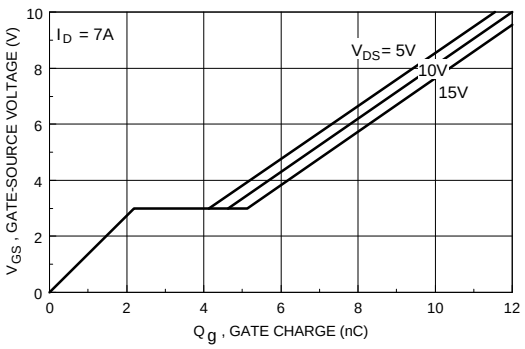


Figure 7. Gate Charge Characteristics.

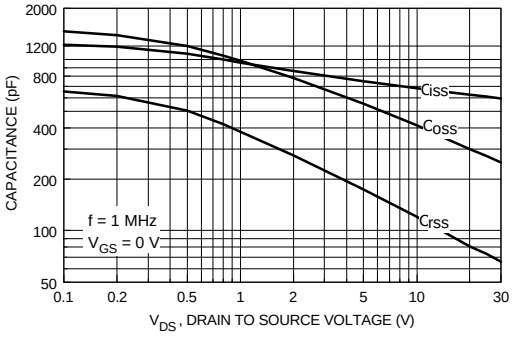


Figure 8. Capacitance Characteristics.

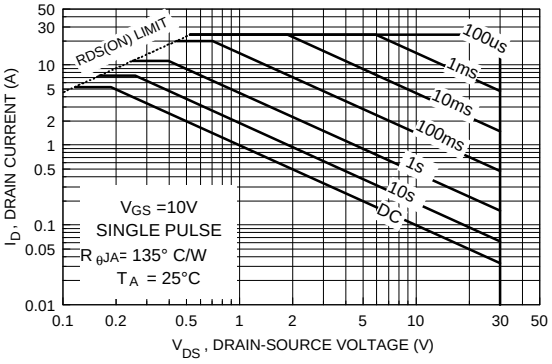


Figure 9. Maximum Safe Operating Area.

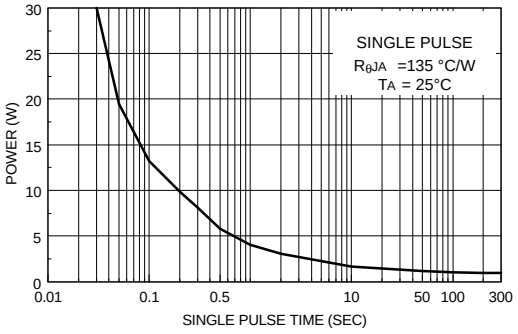


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

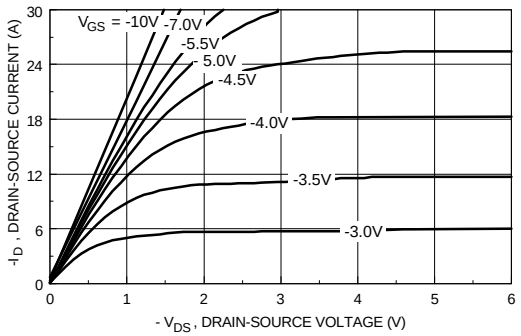


Figure 11. On-Region Characteristics.

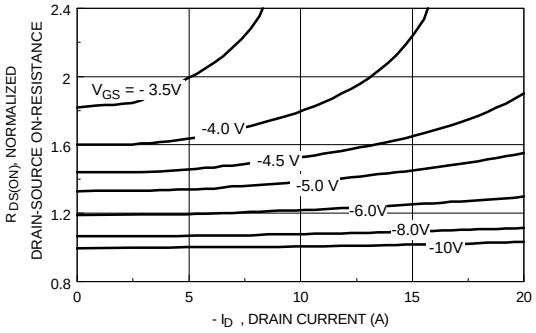


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

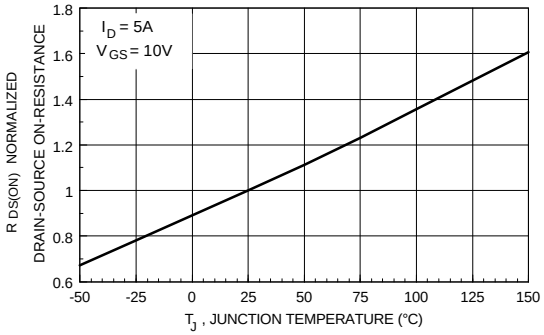


Figure 13. On-Resistance Variation with Temperature.

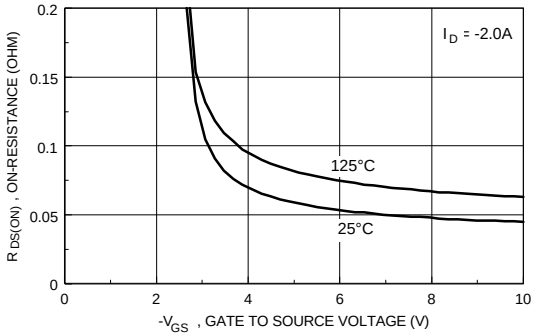


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

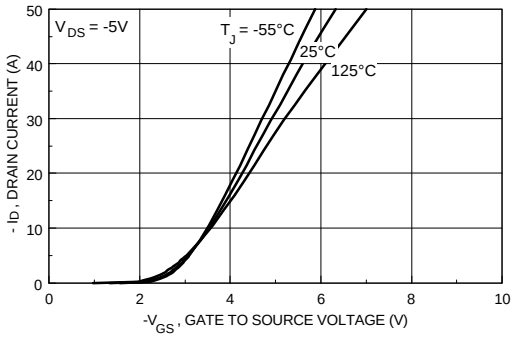


Figure 15. Transfer Characteristics.

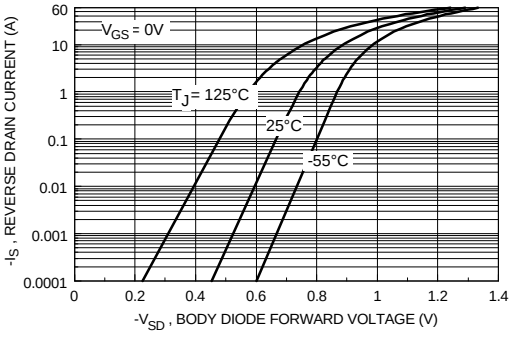


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

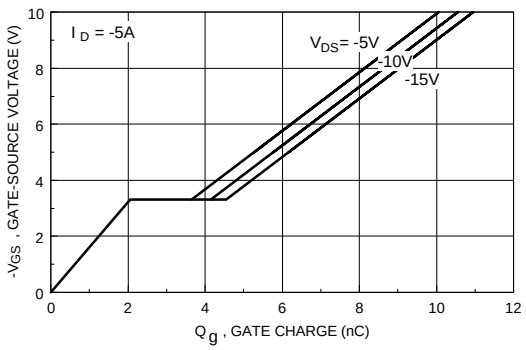


Figure 17. Gate Charge Characteristics.

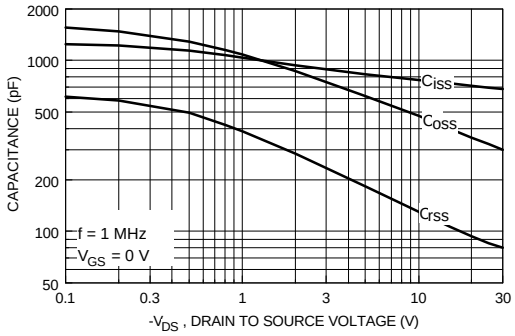


Figure 18. Capacitance Characteristics.

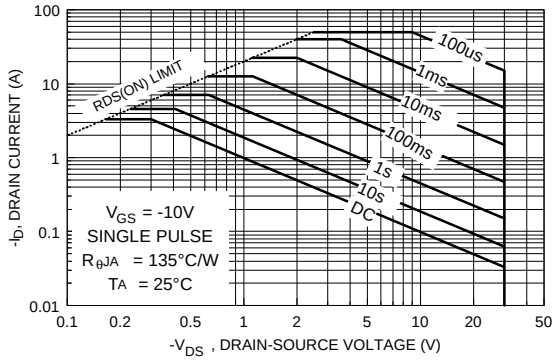


Figure 19. Maximum Safe Operating Area.

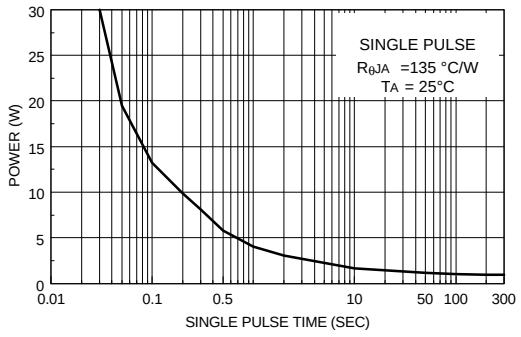


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Thermal Characteristics: N & P-Channel (continued)

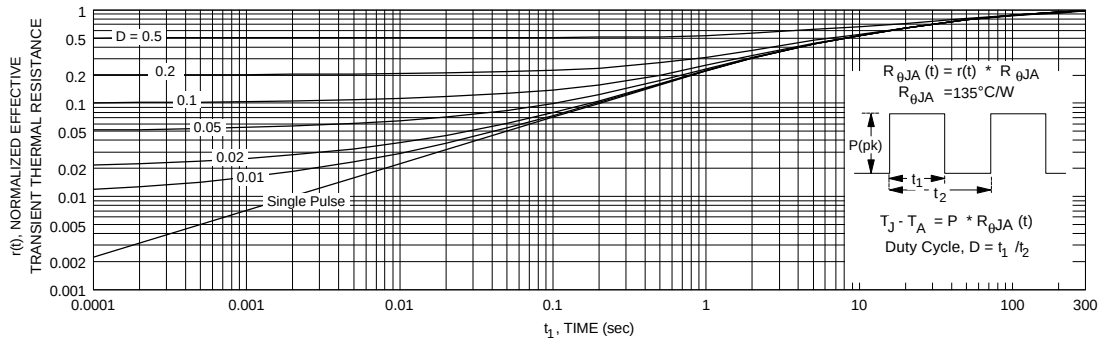


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1.
Transient thermalresponse will change depending on the circuit board design.

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