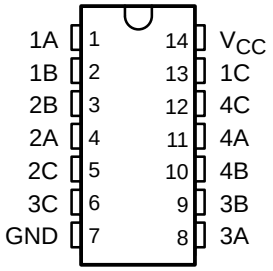
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Typical Switch Enable Time of 18 ns**
- **Low Power Consumption, 20-μA Max $I_{CC}$**
- **Low Input Current of 1 μA Max**
- **High Degree of Linearity**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . . 50-Ω TYP at $V_{CC}$ = 6 V**
- **Individual Switch Controls**

**D, DB, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

**ORDERING INFORMATION**

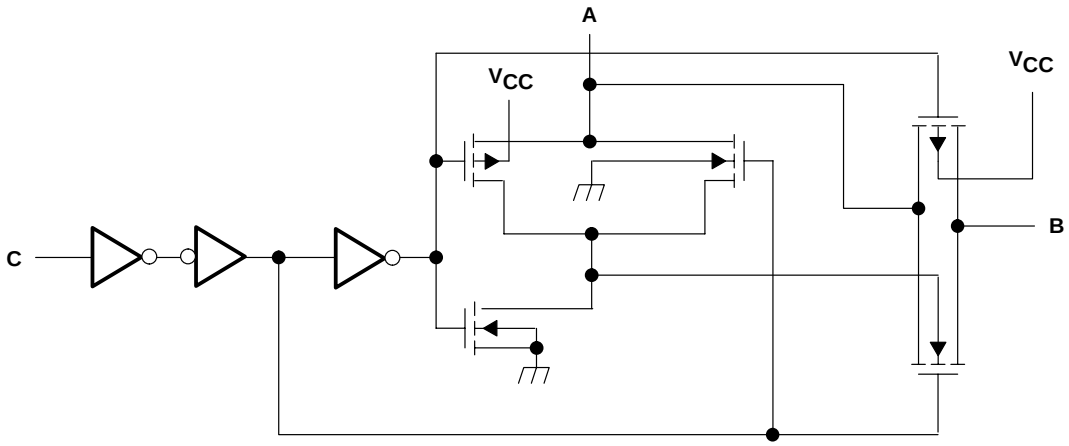
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube of 25 | SN74HC4066N | SN74HC4066N |
| | SOIC – D | Tube of 50 | SN74HC4066D | HC4066 |
| | | Reel of 2500 | SN74HC4066DR | |
| | | Reel of 250 | SN74HC4066DT | |
| | SOP – NS | Reel of 2000 | SN74HC4066NSR | HC4066 |
| | SSOP – DB | Reel of 2000 | SN74HC4066DBR | HC4066 |
| | TSSOP – PW | Tube of 90 | SN74HC4066PW | HC4066 |
| | | Reel of 2000 | SN74HC4066PWR | |
| | | Reel of 250 | SN74HC4066PWT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each switch)**

| INPUT CONTROL (C) | SWITCH |
|---|---|
| L | OFF |
| H | ON |

## logic diagram, each switch (positive logic)




**One of Four Switches**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ (see Note 1) | –0.5 V to 7 V |
| Control-input diode current, $I_I$ ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| I/O port diode current, $I_I$ ($V_I < 0$ or $V_{I/O} > V_{CC}$) | ±20 mA |
| On-state switch current ($V_{I/O} = 0$ to $V_{CC}$) | ±25 mA |
| Continuous current through $V_{CC}$ or GND | ±50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2† | 5 | 6 | V |
| $V_{I/O}$ | I/O port voltage | | 0 | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage, control inputs | $V_{CC}$ = 2 V | 1.5 | | $V_{CC}$ | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | $V_{CC}$ | |
| | | $V_{CC}$ = 6 V | 4.2 | | $V_{CC}$ | |
| $V_{IL}$ | Low-level input voltage, control inputs | $V_{CC}$ = 2 V | 0 | | 0.3 | V |
| | | $V_{CC}$ = 4.5 V | 0 | | 0.9 | |
| | | $V_{CC}$ = 6 V | 0 | | 1.2 | |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC}$ = 2 V | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | | | |
| $r_{on}$ | On-state switch resistance | | $I_T$ = –1 mA, $V_I$ = 0 to $V_{CC}$, $V_C$ = $V_{IH}$ (see Figure 1) | 2 V | | 150 | | | | Ω |
| | | | | 4.5 V | | 50 | 85 | | 106 | |
| | | | | 6 V | | 30 | | | | |
| $r_{on(p)}$ | Peak on-state resistance | | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$, $I_T$ = –1 mA | 2 V | | 320 | | | | Ω |
| | | | | 4.5 V | | 70 | 170 | | 215 | |
| | | | | 6 V | | 50 | | | | |
| $I_I$ | Control input current | | $V_C$ = 0 or $V_{CC}$ | 6 V | | ±0.1 | ±100 | | ±1000 | nA |
| $I_{soff}$ | Off-state switch leakage current | | $V_I$ = $V_{CC}$ or 0, $V_O$ = $V_{CC}$ or 0, $V_C$ = $V_{IL}$ (see Figure 2) | 6 V | | | ±0.1 | | ±5 | µA |
| $I_{son}$ | On-state switch leakage current | | $V_I$ = $V_{CC}$ or 0, $V_C$ = $V_{IH}$ (see Figure 3) | 6 V | | | ±0.1 | | ±5 | µA |
| $I_{CC}$ | Supply current | | $V_I$ = 0 or $V_{CC}$, $I_O$ = 0 | 6 V | | | 2 | | 20 | µA |
| $C_i$ | Input capacitance | A or B | | 5 V | | 9 | | | | pF |
| | | C | | | | 3 | 10 | | 10 | |
| $C_f$ | Feed-through capacitance | A to B | $V_I$ = 0 | | | 0.5 | | | | pF |
| $C_o$ | Output capacitance | A or B | | 5 V | | 9 | | | | pF |

## switching characteristics over recommended operating free-air temperature range

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 50 pF (see Figure 4) | 2 V | | 10 | 60 | | 75 | ns |
| | | | | | 4.5 V | | 4 | 12 | | 15 | |
| | | | | | 6 V | | 3 | 10 | | 13 | |
| $t_{PZH}$, $t_{PZL}$ | Switch turn-on time | C | A or B | $R_L$ = 1 kΩ, $C_L$ = 50 pF (see Figure 5) | 2 V | | 70 | 180 | | 225 | ns |
| | | | | | 4.5 V | | 21 | 36 | | 45 | |
| | | | | | 6 V | | 18 | 31 | | 38 | |
| $t_{PLZ}$, $t_{PHZ}$ | Switch turn-off time | C | A or B | $R_L$ = 1 kΩ, $C_L$ = 50 pF (see Figure 5) | 2 V | | 50 | 200 | | 250 | ns |
| | | | | | 4.5 V | | 25 | 40 | | 50 | |
| | | | | | 6 V | | 22 | 34 | | 43 | |
| $f_I$ | Control input frequency | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ, $V_C$ = $V_{CC}$ or GND, $V_O$ = $V_{CC}$/2 (see Figure 6) | 2 V | | 15 | | | | MHz |
| | | | | | 4.5 V | | 30 | | | | |
| | | | | | 6 V | | 30 | | | | |
| | Control feed-through noise | C | A or B | $C_L$ = 50 pF, $R_{in}$ = $R_L$ = 600 Ω, $V_C$ = $V_{CC}$ or GND, $f_{in}$ = 1 MHz (see Figure 7) | 4.5 V | | 15 | | | | mV (rms) |
| | | | | | 6 V | | 20 | | | | |

## operating characteristics, $V_{CC}$ = 4.5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | $C_L$ = 50 pF, | f = 1 MHz | 45 | pF |
| | Minimum through bandwidth, A to B or B to A† [20 log ($V_O$/$V_I$)] = –3 dB | $C_L$ = 50 pF, $V_C$ = $V_{CC}$ | $R_L$ = 600 Ω, (see Figure 8) | 30 | MHz |
| | Crosstalk between any switches‡ | $C_L$ = 10 pF, $f_{in}$ = 1 MHz | $R_L$ = 50 Ω, (see Figure 9) | 45 | dB |
| | Feed through, switch off, A to B or B to A‡ | $C_L$ = 50 pF, $f_{in}$ = 1 MHz | $R_L$ = 600 Ω, (see Figure 10) | 42 | dB |
| | Amplitude distortion rate, A to B or B to A | $C_L$ = 50 pF, $f_{in}$ = 1 kHz | $R_L$ = 10 kΩ, (see Figure 11) | 0.05% | |

† Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.
‡ Adjust the input amplitude for input = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

## PARAMETER MEASUREMENT INFORMATION

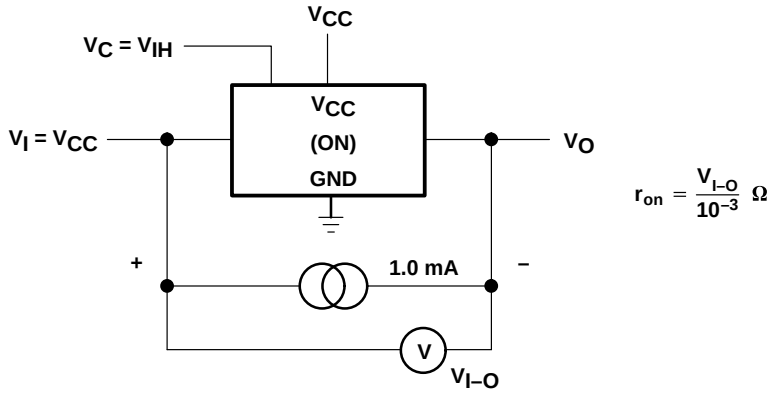
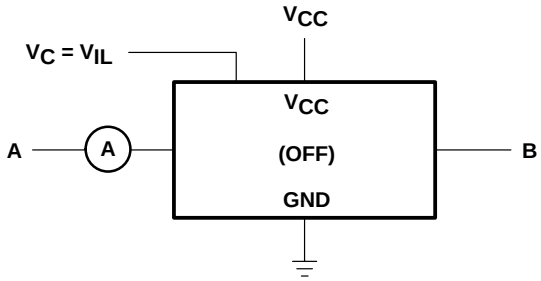



**Figure 1. On-State Resistance Test Circuit**




$V_S = V_A - V_B$
CONDITION 1: $V_A = 0$, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, $V_B = 0$

**Figure 2. Off-State Switch Leakage-Current Test Circuit**

## PARAMETER MEASUREMENT INFORMATION

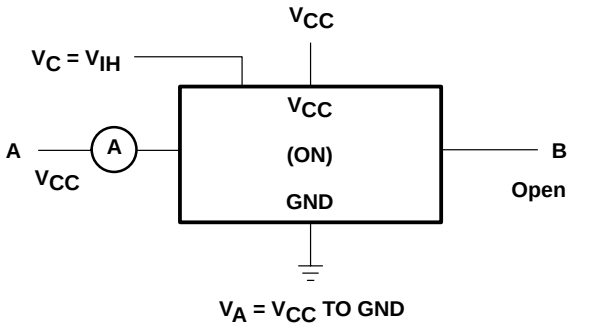



**Figure 3. On-State Leakage-Current Test Circuit**

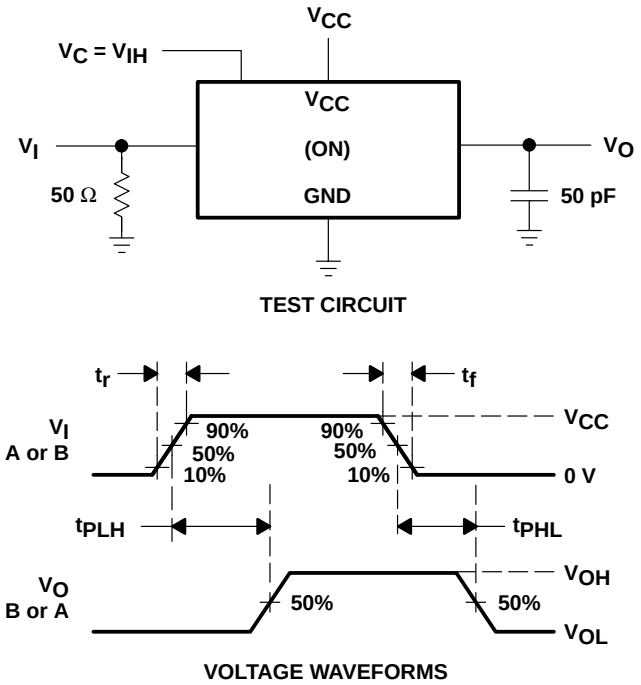
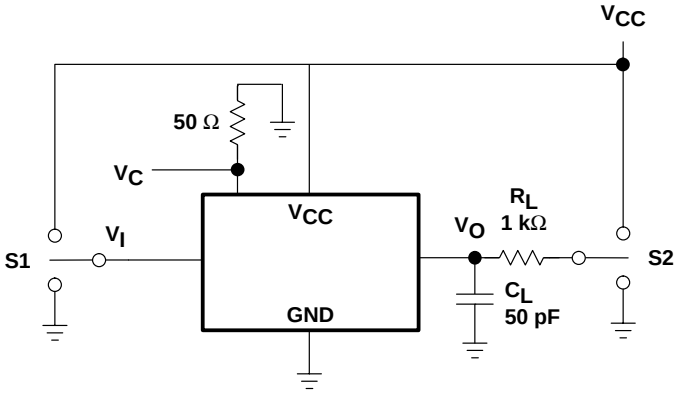


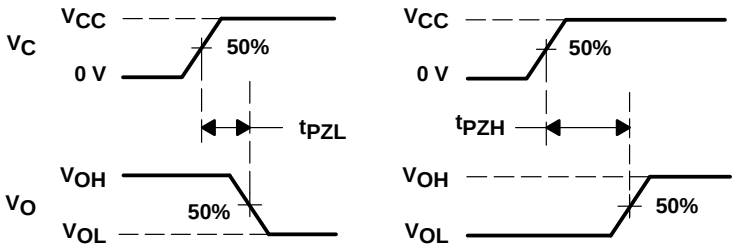

**Figure 4. Propagation Delay Time, Signal Input to Signal Output**

## PARAMETER MEASUREMENT INFORMATION

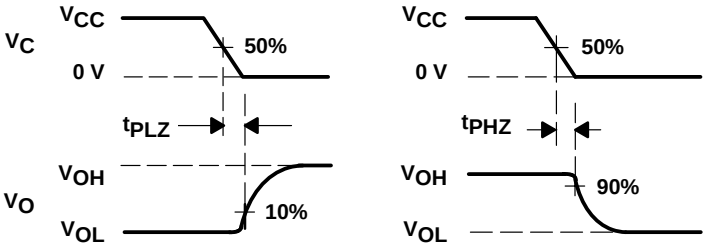



| TEST | S1 | S2 |
|---|---|---|
| $t_{PZL}$ | GND | $V_{CC}$ |
| $t_{PZH}$ | $V_{CC}$ | GND |
| $t_{PLZ}$ | GND | $V_{CC}$ |
| $t_{PHZ}$ | $V_{CC}$ | GND |

TEST CIRCUIT




($t_{PZL}$, $t_{PZH}$)




($t_{PLZ}$, $t_{PHZ}$)

VOLTAGE WAVEFORMS

**Figure 5. Switching Time ($t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$), Control to Signal Output**

## PARAMETER MEASUREMENT INFORMATION

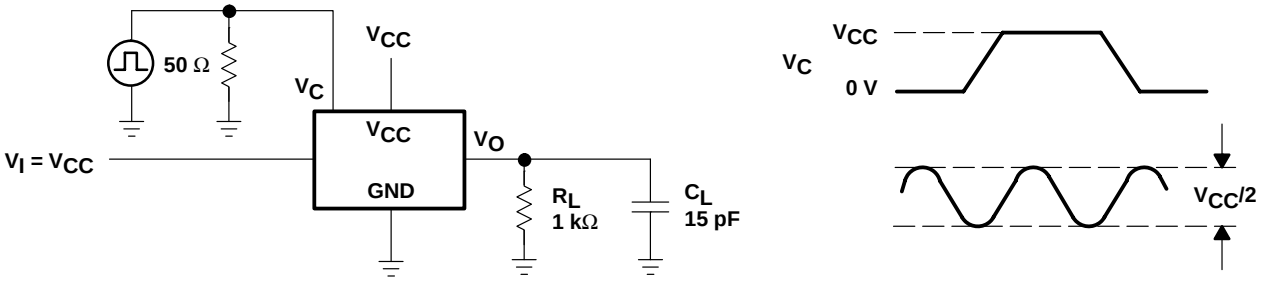



**Figure 6. Control-Input Frequency**

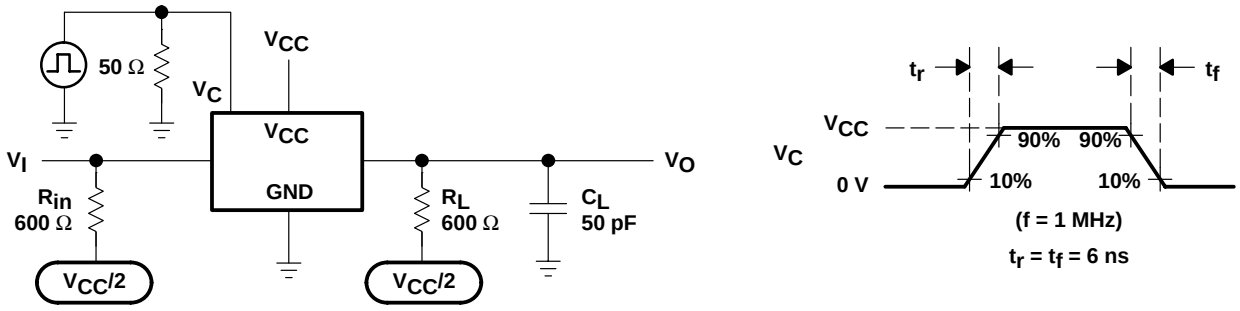



**Figure 7. Control Feed-Through Noise**

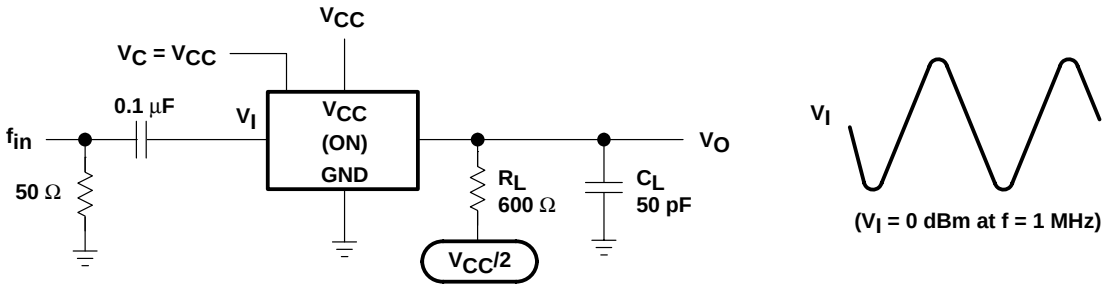



**Figure 8. Minimum Through Bandwidth**

## PARAMETER MEASUREMENT INFORMATION

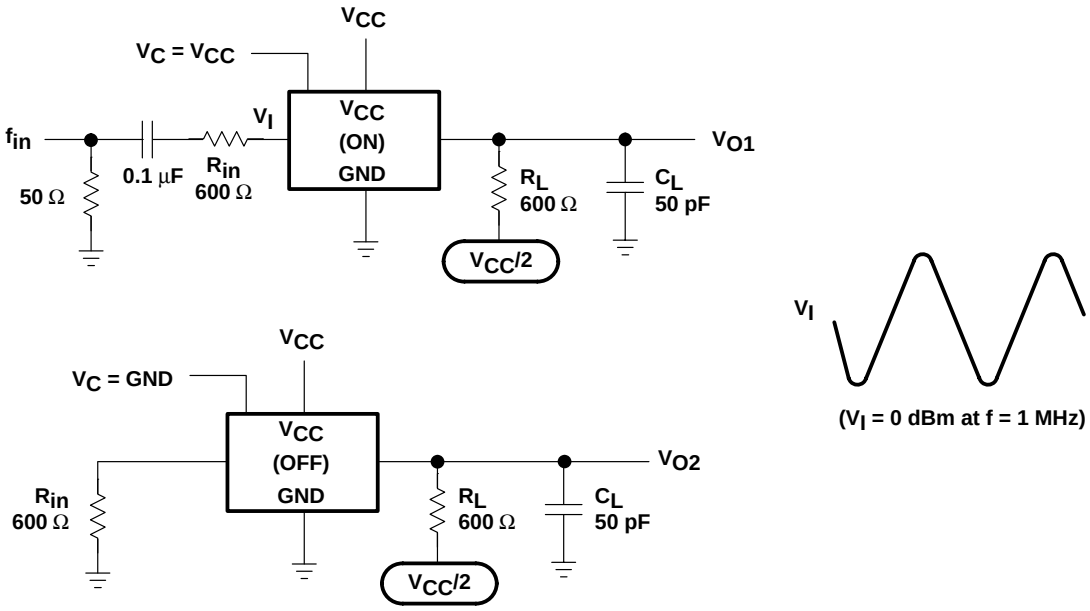



**Figure 9. Crosstalk Between Any Two Switches**

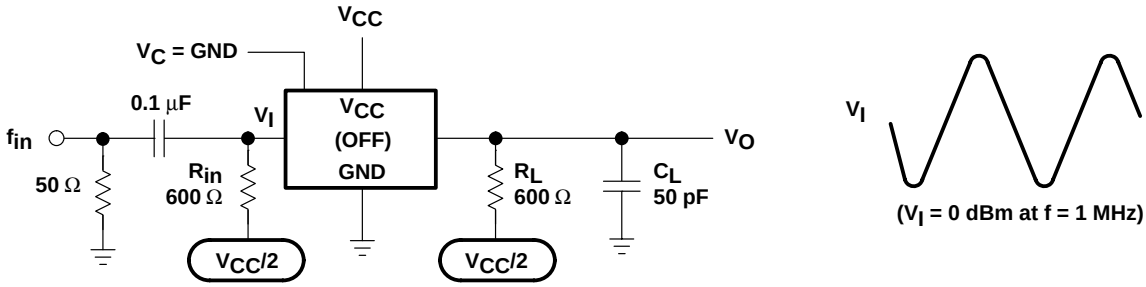



**Figure 10. Feed Through, Switch Off**

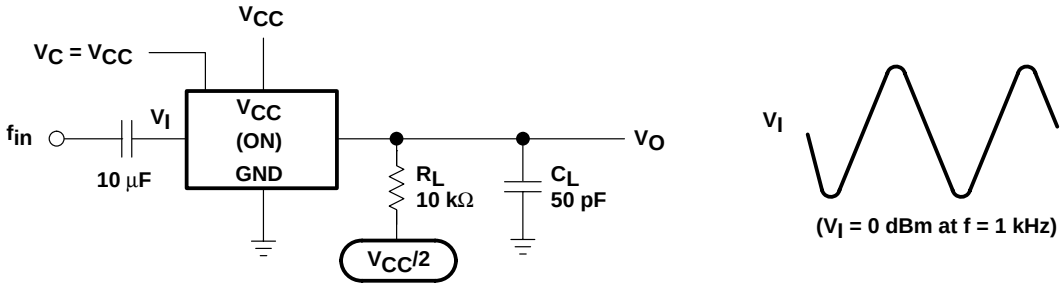



**Figure 11. Amplitude-Distortion Rate**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74HC4066D | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74HC4066DBR | ACTIVE | SSOP | DB | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DE4 | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC4066DT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066DTE4 | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74HC4066NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74HC4066NSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC4066NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC4066PW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4066PWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4066PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |
| SN74HC4066PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4066PWT | ACTIVE | TSSOP | PW | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC4066PWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

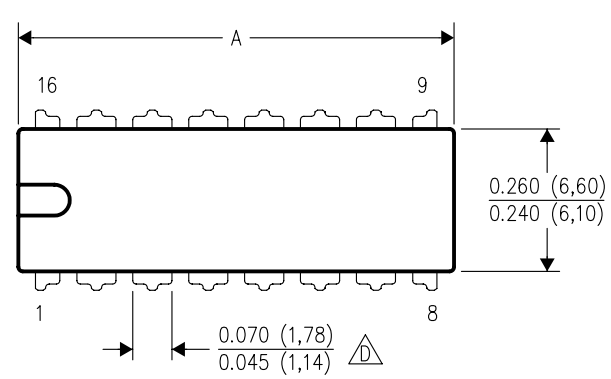
for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

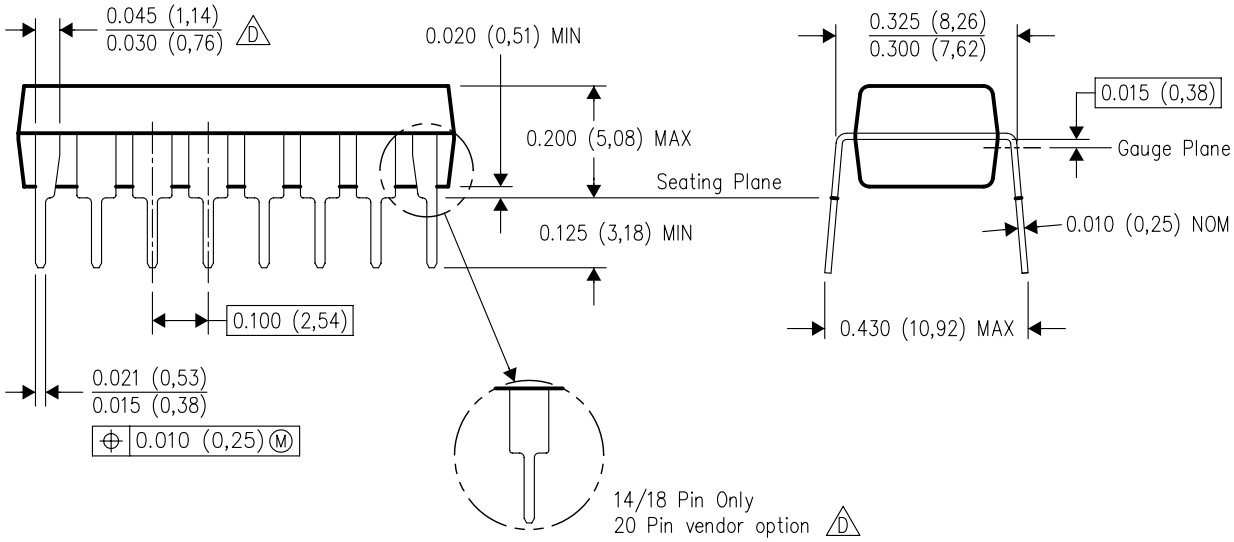
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



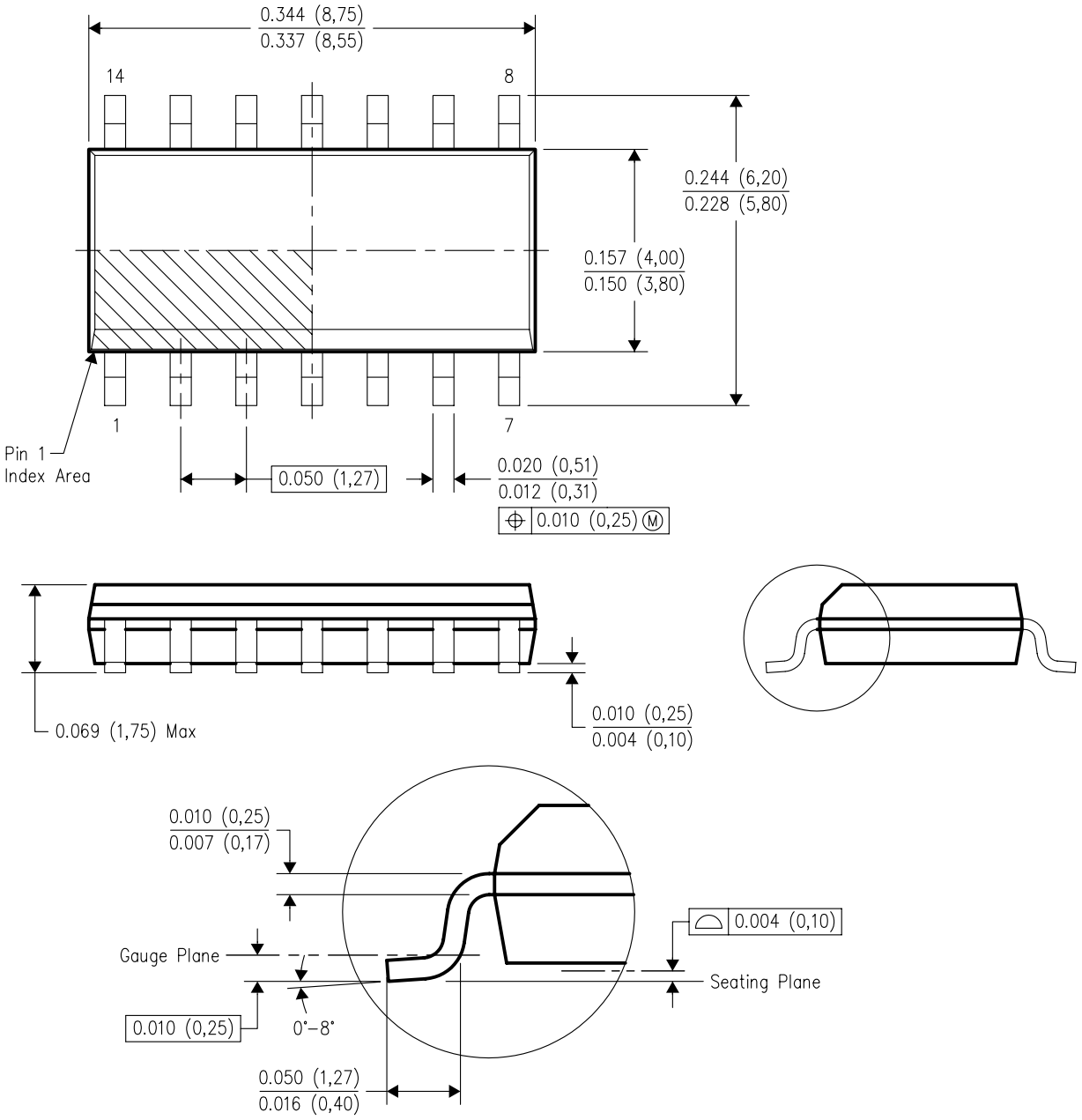

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

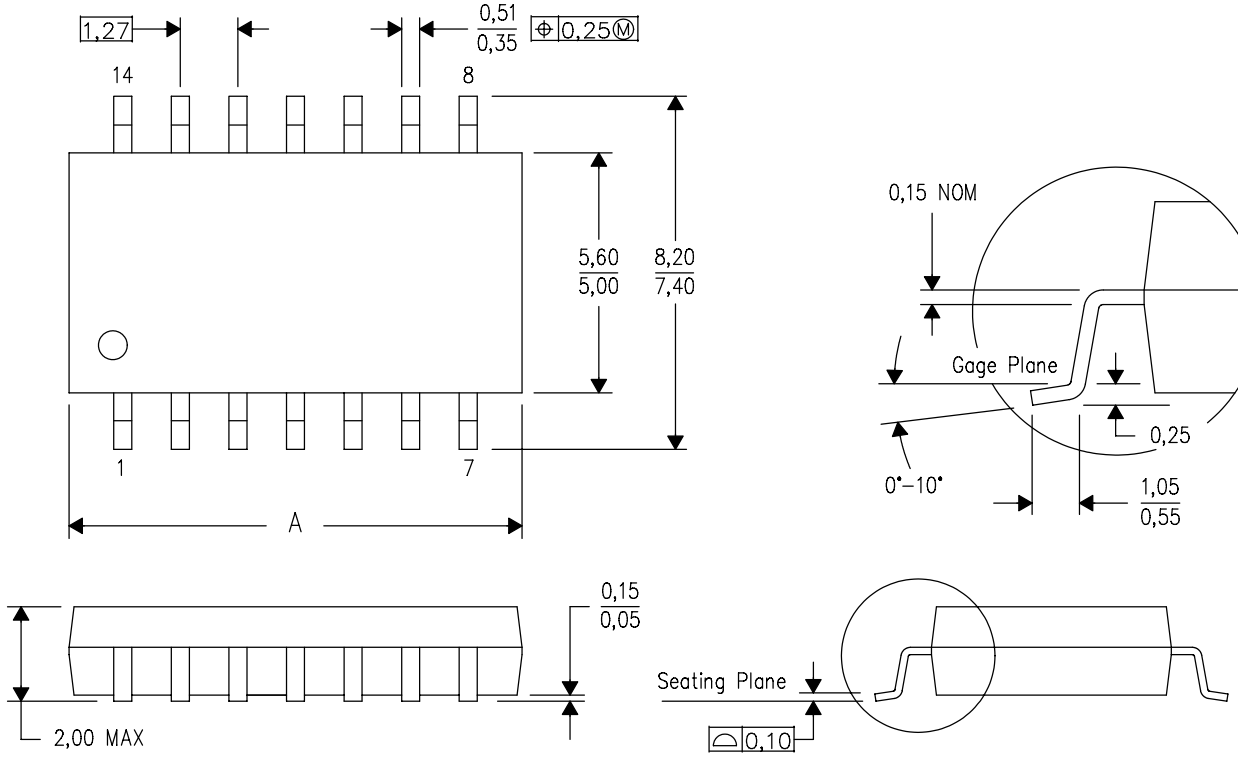



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

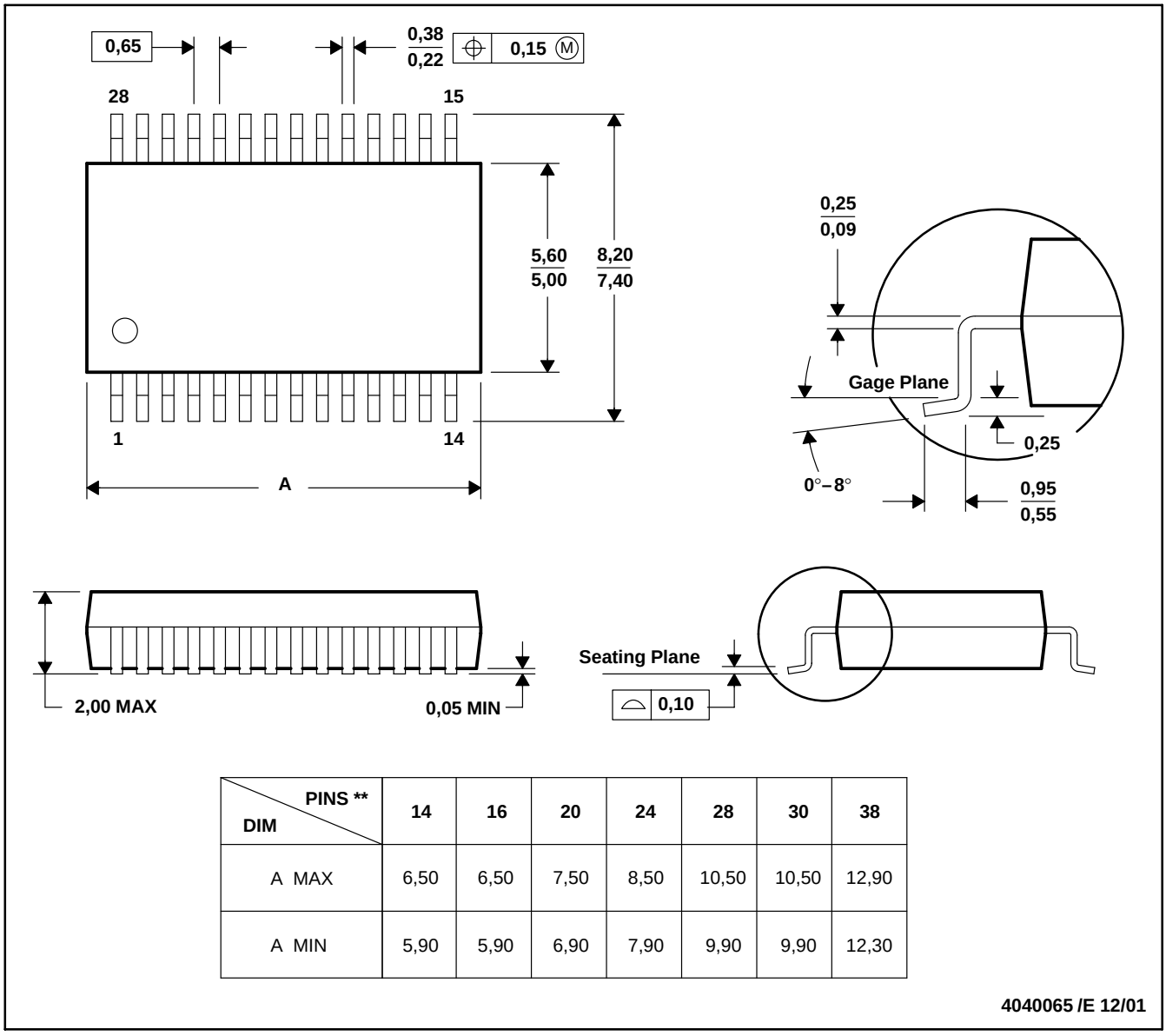
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



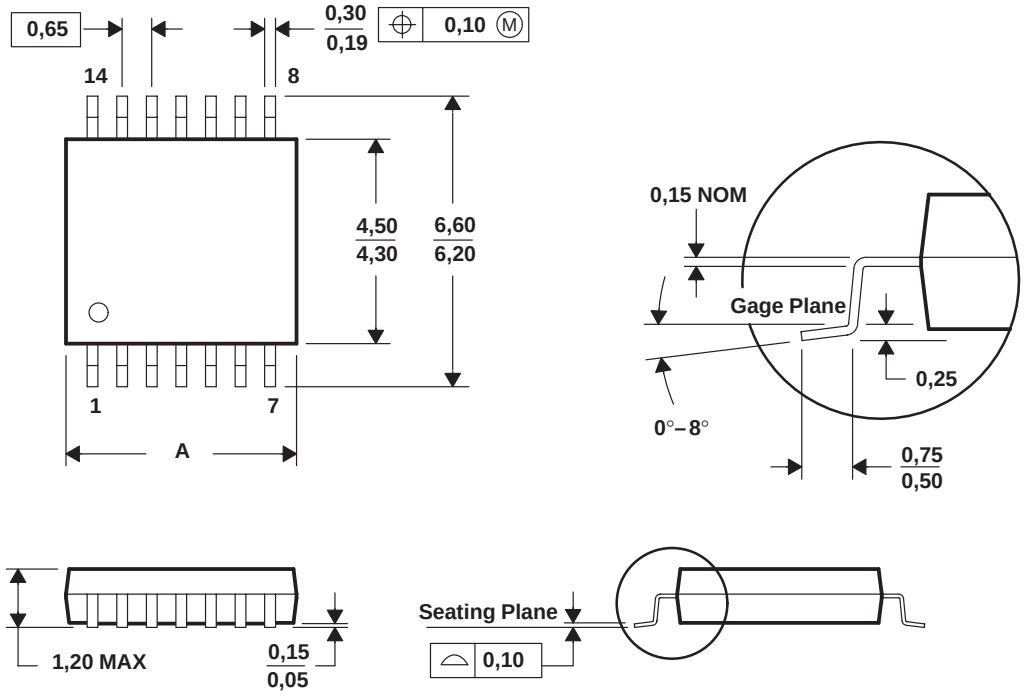

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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