1.5-Gbps 2 × 2 LVDS CROSSPOINT SWITCH

FEATURES

- **Designed for Signaling Rates [(1)] Up To 1.5 Gbps**
- **Total Jitter < 65 ps**
- **Pin-Compatible With SN65LVDS22 and SN65LVDM22**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With CML, LVPECL and LVDS Signal Levels**
- **Propagation Delay Times, 900 ps Maximum**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and TSSOP**

APPLICATIONS

- **10-G (OC-192) Optical Modules**
- **622-MHz Central Office Clock Distribution**
- **Wireless Basestations**
- **Low Jitter Clock Repeater/Multiplexer**
- **Protection Switching for Serial Backplanes**

(1) The signlaing rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

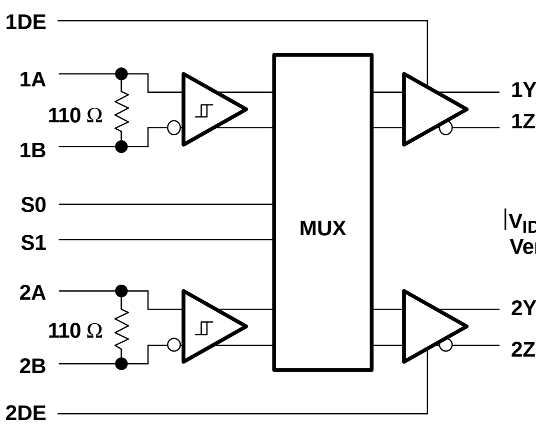
DESCRIPTION

The SN65LVDS122 and SN65LVDT122 are crosspoint switches that use low voltage differential signaling (LVDS) to achieve signaling rates as high as 1.5 Gbps. They are pin-compatible speed upgrades to the SN65LVDS22 and SN65LVDM22. The internal signal paths maintain differential signaling for high speeds and low signal skews. These devices have a 0-V to 4-V common-mode input range that accepts LVDS, LVPECL, or CML inputs. Two logic pins (S0 and S1) set the internal configuration between the differential inputs and outputs. This allows the flexibility to perform the following configurations: 2 x 2 crosspoint switch, 2:1 input multiplexer, 1:2 splitter or dual repeater/translator within a single device. Additionally, SN65LVDT122 incorporates a 110-Ω termination resistor for those applications where board space is a premium. Although these devices are designed for 1.5 Gbps, some applications at a 2-Gbps data rate can be supported depending on loading and signal quality.

The intended application of this device is ideal for loopback switching for diagnostic routines, fanout buffering of clock/data distribution provide protection in fault-tolerant systems, clock multiplexing in optical modules, and for overall signal boosting over extended distances.

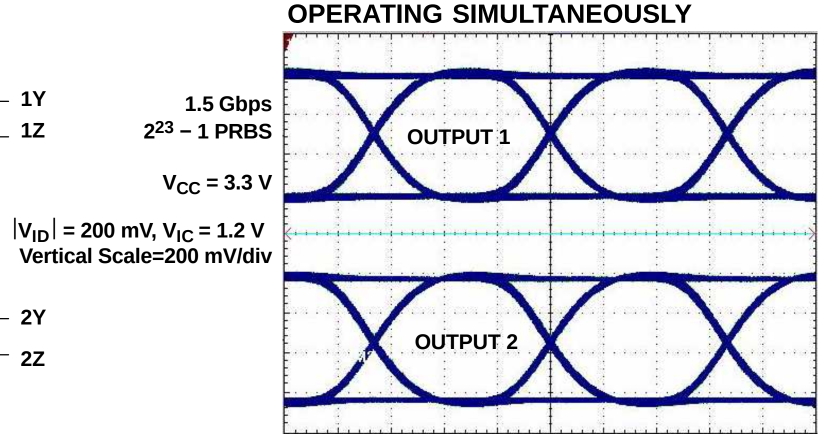
The SN65LVDS122 and SN65LVDT122 are characterized for operation from –40°C to 85°C.

FUNCTIONAL DIAGRAM



Integrated Termination on SN65LVDT122 Only

EYE PATTERNS OF OUTPUTS OPERATING SIMULTANEOUSLY



Horizontal Scale= 200 ps/div

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE	TERMINATION RESISTOR	PART NUMBER(1)	SYMBOLIZATION
SOIC	No	SN65LVDS122D	LVDS122
SOIC	Yes	SN65LVDT122D	LVDT122
TSSOP	No	SN65LVDS122PW	LVDS122
TSSOP	Yes	SN65LVDT122PW	LVDT122

(1) Add the suffix R for taped and reeled carrier

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

				SN65LVDS122, SN65LVDT122
V_{CC}	Supply voltage range(2)			–0.5 V to 4 V
	Voltage range	(A, B)		–0.7 V to 4.3 V
		$\|V_A\text{-}V_B\|$ (LVDT only)		1 V
		(DE, S0, S1)		–0.5 V to 4 V
		(Y, Z)		–0.5 V to 4 V
	ESD	Human Body Model(3)	A, B, Y, Z, and GND	±4 kV
			All pins	±2 kV
		Charged-Device Model(4)	All pins	±1500 V
	Continuous power dissipation			See Dissipation Rating Table
T_{stg}	Storage temperature range			–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	S0, S1, 1DE, 2DE	2		4	V
V_{IL}	Low-level input voltage	S0, S1, 1DE, 2DE	0		0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	LVDS	0.1		1	V
		LVDT	0.1		0.8	
	Input voltage (any combination of common-mode or input signals)		0		4	V
T_A	Operating free-air temperature		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
PW	712 mW	6.2 mW/°C	340 mW
D	1002 mW	8.7 mW/°C	480 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		See Figure 1 and Table 1	–100(2)			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis (V_{IT+}– V_{IT-})				25		mV
I_{IH}	High-level input current	DE	V_{IH} = 2	–10		0	µA
		S0, S1		0		20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V	–10		0	µA
		S0, S1				20	
I_{CC}	Supply current		R_L = 100 Ω		80	100	mA
			Disabled		35	45	
I_I	Input current (A or B inputs 'LVDS)		V_I = 0 V or 2.4 V, Other input at 1.2 V	–20		20	µA
			V_I = 4 V, Other input at 1.2 V	0		33	
	Input current (A or B inputs 'LVDT)		V_I = 0 V or 2.4 V, Other input open	–40		40	µA
			V_I = 4 V, Other input open	0		66	
$I_{I(OFF)}$	Input current (A or B inputs 'LVDS)		V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Other input at 1.2 V	–20		20	µA
			V_{CC} = 1.5 V, V_I = 2.4 V or 4 V, Other input at 1.2 V	0		33	
	Input current (A or B inputs 'LVDT)		V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Other input open	–40		40	µA
			V_{CC} = 1.5 V, V_I = 2.4 V or 4 V, Other input open	0		66	
I_{IO}	Input offset current (| I_{IA}– I_{IB} |) 'LVDS		V_{IA} = V_{IB}, 0 ≤ V_{IA} ≤ 4 V	–6		6	µA
R_T	Termination resistance ('LVDT)		V_{ID} = 300 mV and 500 mV, V_{IC} = 0 V to 2.4 V	90	110	132	Ω
	Termination resistance ('LVDT with power-off)		V_{ID} = 300 mV and 500 mV, V_{CC} = 1.5 V, V_{IC} = 0 V to 2.4 V	90	110	132	
C_I	Differential input capacitance ('LVDT with power-off)		V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
			Powered down (V_{CC} = 1.5 V)		3		

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2	247	310	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0 V	–24		24	mA
$I_{OS(D)}$	Differential short-circuit output current	V_{OD} = 0 V	–12		12	mA
I_{OZ}	High-impedance output current	V_{OD} = 600 mV	–1		1	µA
		V_O = 0 V or V_{CC}	–1		1	
C_o	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time		0			ns
t_{HOLD}	Input to select hold time		0.5			ns
t_{SWITCH}	Select to switch output		1	2	2.6	ns

SWITCHING CHARACTERISTICS

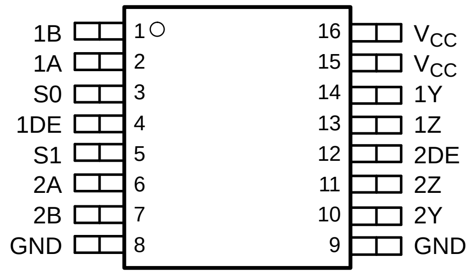
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	400	650	900	ps
t_{PHL}	Propagation delay time, high-to-low-level output		400	650	900	ps
t_r	Differential output signal rise time (20% - 80%)				280	ps
t_f	Differential output signal fall time (20% - 80%)				280	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)(2)			10	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)	V_{ID} = 0.2 V			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5)		1	2.2	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak)(4)	750 MHz clock input(6)		10	17	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	1.5 Gbps 2^{23}–1 PRBS input(7)		33	65	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^7–1 PRBS input(8)		17	50	ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		4	6	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 5		4	6	ns
$t_{sk(o)}$	Output skew(9)			15	40	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter is specified by design and characterization. Stimulus jitter has been subtracted.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%), measured over 1000 samples.
(6) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%).
(7) Input voltage = V_{ID} = 200 mV, 2^{23}–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200 k samples.
(8) Input voltage = V_{ID} = 200 mV, 2^7–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%).
(9) Output skew is the magnitude of the time delay difference between the outputs of a single device with all inputs tied together.

PIN ASSIGNMENT

D OR PW PACKAGE
(TOP VIEW)



Circuit Function Table

<table>
<tr><th colspan="6">INPUTS (1)</th><th colspan="2">OUTPUTS (1)</th><th rowspan="2">LOGIC DIAGRAM</th></tr>
<tr><th>$1V_{ID}$</th><th>$2V_{ID}$</th><th>S1</th><th>S0</th><th>1DE</th><th>2DE</th><th>$1V_{OD}$</th><th>$2V_{OD}$</th></tr>
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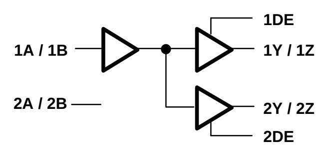
<tr><td>> 100 mV</td><td>X</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>Z</td><td rowspan="6">
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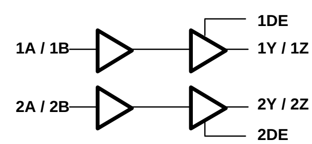
<tr><td>> 100 mV</td><td>X</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>Z</td><td rowspan="8">
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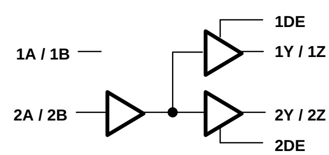
<tr><td>X</td><td>> 100 mV</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>Z</td><td rowspan="6">
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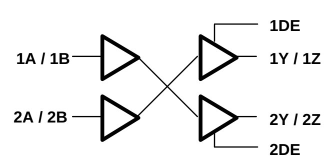
<tr><td>X</td><td>> 100 mV</td><td>H</td><td>H</td><td>H</td><td>L</td><td>H</td><td>Z</td><td rowspan="8">
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<tr><td>< -100 mV</td><td>X</td><td>H</td><td>H</td><td>L</td><td>H</td><td>Z</td><td>L</td></tr>
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(1) H = high level, L = low level, Z = high impedance, X = don't care

PARAMETER MEASUREMENT INFORMATION

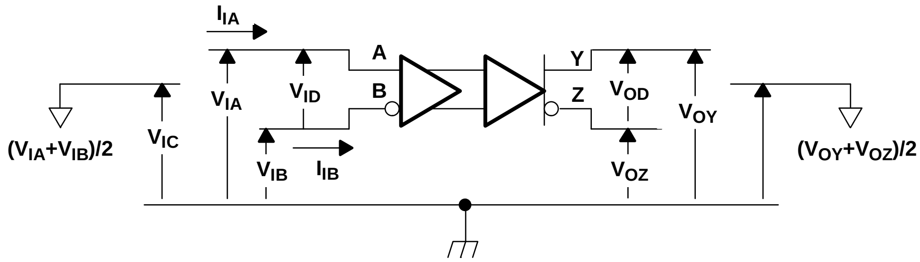


Figure 1. Voltage and Current Definitions

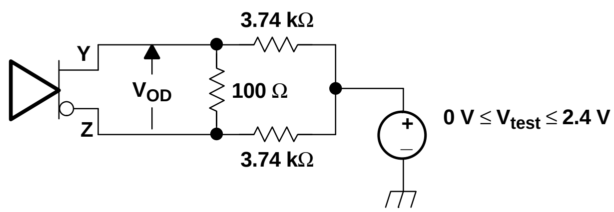
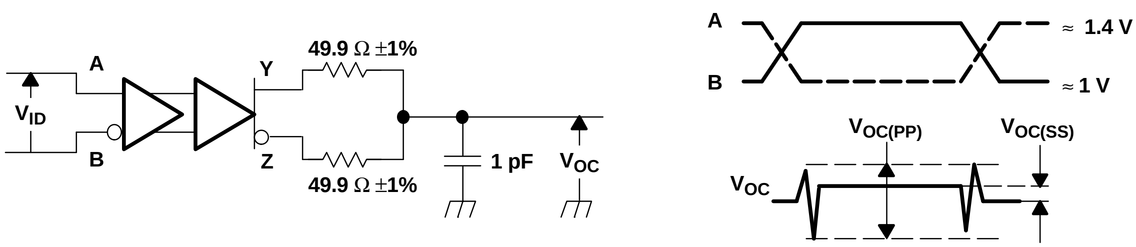
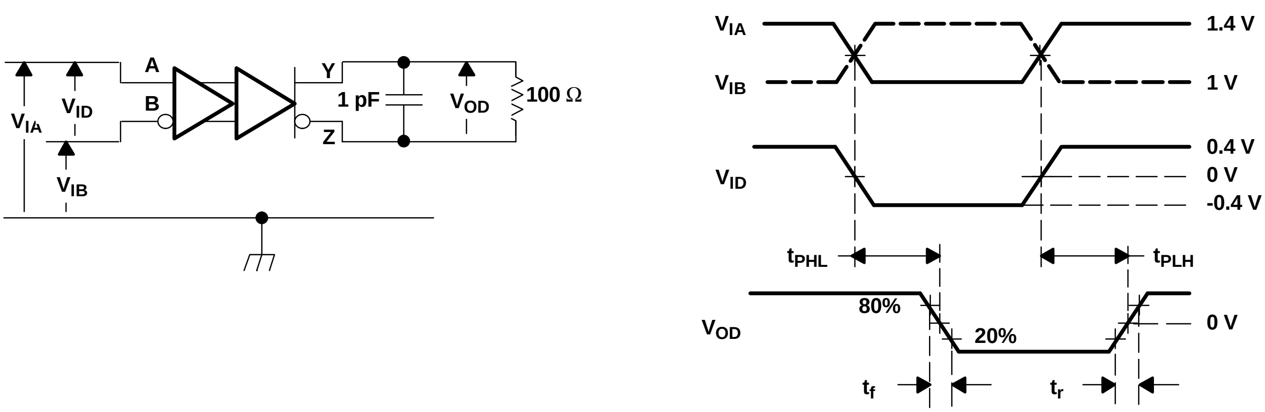


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 0.25 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100 Ω; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

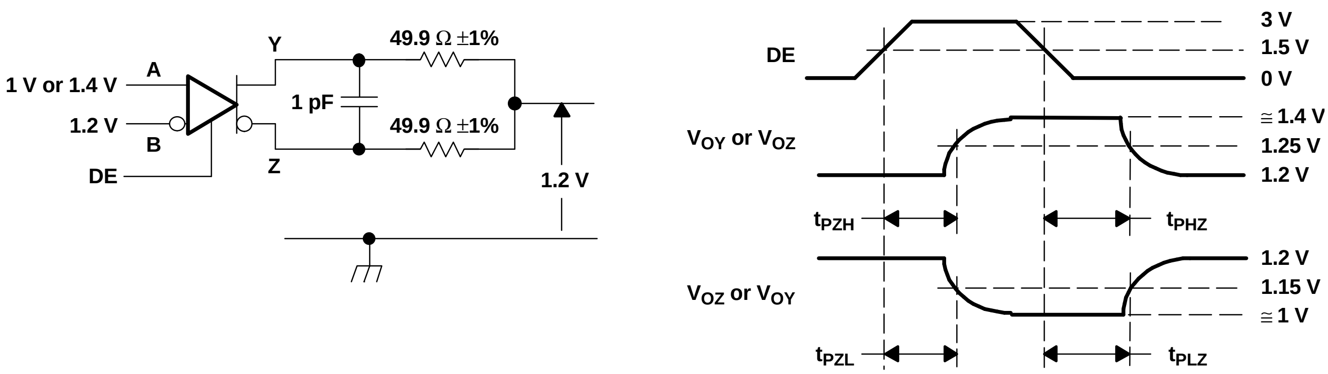
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 0.25 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

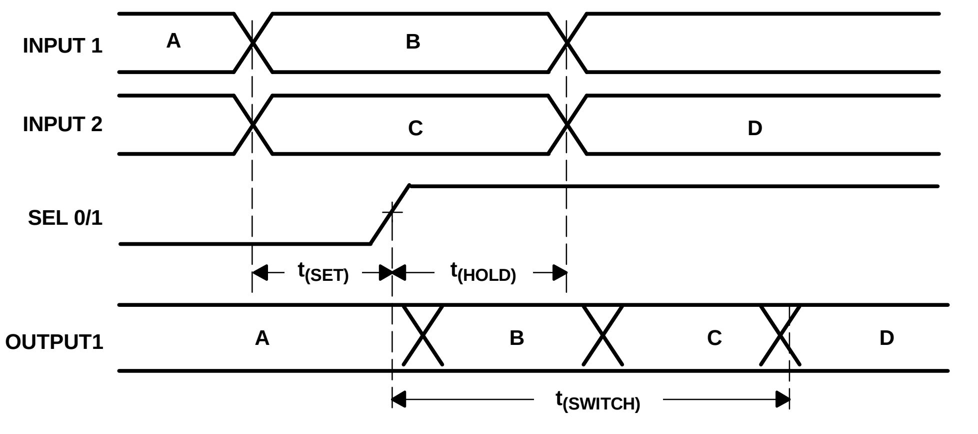


Figure 6. Example Switch, Setup, and Hold Times

PARAMETER MEASUREMENT INFORMATION (continued)

$t_{(SET)}$ and $t_{(HOLD)}$ times specify that data must be in a stable state before and after multiplex control switches.

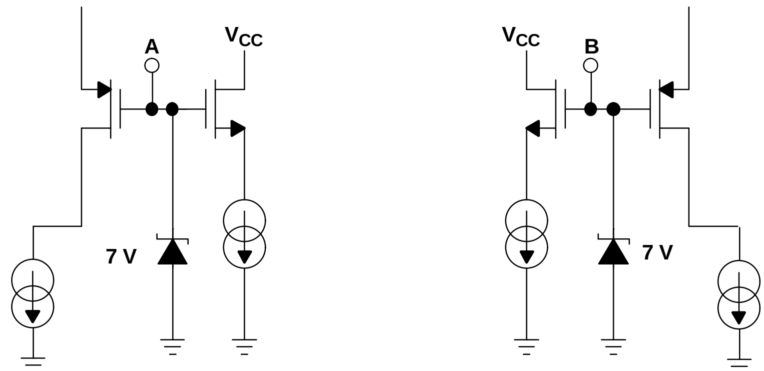
Table 1. Receiver Input Voltage Threshold Test

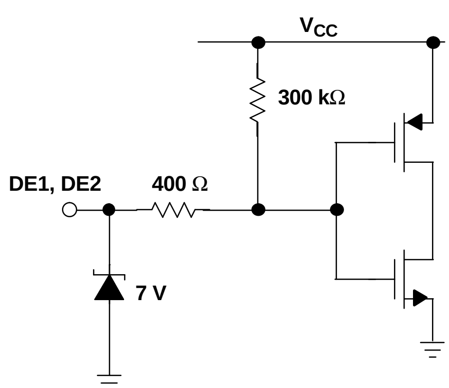
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

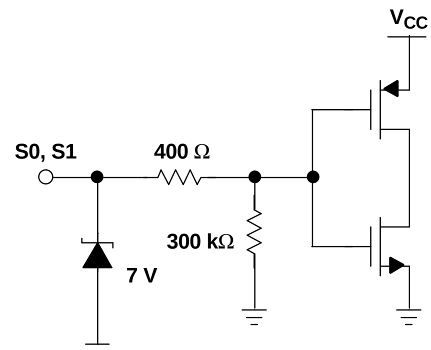
(1) H = high level, L = low level

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

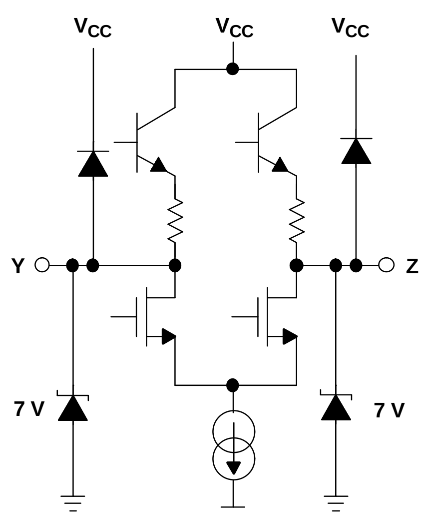
INPUT LVDS122







OUTPUT LVDS122



TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

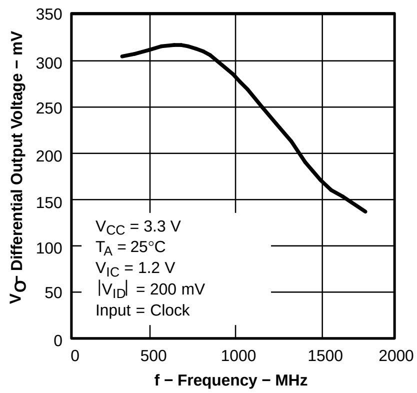


Figure 7.

DIFFERENTIAL PROPAGATION DELAY vs COMMON-MODE INPUT VOLTAGE

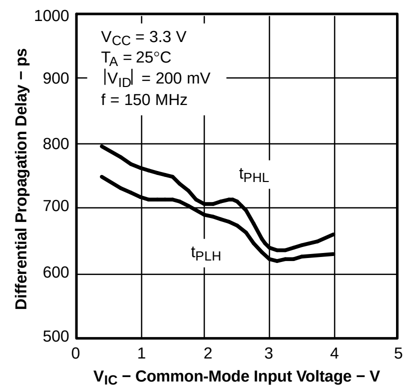


Figure 8.

DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

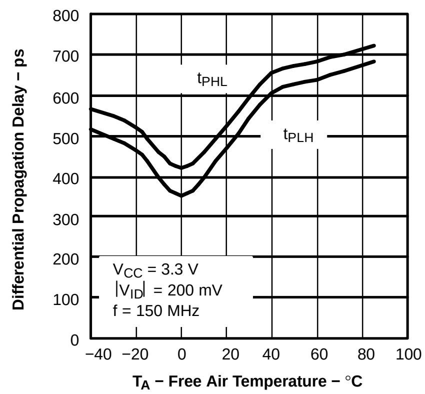


Figure 9.

PEAK-TO-PEAK JITTER vs FREQUENCY

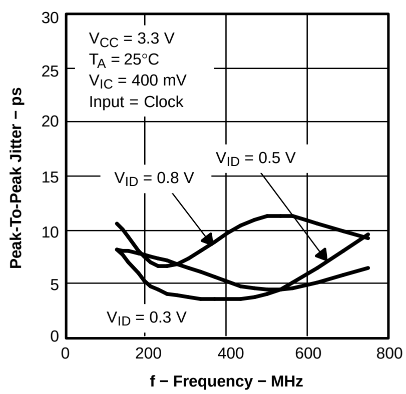


Figure 10.

PEAK-TO-PEAK JITTER vs DATA RATE

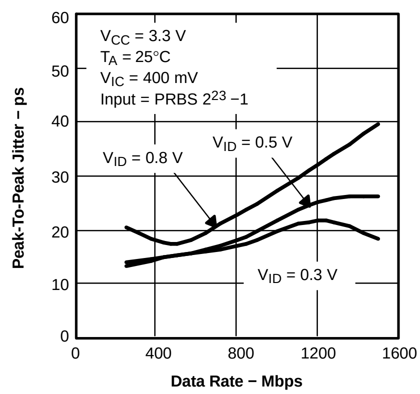


Figure 11.

PEAK-TO-PEAK JITTER vs FREQUENCY

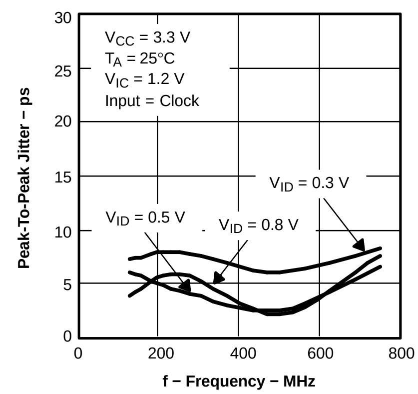


Figure 12.

PEAK-TO-PEAK JITTER vs DATA RATE

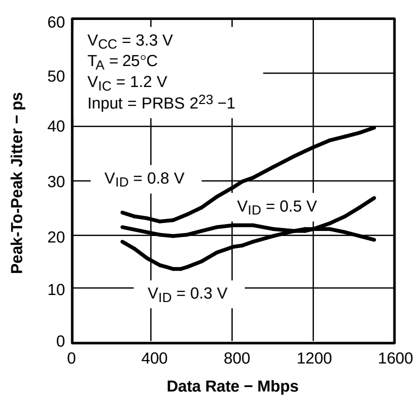


Figure 13.

PEAK-TO-PEAK JITTER vs FREQUENCY

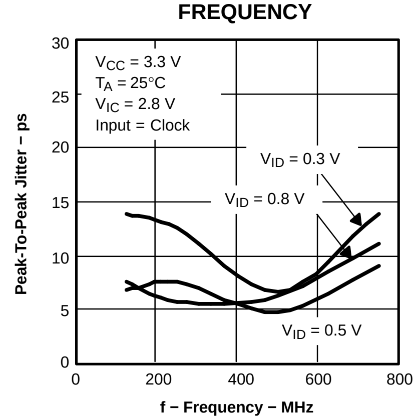


Figure 14.

PEAK-TO-PEAK JITTER vs DATA RATE

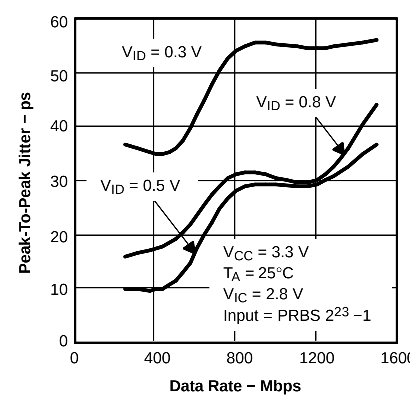


Figure 15.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK JITTER vs TEMPERATURE

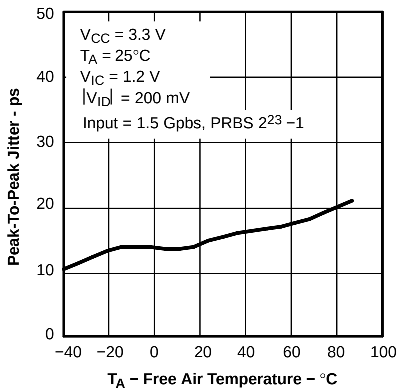


Figure 16.

PEAK-TO-PEAK JITTER vs DATA RATE

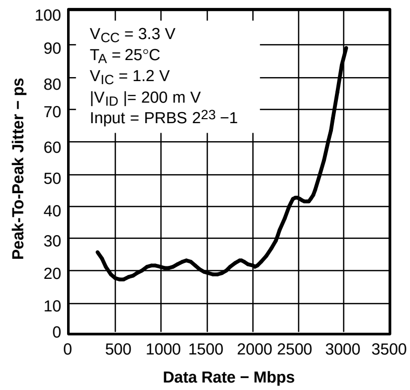
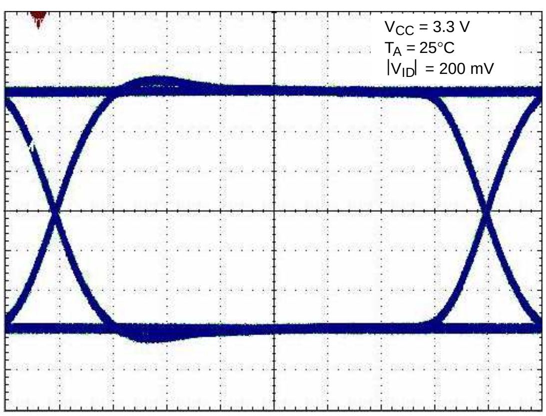


Figure 17.

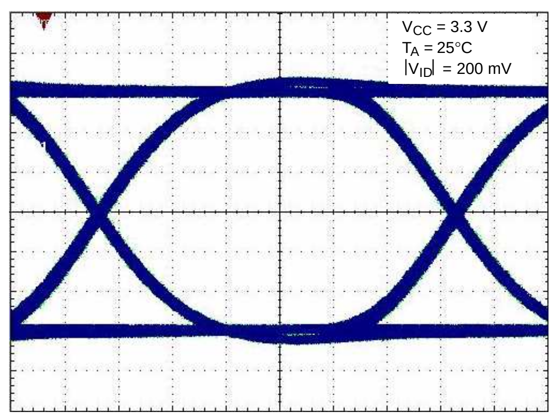
LVDS122
622 Mbps, 2^{23}– 1 PRBS



Horizontal Scale= 200 ps/div
LVPECL-to-LVDS

Figure 18.

LVDS122
1.5 Gbps, 2^{23}– 1 PRBS

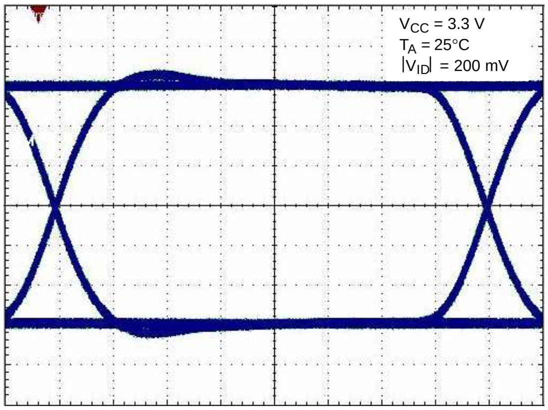


Horizontal Scale= 100 ps/div
LVPECL-to-LVDS

Figure 19.

TYPICAL CHARACTERISTICS (continued)

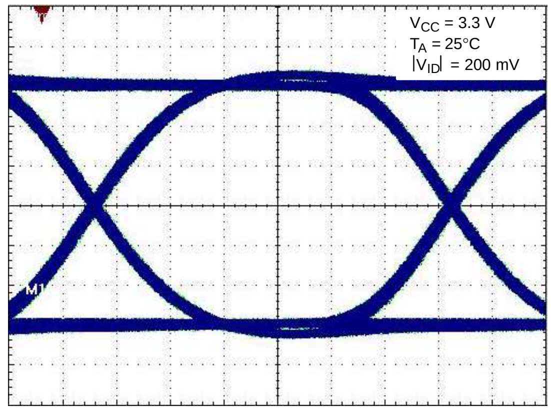
LVDS122
622 Mbps, 2^{23}– 1 PRBS



Horizontal Scale= 200 ps/div
LVDS-to-LVDS

Figure 20.

LVDS122
1.5 Gbps, 2^{23}– 1 PRBS



Horizontal Scale= 100 ps/div
LVDS-to-LVDS

Figure 21.

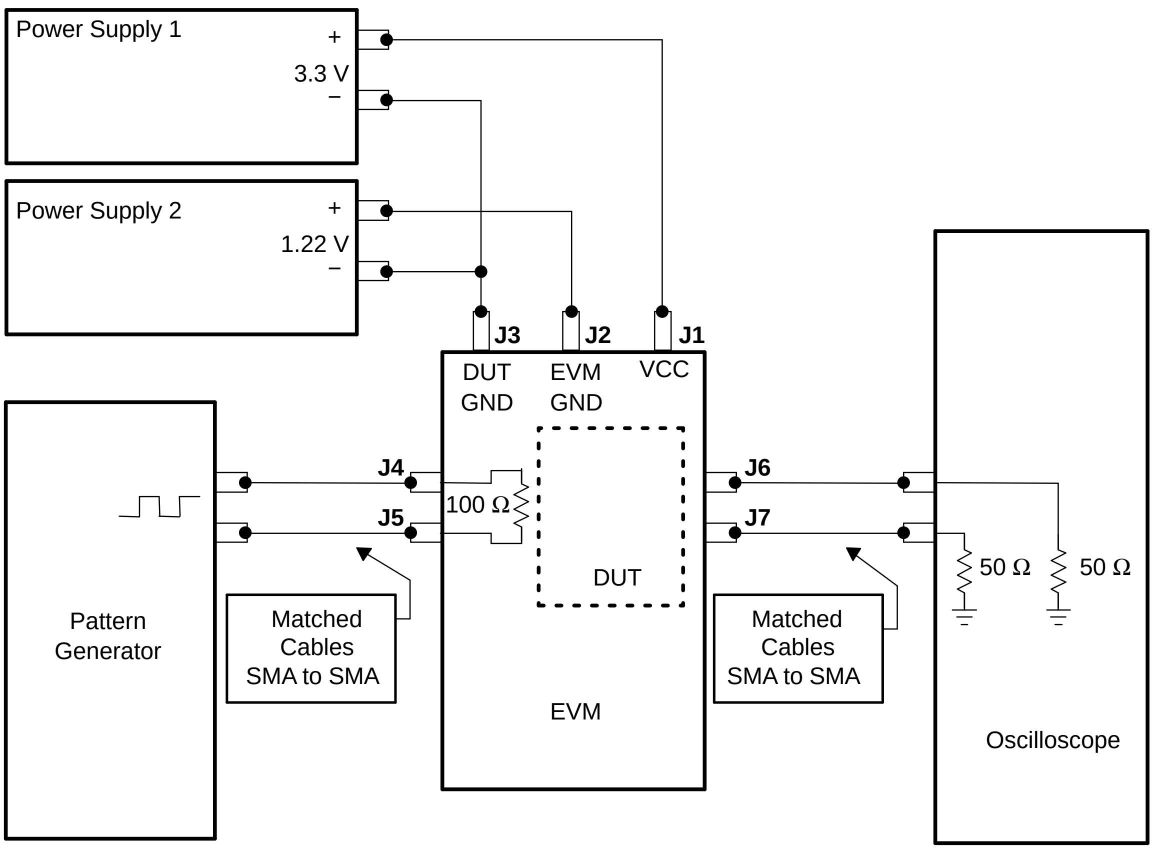


Figure 22. Jitter Setup Connections for SN65LVDS122

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

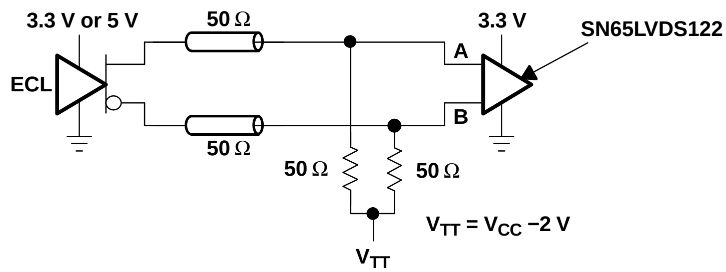


Figure 23. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

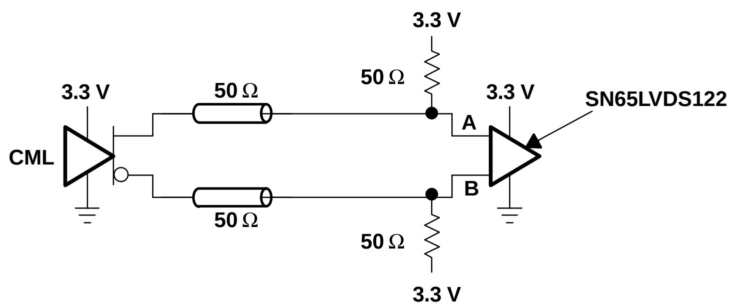


Figure 24. Current-Mode Logic (CML)

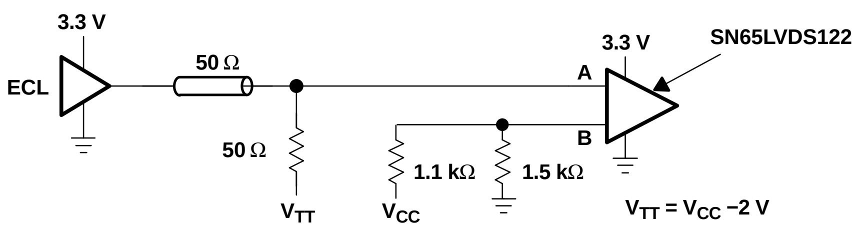


Figure 25. Single-Ended (LVPECL)

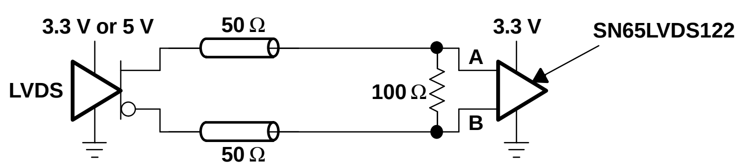


Figure 26. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS122D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS122DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS122DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS122PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS122PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS122PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT122PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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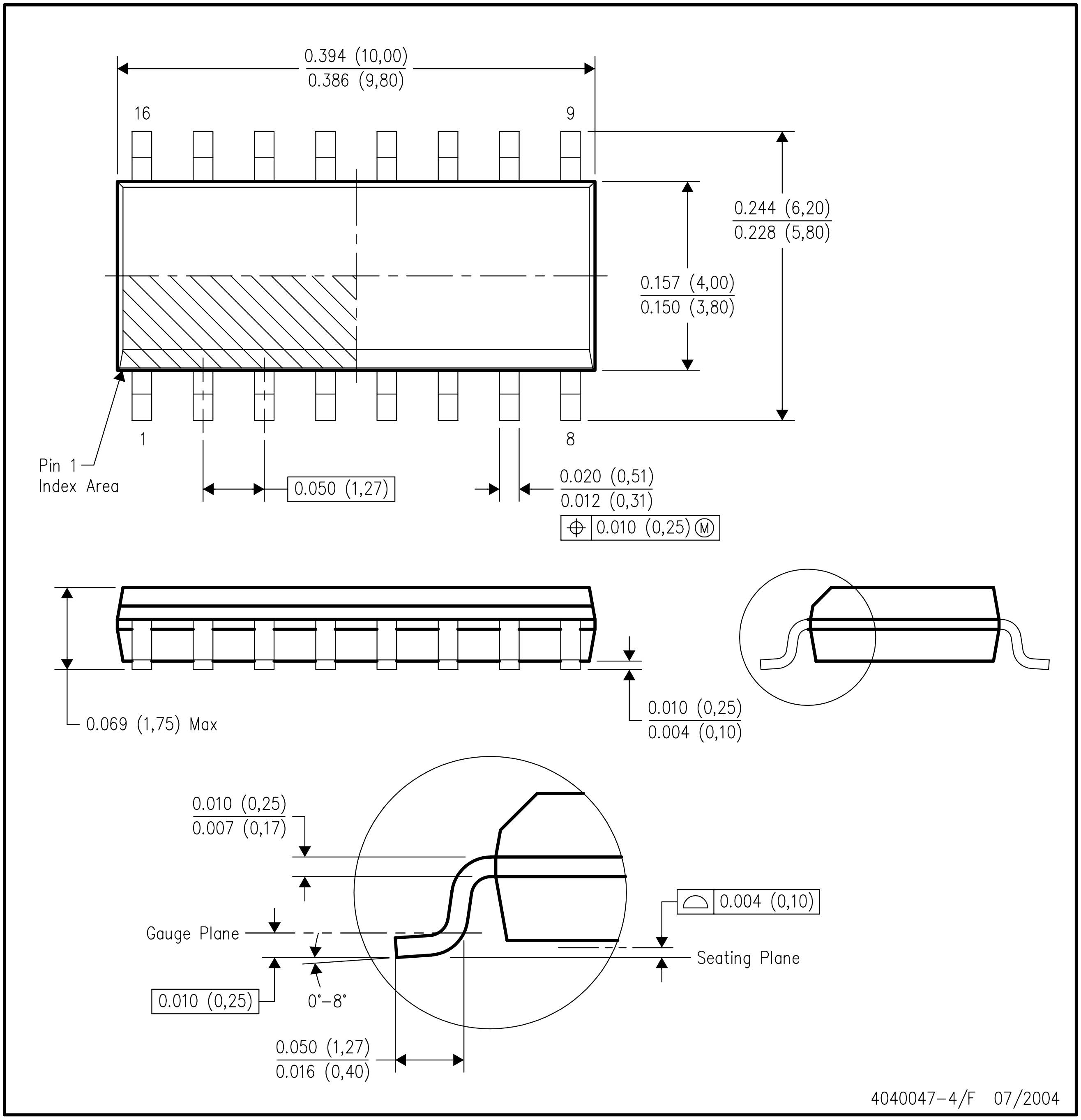
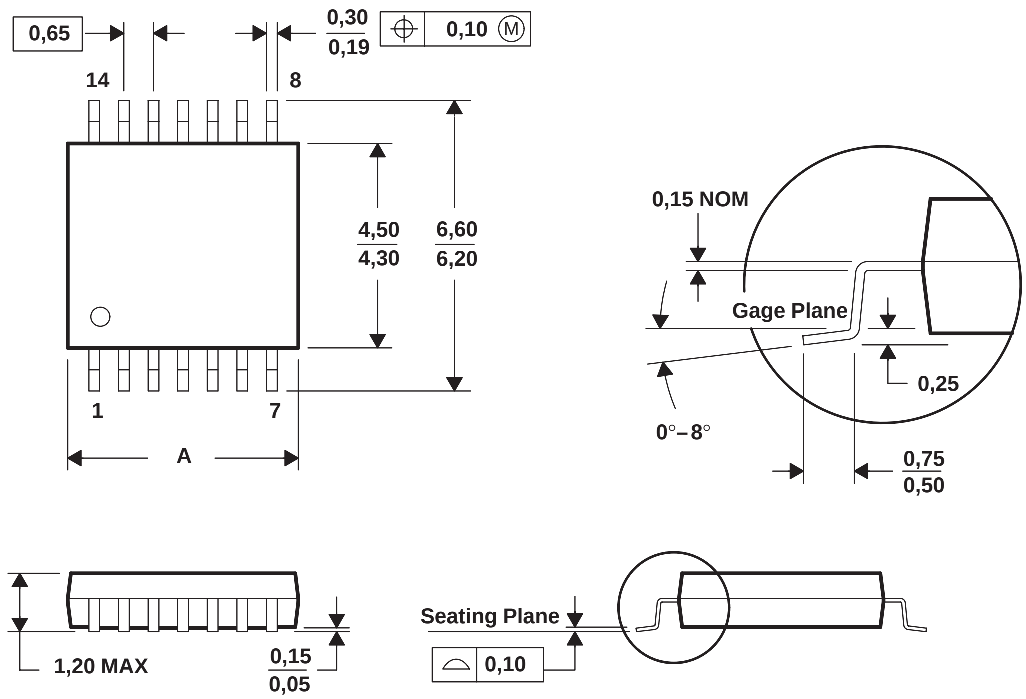
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153