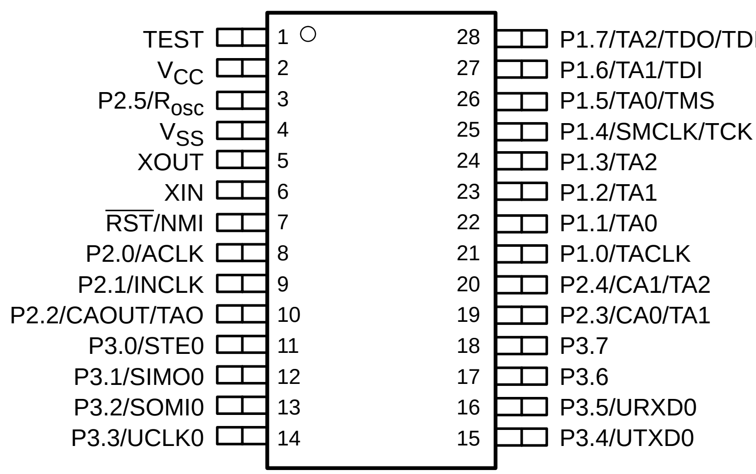
- **Low Supply Voltage Range 1.8 V – 3.6 V**
- **Ultralow-Power Consumption:**
  - **– Active Mode: 200 µA at 1 MHz, 2.2 V**
  - **– Standby Mode: 0.7 µA**
  - **– Off Mode (RAM Retention): 0.1 µA**
- **Five Power Saving Modes**
- **Wake-Up From Standby Mode in 6 µs**
- **16-Bit RISC Architecture, 125 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **– Various Internal Resistors**
  - **– Single External Resistor**
  - **– 32 kHz Crystal**
  - **– High Frequency Crystal**
  - **– Resonator**
  - **– External Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion**
- **Serial Communication Interface (USART) Software-Selects Asynchronous UART or Synchronous SPI**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Family Members Include:**
  MSP430F122: 4KB + 256B Flash Memory 256B RAM
  MSP430F123: 8KB + 256B Flash Memory 256B RAM
- **Available in a 28-Pin Plastic Small-Outline Wide Body (SOWB) Package and 28-Pin Plastic Thin Shrink Small-Outline Package (TSSOP)**
- **For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

DW OR PW PACKAGE
(TOP VIEW)



description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6µs.

description (continued)

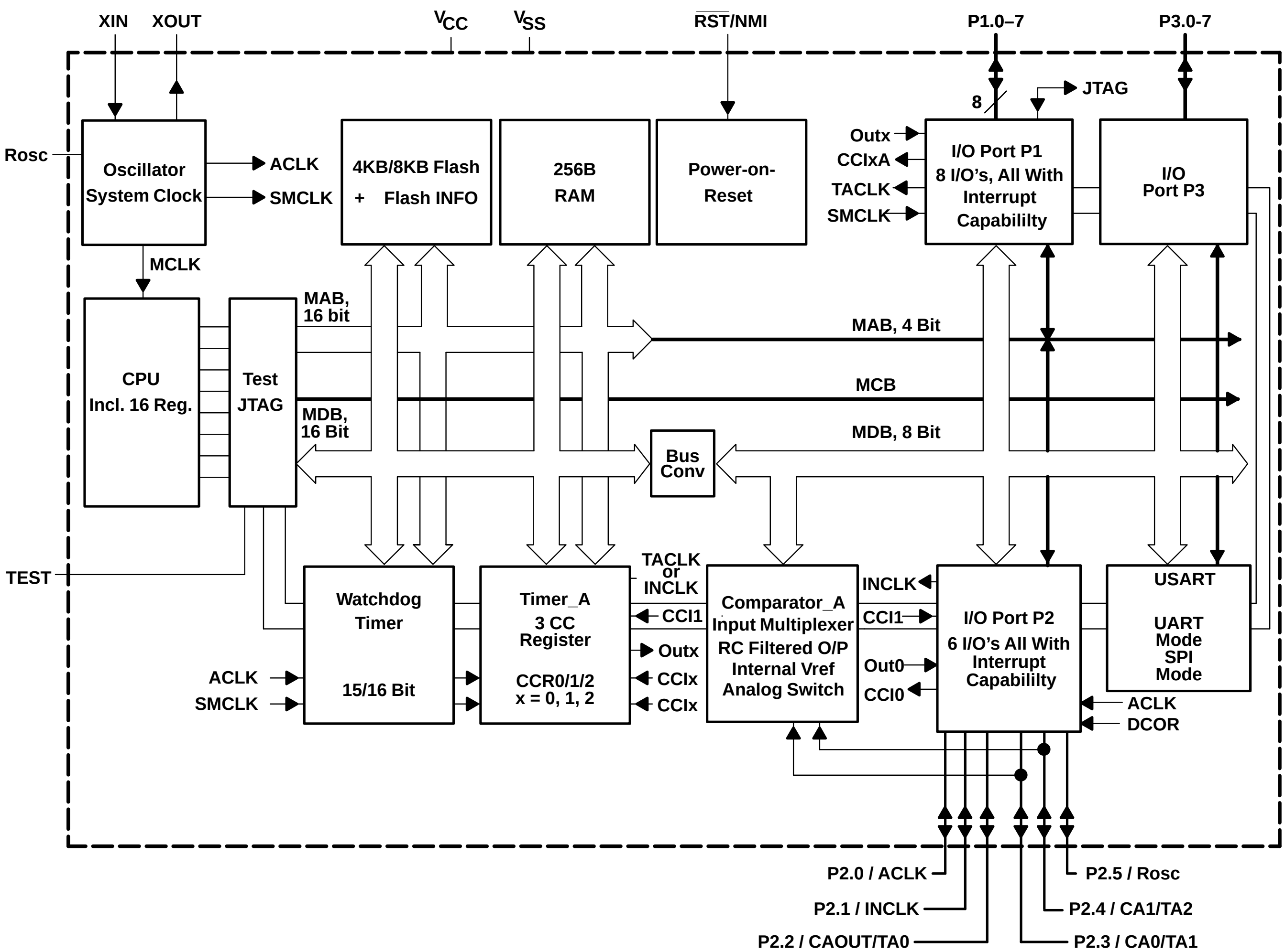
The MSP430F12x series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer and twenty-two I/O pins.The MSP430F12x series also has a built-in communication capability using asynchronous (UART) and synchronous (SPI) protocols in addition to a versatile analog comparator.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. Stand alone RF sensor front end is another area of application. The I/O port inputs provide single slope A/D conversion capability on resistive sensors.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 28-PIN SOWB (DW)	PLASTIC 28-PIN TSSOP (PW)
–40°C to 85°C	MSP430F122IDW MSP430F123IDW	MSP430F122IPW MSP430F123IPW

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
P1.0/TACLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	25	I/O	General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test
P1.5/TA0/TMS	26	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test
P1.6/TA1/TDI	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input terminal
P1.7/TA2/TDO/TDI†	28	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming
P2.0/ACLK	8	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	10	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/comparator_A, output
P2.3/CA0/TA1	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/comparator_A, input
P2.4/CA1/TA2	20	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/comparator_A, input
P2.5/R_{OSC}	3	I/O	General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency
P3.0/STE0	11	I/O	General digital I/O, slave transmit enable—USART0/SPI mode
P3.1/SIMO0	12	I/O	General digital I/O, slave in/master out of USART0/SPI mode
P3.2/SOMI0	13	I/O	General digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0	14	I/O	General digital I/O, external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode clock input
P3.4/UTXD0	15	I/O	General digital I/O, transmit data out—USART0/UART mode
P3.5/URXD0	16	I/O	General digital I/O, receive data in—USART0/UART mode
P3.6	17	I/O	General digital I/O
P3.7	18	I/O	General digital I/O
$\overline{RST}$/NMI	7	I	Reset or nonmaskable interrupt input
TEST	1	I	Select of test mode for JTAG pins on Port1
V_{CC}	2		Supply voltage
V_{SS}	4		Ground reference
XIN	6	I	Input terminal of crystal oscillator
XOUT	5	I/O	Output terminal of crystal oscillator

† TDO or TDI is selected via JTAG instruction.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV and MEM,and TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the memory with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	WDTIFG (see Note1) KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI, oscillator fault, flash memory access violation	NMIIFG (see Notes 1 and 4) OFIFG (see Notes 1 and 4) ACCVIFG (see Notes 1 and 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A	CAIFG	maskable	0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
Timer_A	TACCR0 CCIFG (see Note 2)	maskable	0FFF2h	9
Timer_A	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2)	maskable	0FFF0h	8
USART0 receive	URXIFG0	maskable	0FFEEh	7
USART0 transmit	UTXIFG0	maskable	0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags – see Note 3)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) are implemented on the ’12x devices.
4. (non)-maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h							UTXIE0	URXIE0
							rw-0	rw-0

URXIE0: USART0, UART, and SPI receive-interrupt enable

UTXIE0: USART0, UART, and SPI transmit-interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-0

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h							UTXIFG0	URXIFG0
							rw-0	rw-0

URXIFG0: USART0, UART, and SPI receive flag

UTXIFG0: USART0, UART, and SPI transmit flag

module enable registers 1 and 2

Address 04h	7	6	5	4	3	2	1	0

Address 05h	7	6	5	4	3	2	1	0
							UTXE0	URXE0 USPIE0
							rw-0	rw-0

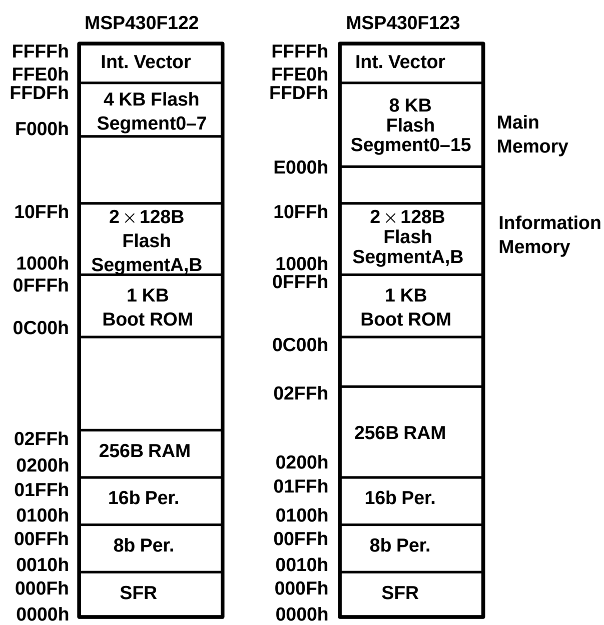
URXE0: USART0, UART receive enable

UTXE0: USART0, UART transmit enable

USPIE0: USART0, SPI (synchronous peripheral interface) transmit and receive enable

Legend		
	rw:	Bit can be read and written.
	rw-0:	Bit can be read and written. It is reset by PUC
	(shaded box)	SFR bit is not present in device.

memory organization



bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions.

oscillator and system clock

The clock system in the MSP430x12x devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

digital I/O

There are three 8-bit I/O ports implemented—ports P1, P2, and P3 (only six port P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE:
Six bits of port P2, P2.0 to P2.5, are available on external pins – but all control and data bits for port P2 are implemented. Port P3 has no interrupt capability.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

USART0

The MSP430x12x devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

comparator_A

The primary function of the comparator_A module is to support precision slope analog–to–digital conversions, battery–voltage supervision, and monitoring of external analog signals.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Basic Clock	Basic clock sys. control2	BCSCTL2	058h
	Basic clock sys. control1	BCSCTL1	057h
	DCO clock freq. control	DCOCTL	056h
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	Module enable2	ME2	005h
	Module enable1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . –0.3 V to 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . –40°C to 85°C

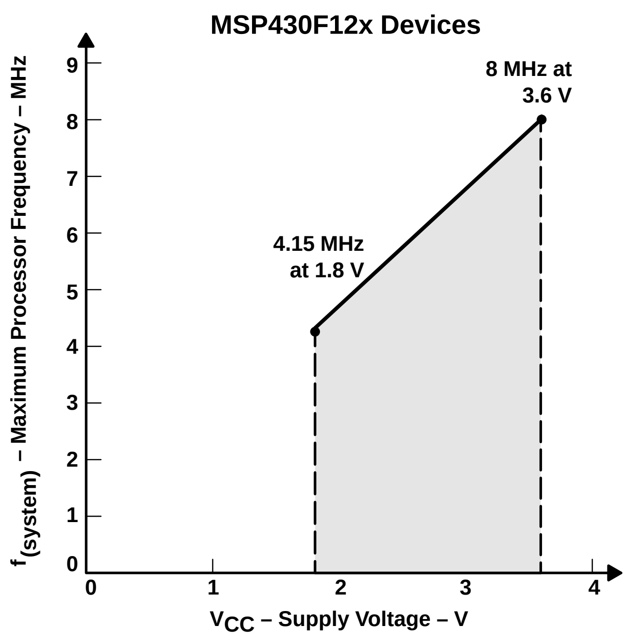
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (see Note 1)		MSP430F12x	1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		MSP430F12x	2.7		3.6	V
Supply voltage, V_{SS}				0		V
Operating free-air temperature range, T_A		MSP430F12x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF mode selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected mode, XTS=1	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency $f_{(system)}$ (MCLK signal)		V_{CC} = 1.8 V, MSP430F12x	dc		4.15	MHz
		V_{CC} = 3.6 V, MSP430F12x	dc		8	
Flash timing generator frequency, $f_{(FTG)}$		MSP430F12x	257		476	kHz
Cumulative program time, block write, $t_{(CPT)}$ (see Note 3)		V_{CC} = 2.7 V/3.6 V MSP430F12x			3	ms
Low-level input voltage (TEST, $\overline{RST}$/NMI), V_{IL} (excluding XIN, XOUT)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS}+0.6	V
High-level input voltage (TEST, $\overline{RST}$/NMI), V_{IH} (excluding XIN, XOUT)		V_{CC} = 2.2 V/3 V	0.8V_{CC}		V_{CC}	V
Input levels at XIN, XOUT	$V_{IL(XIN, XOUT)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{CC}	V
	$V_{IH(XIN, XOUT)}$		0.8×V_{CC}		V_{CC}	

NOTES: 1. The LFXT1 oscillator in LF-mode requires a resistor of 5.1 MΩ from XOUT to V_{SS} when V_{CC} <2.5 V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 4 MHz at $V_{CC} \geq 2.2$ V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 8 MHz at $V_{CC} \geq 2.8$ V.
2. The LFXT1 oscillator in LF-mode requires a watch crystal.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal.
3. The cumulative program time must not be exceeded during a block-write operation.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.7 V.

Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode	T_A = –40°C +85°C, $f_{MCLK} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, Program executes in Flash	V_{CC} = 2.2 V		200	250	μA
			V_{CC} = 3 V		300	350	
		T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz, Program executes in Flash	V_{CC} = 2.2 V		3	5	μA
			V_{CC} = 3 V		11	18	
$I_{(CPUOff)}$	Low-power mode, (LPM0)	T_A = –40°C +85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz	V_{CC} = 2.2 V		32	45	μA
			V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2)	T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0	V_{CC} = 2.2 V		11	14	μA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3)	T_A = –40°C	V_{CC} = 2.2 V		0.8	1.2	μA
		T_A = 25°C			0.7	1	
		T_A = 85°C			1.6	2.3	
		T_A = –40°C	V_{CC} = 3 V		1.8	2.2	μA
		T_A = 25°C			1.6	1.9	
		T_A = 85°C			2.3	3.4	
$I_{(LPM4)}$	Low-power mode, (LPM4)	T_A = –40°C	V_{CC} = 2.2 V/3 V		0.1	0.5	μA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	1.9	

NOTE: All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

current consumption of active mode versus system frequency

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

current consumption of active mode versus supply voltage

$$I_{AM} = I_{AM[3\ V]} + 120\ \mu A/V \times (V_{CC} - 3\ V)$$

Schmitt-trigger inputs Port P1 to Port P3; P1.0 to P1.7, P2.0 to P2.5, P3.0 to P3.7

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis, ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs Port 1 to P3; P1.0 to P1.7, P2.0 to P2.5, P3.0 to P3.7

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –6 mA		See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 3 V	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA		See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 3 V	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

outputs – Ports P1, P2, and P3

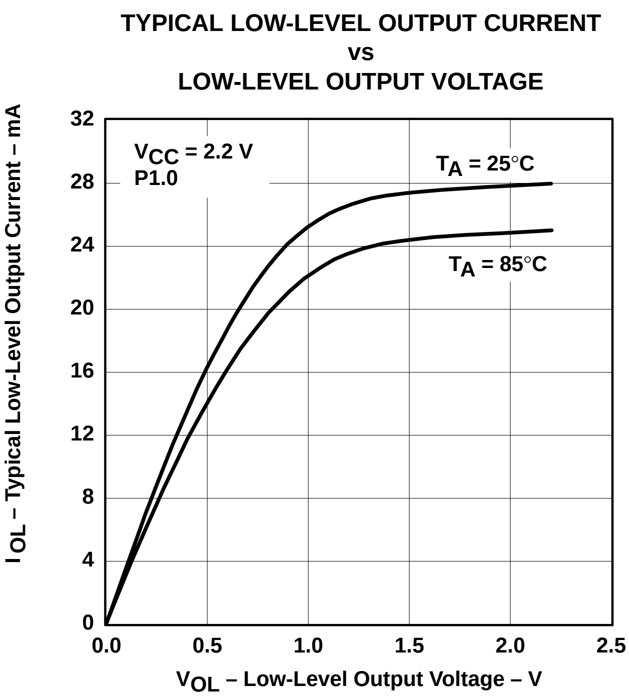


Figure 2

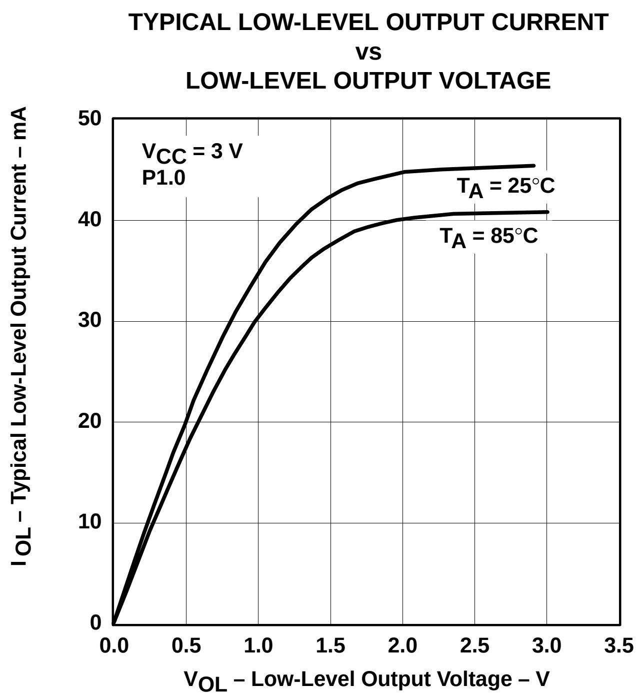


Figure 3

NOTE: Only one output is loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, and P3 (continued)

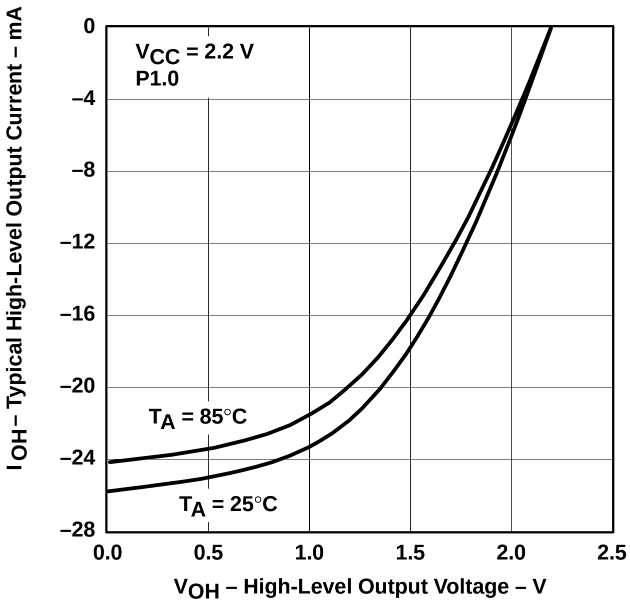


Figure 4

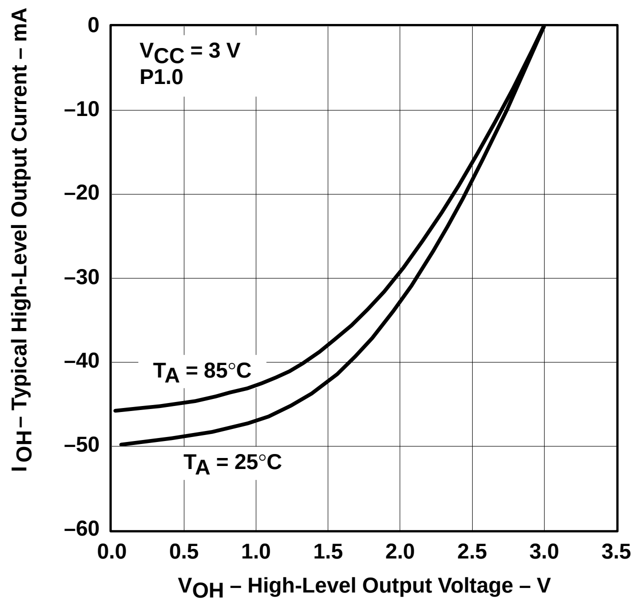


Figure 5

NOTE: Only one output is loaded at a time.

leakage current

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	Port P1: P1.x, 0 ≤ × ≤ 7 (see Notes 1 and 2)	2.2 V/3 V			±50	nA
		Port P2: P2.x, 0 ≤ × ≤ 5 (see Notes 1 and 2)	2.2 V/3 V			±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2 (see Note 2)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $T_{(H)} = T_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.
2. The external capture signal triggers the capture event every time the mimimum $t_{(cap)}$ cycle and time parameters are met. A capture may be triggered with capture signals even shorter than $t_{(cap)}$. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

USART (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 1: The signal applied to the USART receive signal/terminal (URXD) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD line.

outputs P1.x, P2.x, P3.x, TAx

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{(P20)}$	Output frequency	P2.0/ACLK,	C_L = 20 pF	2.2 V/3 V			f_{System}	MHz
$f_{(TAx)}$		TA0, TA1, TA2, Internal clock source, SMCLK signal applied (see Note 1)	C_L = 20 pF,	2.2 V/3 V	dc		f_{System}	
$t_{(Xdc)}$	Duty cycle of O/P frequency	P1.4/SMCLK, C_L = 20 pF	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$		35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$		50%– 15 ns	50%	50%+ 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	2.2 V/3 V	50%– 15 ns	50%	50%+ 15 ns	
		P2.0/ACLK, C_L = 20 pF	$f_{P20} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{P20} = f_{LFXT1} = f_{LF}$		30%		70%	
			$f_{P20} = f_{LFXT1/n}$			50%		
$t_{(TAdc)}$		TA0, TA1, TA2,	C_L = 20 pF, Duty cycle = 50%	2.2 V/3 V		0	±50	ns

NOTE 1: The limits of the system clock MCLK has to be met. MCLK and SMCLK can have different frequencies.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage at 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage at 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	2.2 V	160	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

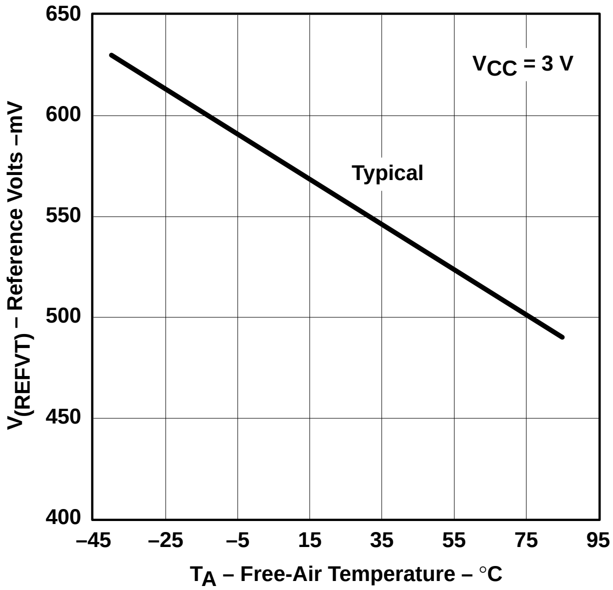


Figure 6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

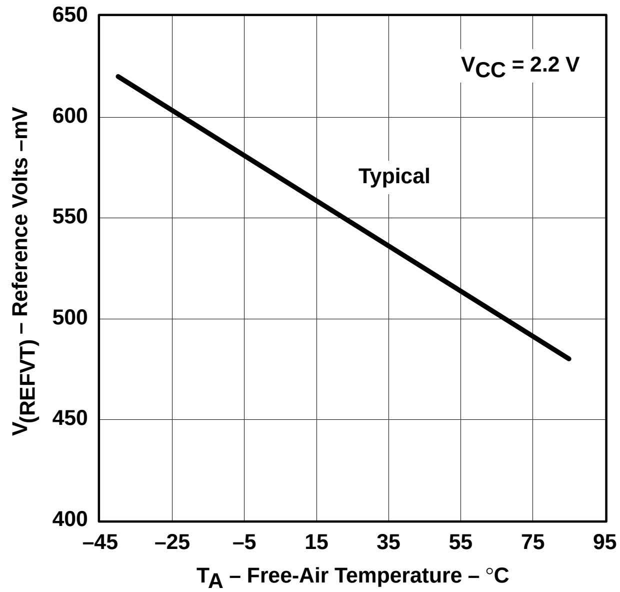


Figure 7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

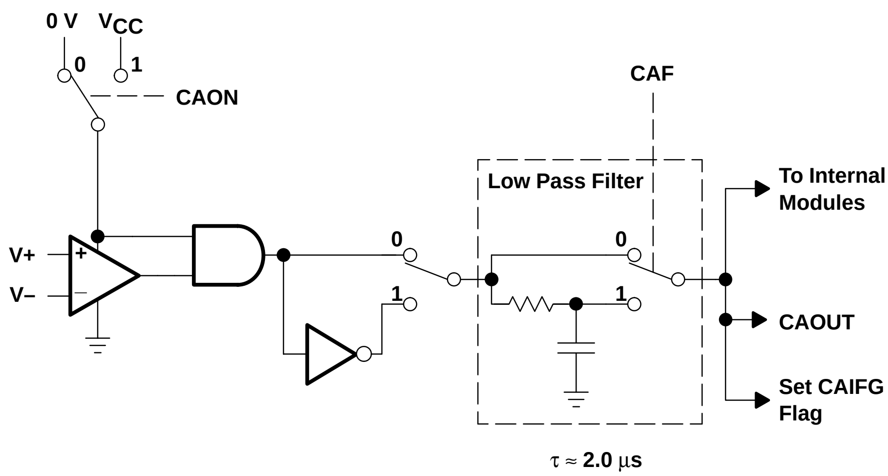


Figure 8. Block Diagram of Comparator_A Module

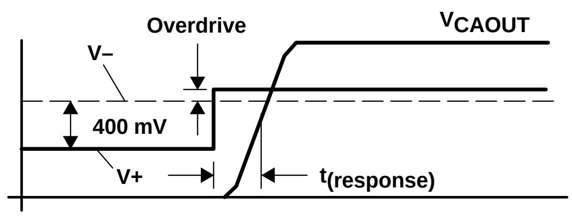


Figure 9. Overdrive Definition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(POR\_Delay)}$	POR		V_{CC} = 2.2 V/3 V		150	250	µs
V_{POR}	POR	T_A = –40°C	V_{CC} = 2.2 V/3 V	1.4		1.8	V
V_{POR}	POR	T_A = 25°C	V_{CC} = 2.2 V/3 V	1.1		1.5	V
V_{POR}	POR	T_A = 85°C	V_{CC} = 2.2 V/3 V	0.8		1.2	V
$V_{(min)}$	POR		V_{CC} = 2.2 V/3 V	0		0.4	V
$t_{(reset)}$	PUC/POR	Reset is accepted internally	V_{CC} = 2.2 V/3 V	2			µs

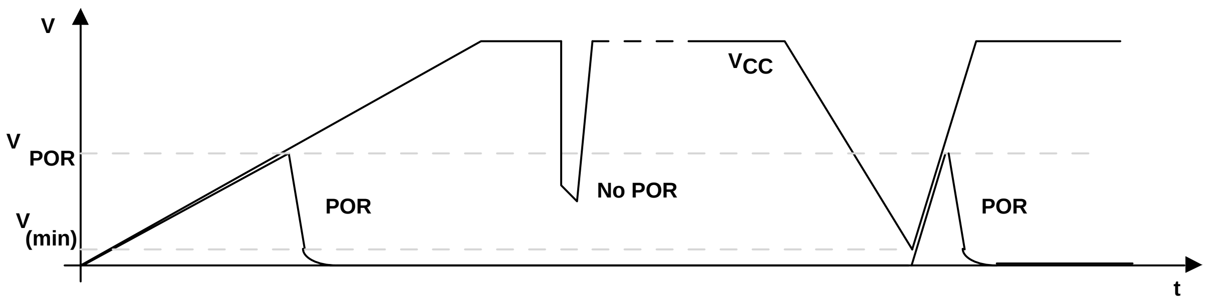


Figure 10. Power-On Reset (POR) vs Supply Voltage

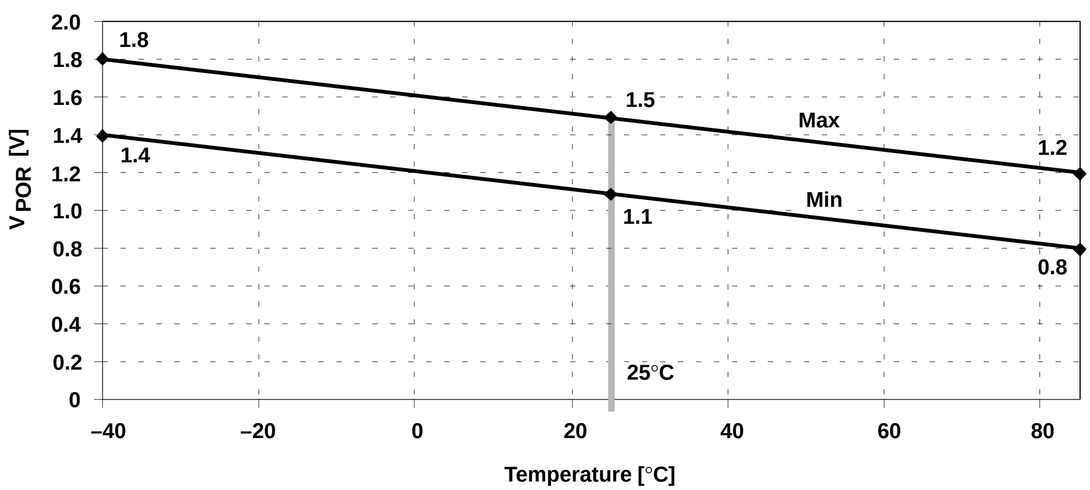


Figure 11. V_{POR} vs Temperature

RAM

PARAMETER		MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator,LFXT1

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{(XIN)}$	Input capacitance	XTS=0; LF mode selected	2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected (see Note 1)	2.2 V / 3 V		2		
$C_{(XOUT)}$	Output capacitance	XTS=0; LF mode selected	2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected (see Note 1)	2.2 V / 3 V		2		

NOTE 1: Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.08	0.12	0.15	MHz
		3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.14	0.19	0.23	MHz
		3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.22	0.30	0.36	MHz
		3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.37	0.49	0.59	MHz
		3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.61	0.77	0.93	MHz
		3 V	0.61	0.75	0.9	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	1	1.2	1.5	MHz
		3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	1.6	1.9	2.2	MHz
		3 V	1.69	2	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	2.4	2.9	3.4	MHz
		3 V	2.7	3.2	3.65	
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	4	4.5	4.9	MHz
		3 V	4.4	4.9	5.4	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V/3 V	F_{DCO40} x1.7	F_{DCO40} x2.1	F_{DCO40} x2.5	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	2.2 V/3 V	1.35	1.65	2	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	2.2 V	–0.31	–0.36	–0.40	%/°C
		3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	2.2 V/3 V	0	5	10	%/V

NOTES: 1. These parameters are not production tested.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

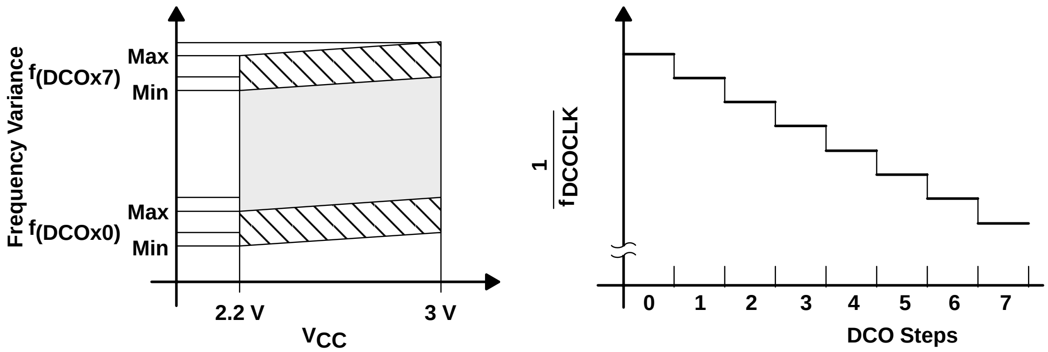


Figure 12. DCO Characteristics

principle characteristics of the DCO

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices
- The DCO control bits DCO0, DCO1 and DCO2 have a step size as defined in parameter S_{DCO}.
- The modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. f_{DCO} is used for the remaining cycles. The frequency is an average = $f_{DCO} \times (2^{MOD/32})$.
- All ranges selected by $R_{sel(n)}$ overlap with $R_{sel(n+1)}$: R_{sel0} overlaps with R_{sel1}, ... R_{sel6} overlaps with R_{sel7}.

wake-up from lower power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM0)}$	Delay time (see Note 1)	V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM2)}$		V_{CC} = 2.2 V/3 V			100		
$t_{(LPM3)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	
$t_{(LPM4)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	

NOTE 1: Parameter applicable only if DCOCLK is used for MCLK.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

JTAG, program memory and fuse

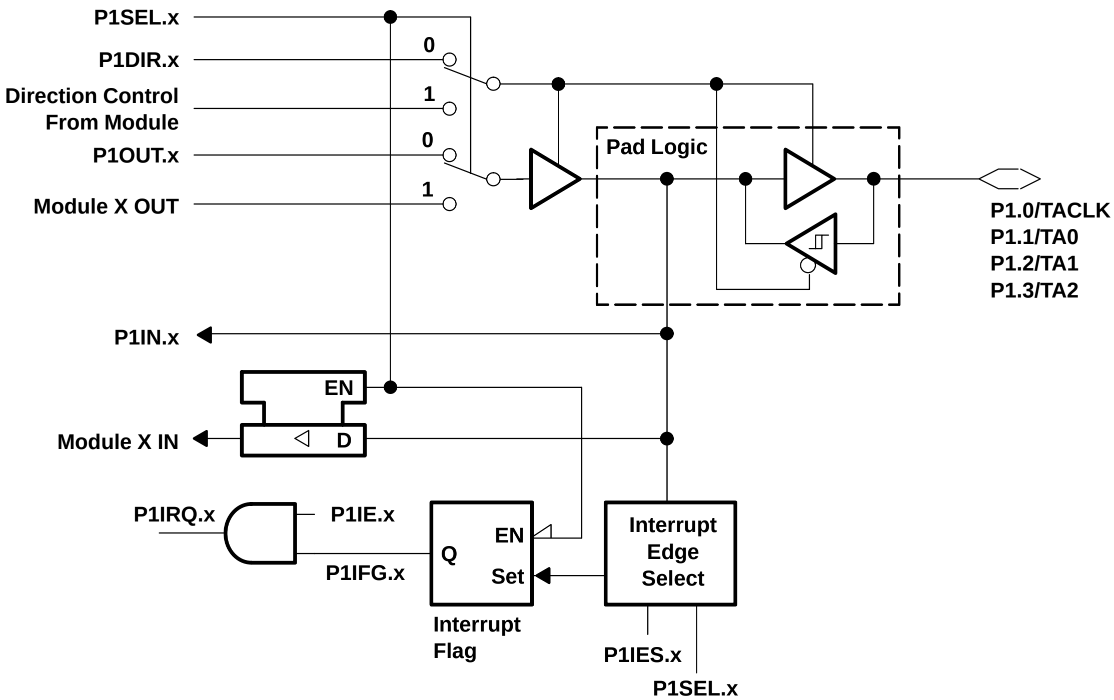
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(TCK)}$	TCK frequency, JTAG/test (see Note 3)	V_{CC} = 2.2 V	dc		5	MHz
		V_{CC} = 3 V	dc		10	
$V_{CC(FB)}$	Supply voltage during fuse-blow condition, $T_{(A)}$ = 25°C		2.5			V
$V_{(FB)}$	Fuse blow voltage (see Notes 1 and 2)		6		7	V
$I_{(FB)}$	Supply current on TEST during fuse blow (see Note 2)				100	mA
$t_{(FB)}$	Time to blow the fuse (see Note 2)				1	ms
$I_{(DD-PGM)}$	Current during program cycle (see Note 4)	V_{CC} = 2.7 V/3.6 V		3	5	mA
$I_{(DD-ERASE)}$	Current during erase cycle (see Note 4)	V_{CC} = 2.7 V/3.6 V		3	7	mA
$t_{(retention)}$	Write/erase cycles		10^4	10^5		
	Data retention T_J = 25°C		100			Year

NOTES:
1. The power source to blow the fuse is applied to TEST pin.
2. Once the JTAG fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
3. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected.
4. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:
   $t_{(word\ write)} = 35 \times 1/f_{(FTG)}$
   $t_{(block\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
   $t_{(block\ write,\ bytes\ 1–63)} = 20 \times 1/f_{(FTG)}$
   $t_{(block\ write\ end\ sequence)} = 6 \times 1/f_{(FTG)}$
   $t_{(mass\ erase)} = 5297 \times 1/f_{(FTG)}$
   $t_{(segment\ erase)} = 4819 \times 1/f_{(FTG)}$

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



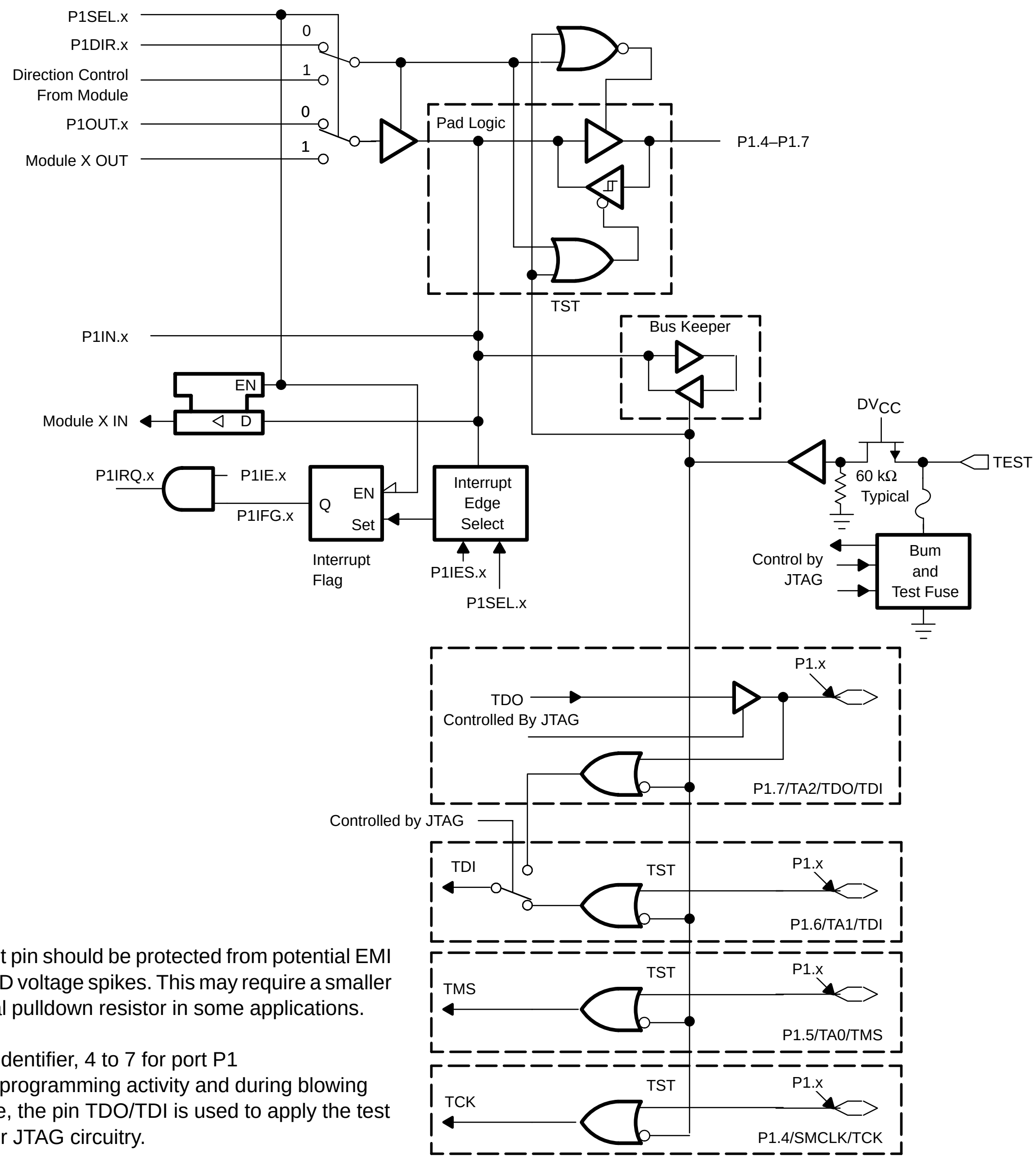
NOTE: x = Bit/identifier, 0 to 3 for port P1

P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	V_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

APPLICATION INFORMATION

Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

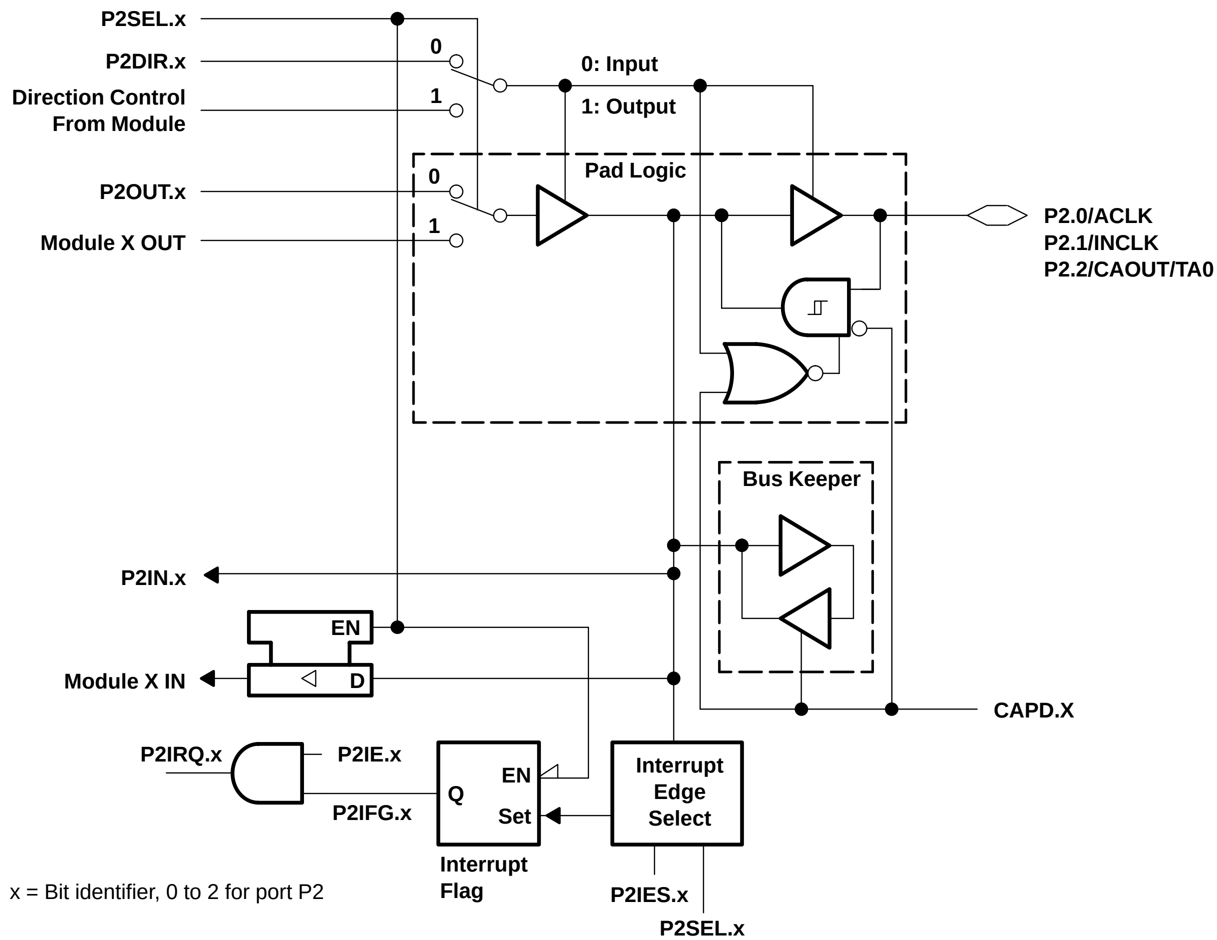
x = Bit identifier, 4 to 7 for port P1
During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

APPLICATION INFORMATION

Port P2, P2.0 to P2.2, input/output with Schmitt-trigger



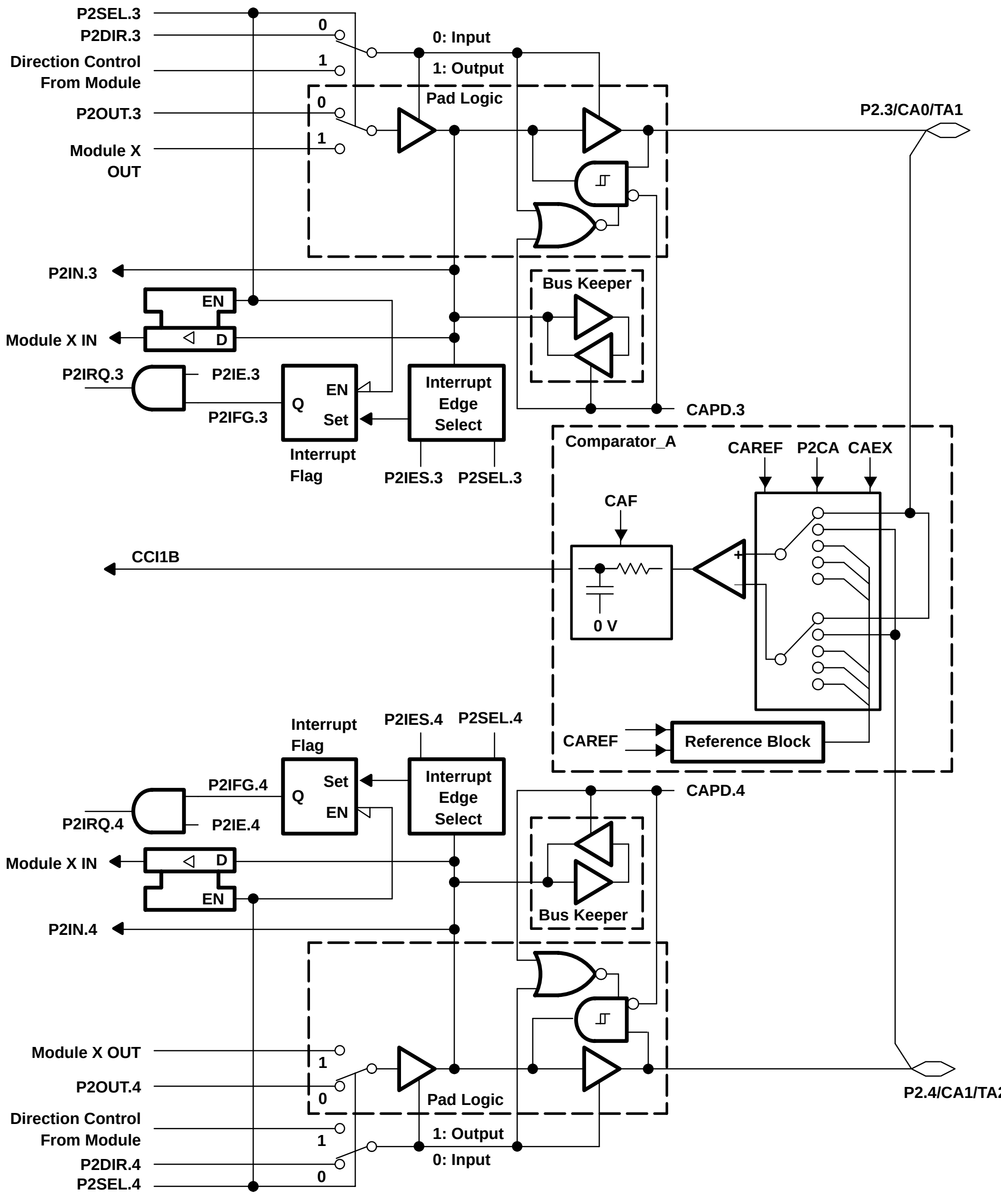
NOTE: x = Bit identifier, 0 to 2 for port P2

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	V_{SS}	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2

† Signal from or to Timer_A

APPLICATION INFORMATION

Port P2, P2.3 to P2.4, input/output with Schmitt-trigger

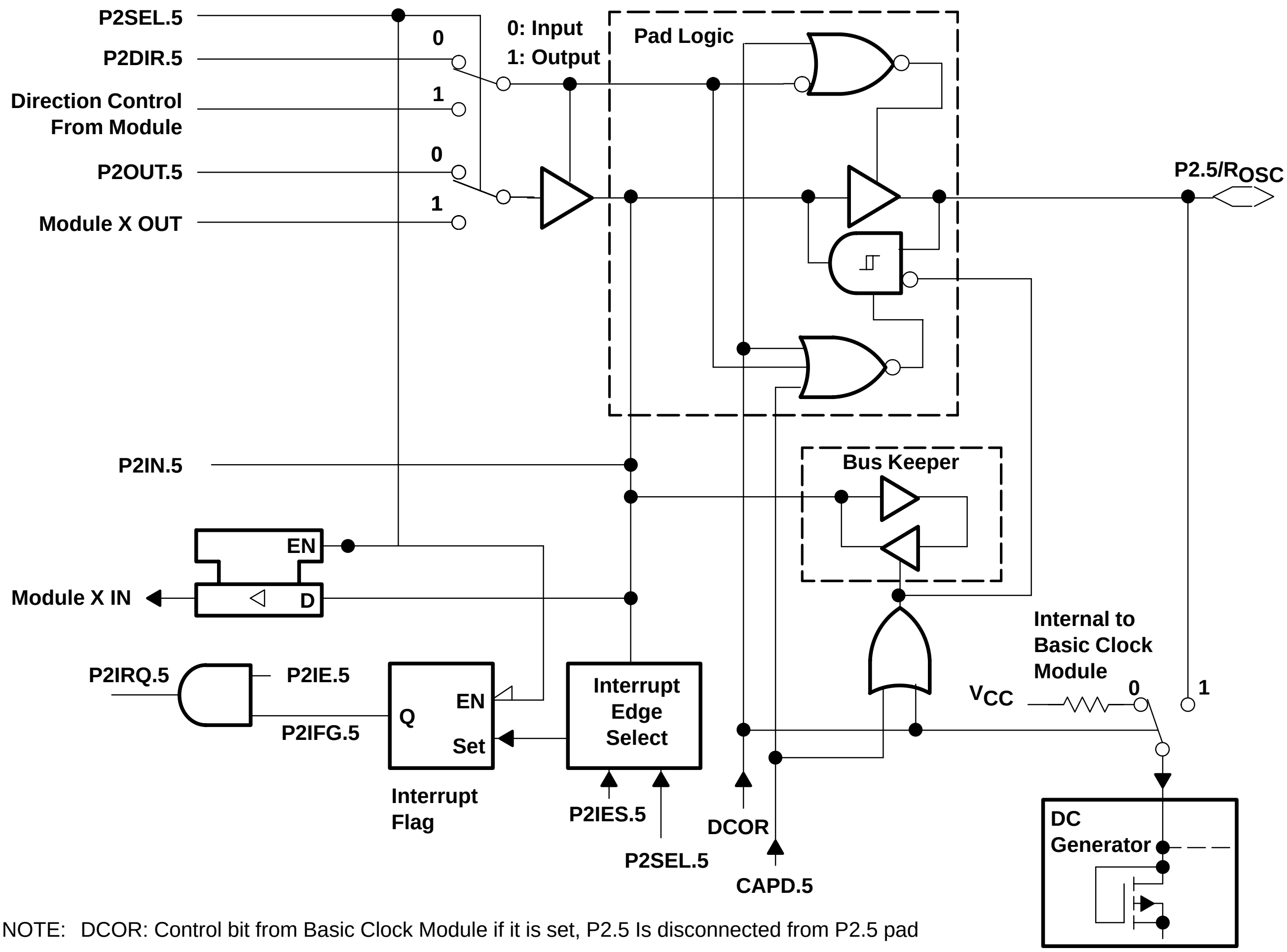


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

† Signal from Timer_A

APPLICATION INFORMATION

Port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the Basic Clock module

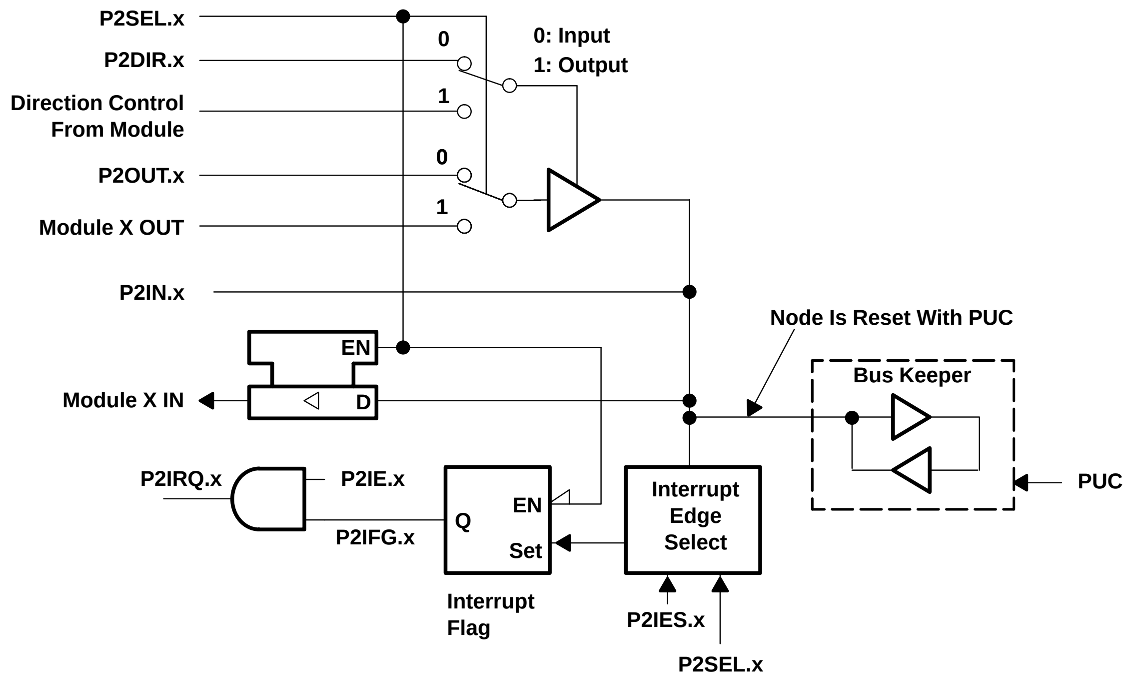


NOTE: DCOR: Control bit from Basic Clock Module if it is set, P2.5 Is disconnected from P2.5 pad

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	V_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

APPLICATION INFORMATION

Port P2, unbonded bits P2.6 and P2.7



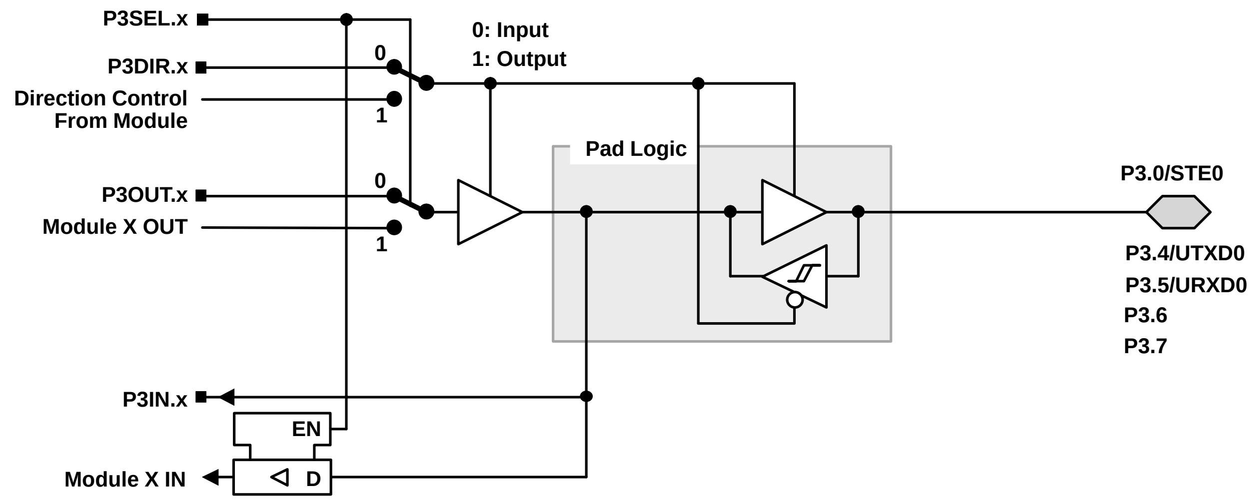
NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

P2Sel.x	P2DIR.x	DIRECTION-CONTROL FROM MODULE	P2OUT.x	MODULE X OUT	P2IN.x	MODULE X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	V_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	V_{SS}	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE: Unbonded bits 6 and 7 of port P2 can be used as interrupt flags. Only software can affect the interrupt flags. They work as software interrupts.

APPLICATION INFORMATION

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger

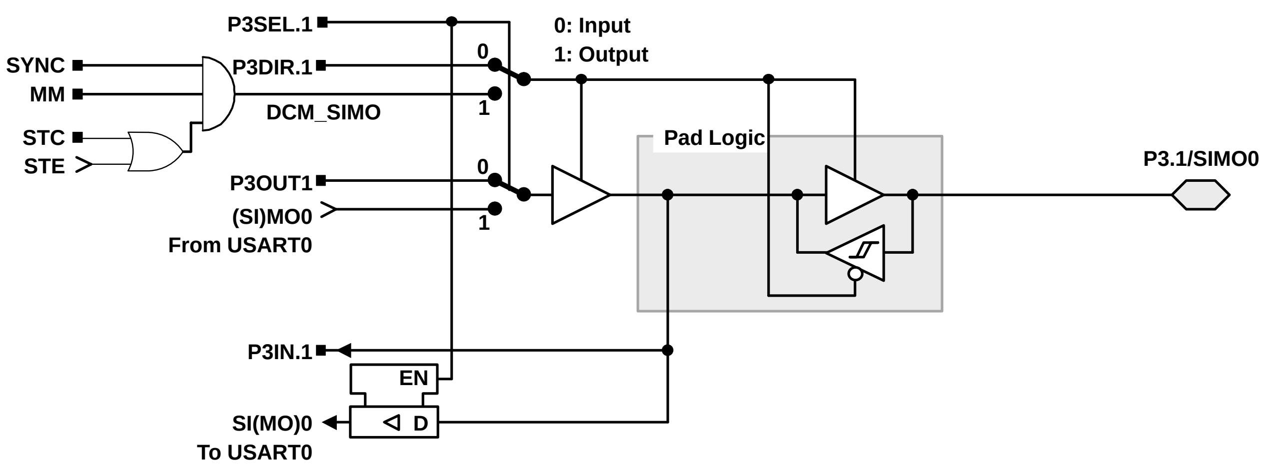


x: Bit Identifier, 0 and 4 to 7 for Port P3

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	V_{SS}	P3OUT.0	V_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	V_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	V_{SS}	P3OUT.5	V_{SS}	P3IN.5	URXD0‡
P3Sel.6	P3DIR.6	V_{SS}	P3OUT.6	V_{SS}	P3IN.6	Unused
P3Sel.7	P3DIR.7	V_{SS}	P3OUT.7	V_{SS}	P3IN.7	Unused

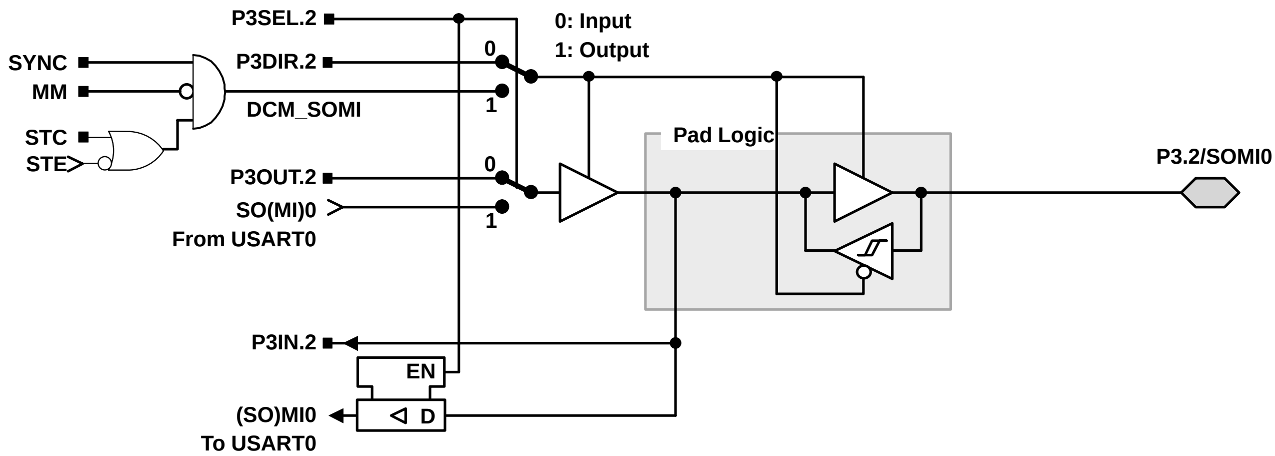
† Output from USART0 module
‡ Input to USART0 module

port P3, P3.1, input/output with Schmitt-trigger

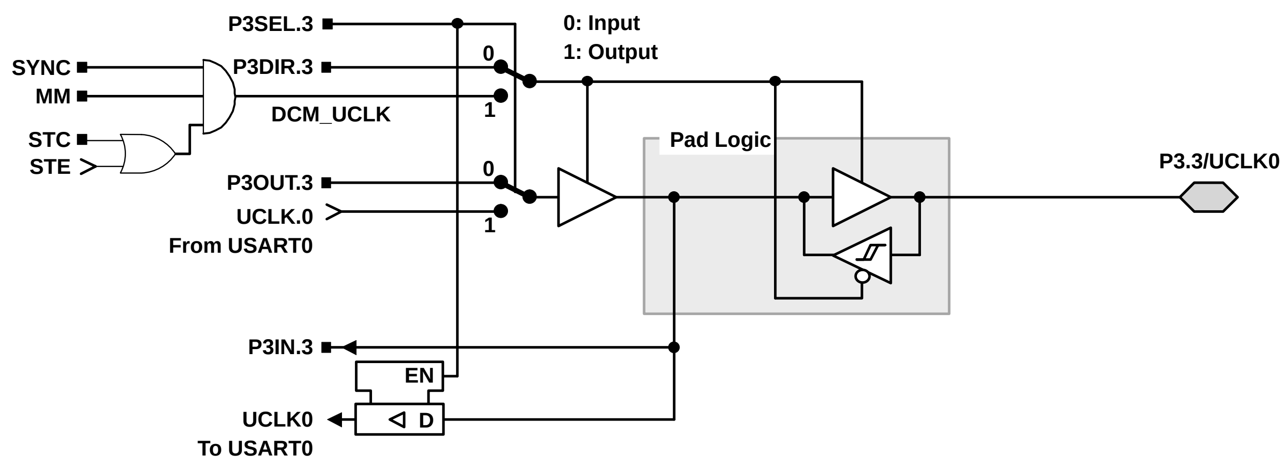


APPLICATION INFORMATION

port P3, P3.2, input/output with Schmitt-trigger



port P3, P3.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 13). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

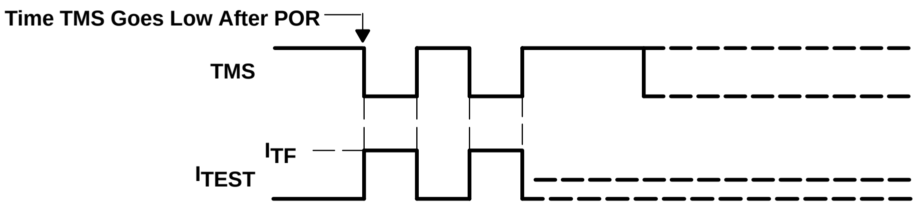


Figure 13. Fuse Check Mode Current, MSP430F12x

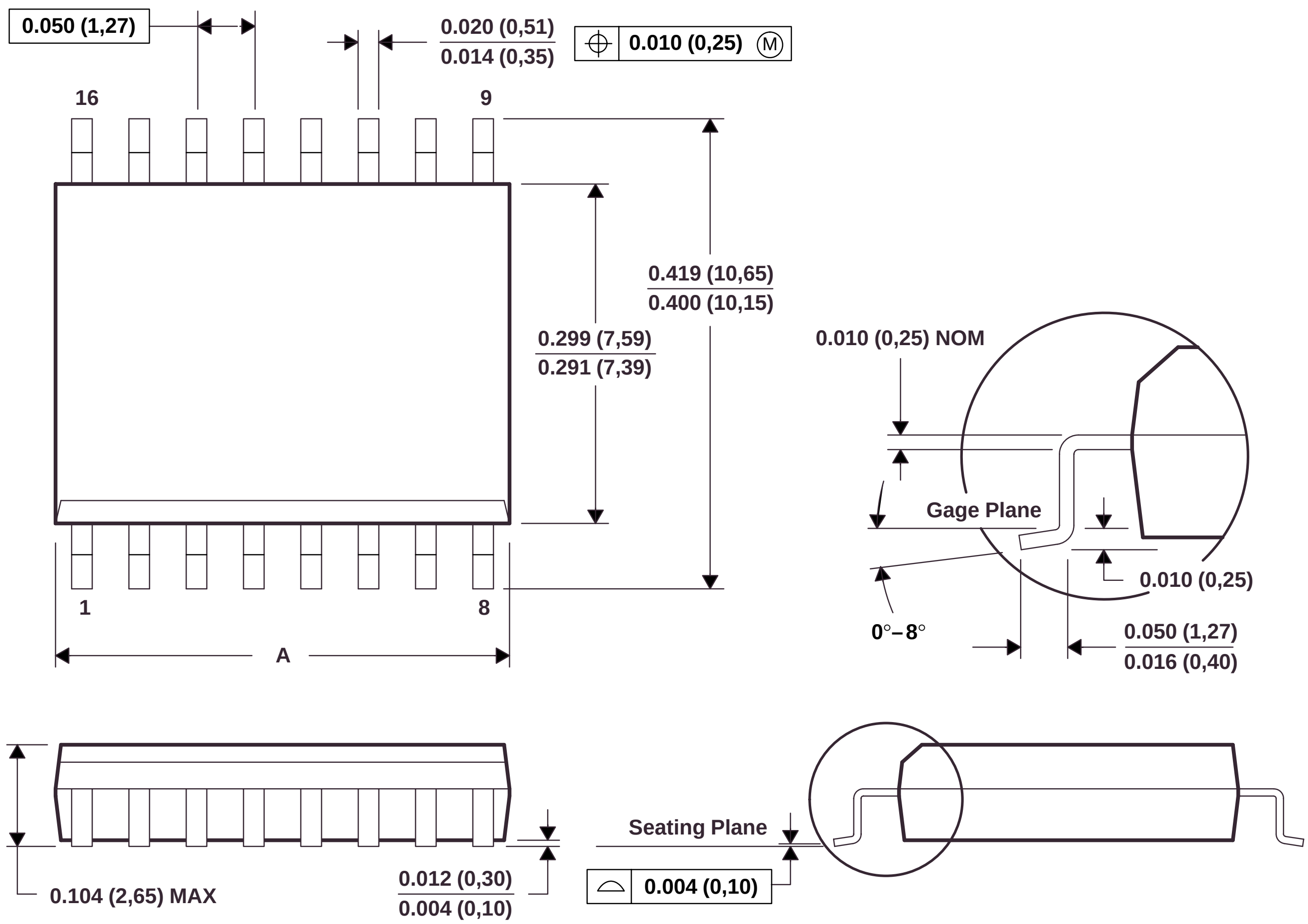
NOTE:

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also see the *bootstrap loader* section for more information.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



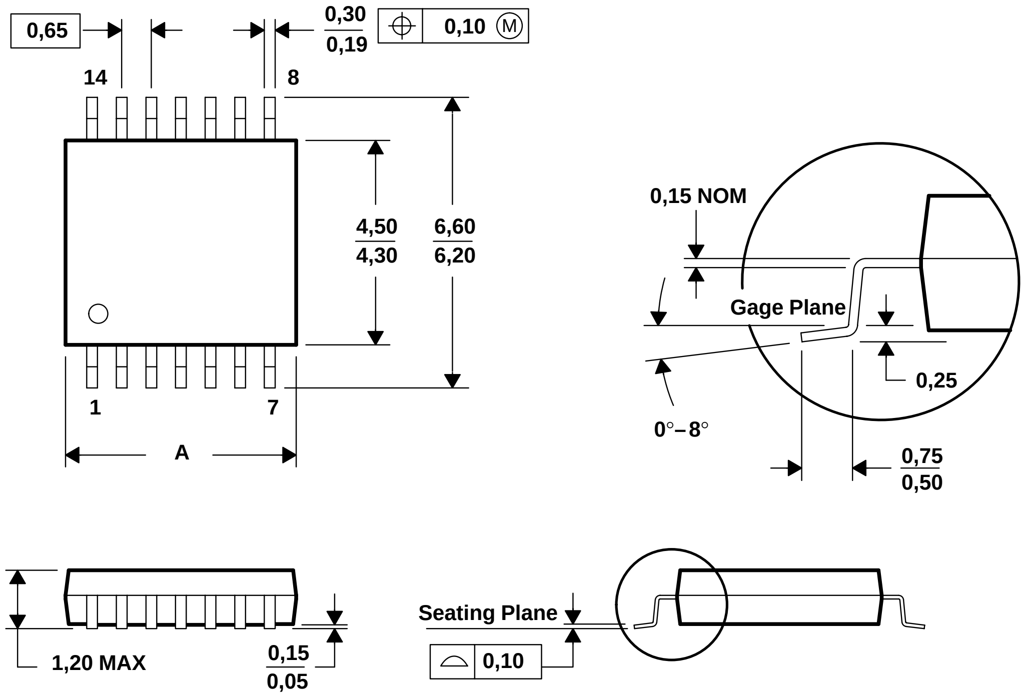
PINS ** / DIM	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/D 01/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153