DATA SHEET

COMPOUND FIELD EFFECT POWER TRANSISTOR
μPA1526

N-CHANNEL POWER MOS FET ARRAY
SWITCHING TYPE

DESCRIPTION

The μPA1526 is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
  $I_{D(pulse)} = \pm 8$ A
  $R_{DS(on)} \leqq 0.30\ \Omega$ TYP. (V_{GS} = 10 V)
  $R_{DS(on)} \leqq 0.35\ \Omega$ TYP. (V_{GS} = 4 V)
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1526H	10-Pin SIP	Standard

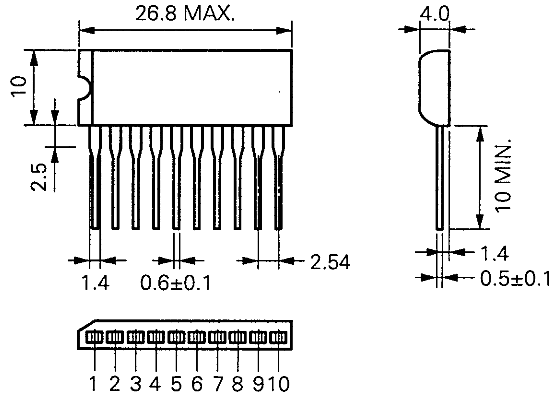
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$*	±8.0	A/unit
Total Power Dissipation (4 circuits) <T_c = 25 °C>	P_{T1}	28	W
Total Power Dissipation (4 circuits) <T_a = 25 °C>	P_{T2}	3.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* PW ≦ 10 ms, Duty Cycle ≦ 10 %

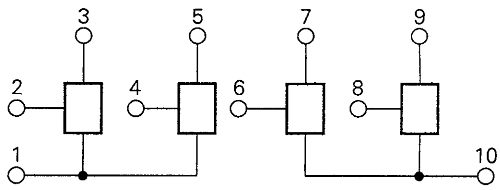
PACKAGE DIMENSIONS
(in millimeters)

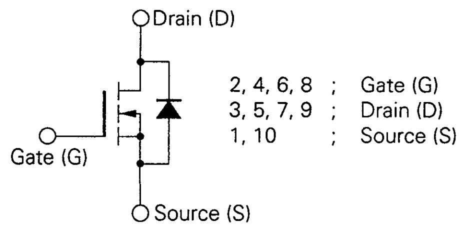


ELECTRODE CONNECTION

2, 4, 6, 8	GATE
3, 5, 7, 9	DRAIN
1, 10	SOURCE

PIN CONNECTION





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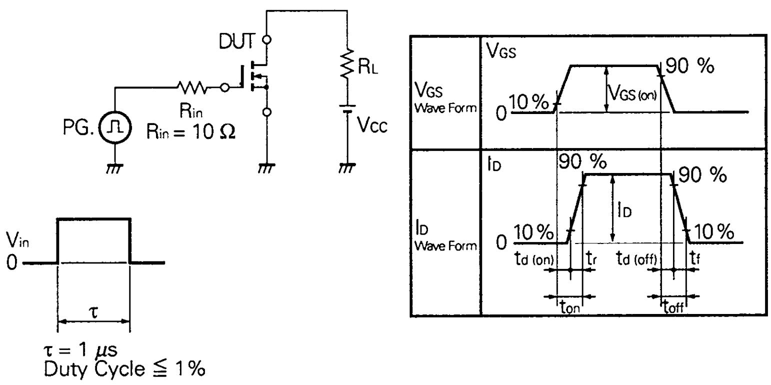
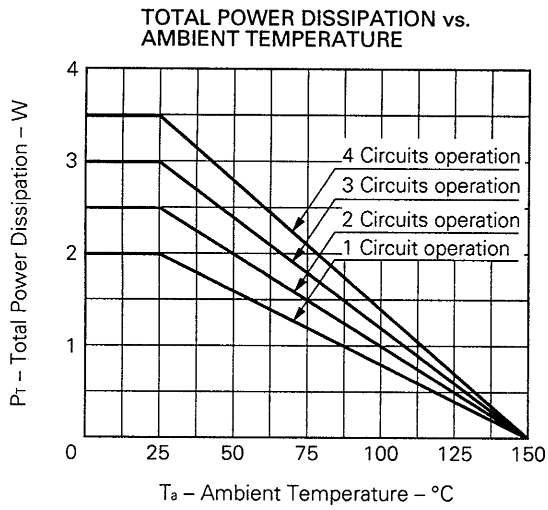
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

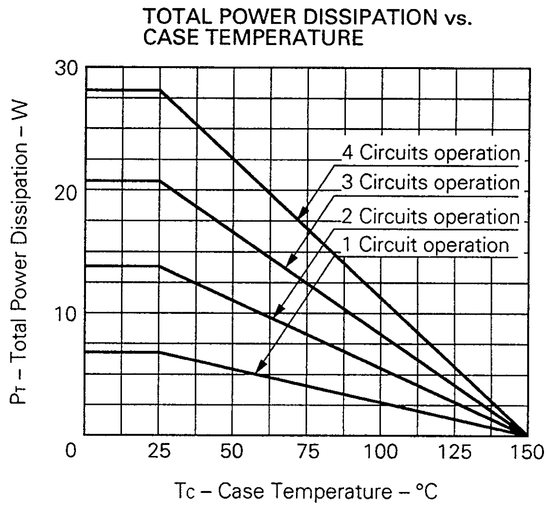
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 100 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	1.0			S	V_{DS} = 10 V, I_D = 1 A
Drain to Source On-state Resistance	$R_{DS(on)1}$		0.3	0.4	Ω	V_{GS} = 10 V, I_D = 1 A
Drain to Source On-state Resistance	$R_{DS(on)2}$		0.35	0.6	Ω	V_{GS} = 4 V, I_D = 0.8 A
Input Capacitance	C_{iss}		500		pF	V_{DS} = 10 V V_{GS} = 0 f = 1.0 MHz
Output Capacitance	C_{oss}		120		pF	
Reverse Transfer Capacitance	C_{rss}		30		pF	
Turn-On Delay Time	$t_{d(on)}$		10		ns	I_D = 1 A V_{GS} = 10 V V_{CC} = 50 V R_L = 50 Ω, R_{in} = 10 Ω See Fig. 1
Rise Time	t_r		20		ns	
Turn-Off Delay Time	$t_{d(off)}$		80		ns	
Fall Time	t_f		20		ns	

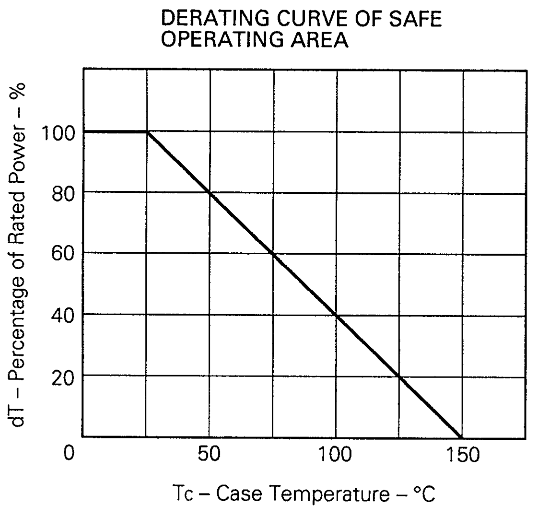
Fig. 1 Switching Test Circuit

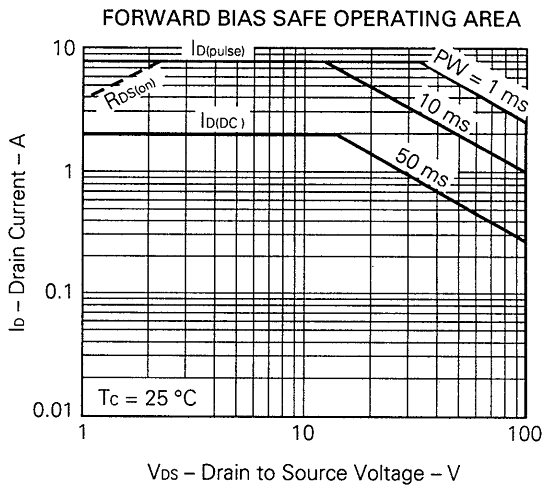


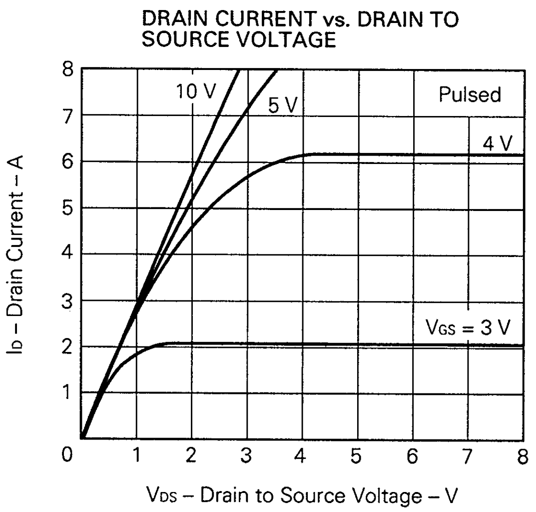
TYPICAL CHARACTERISTICS (T_a = 25 °C)

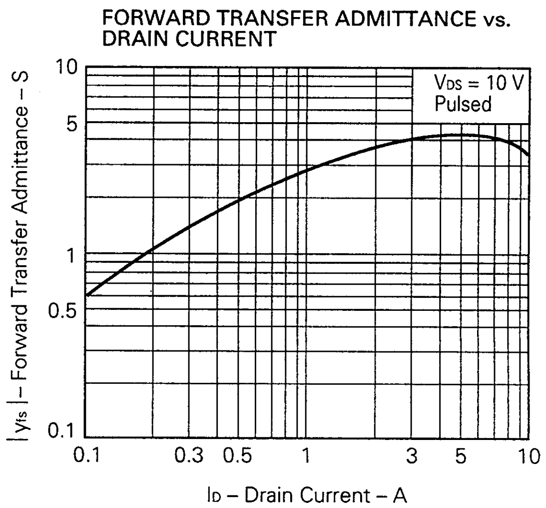




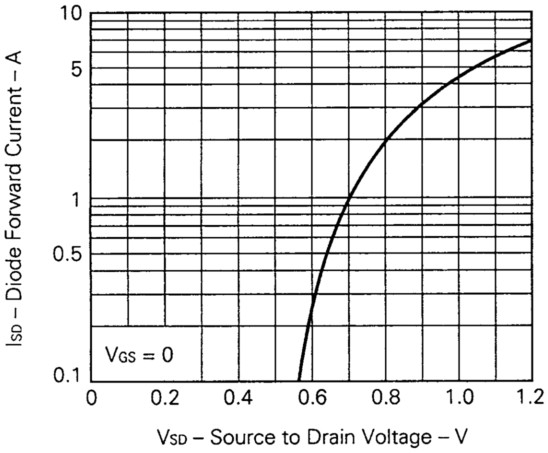




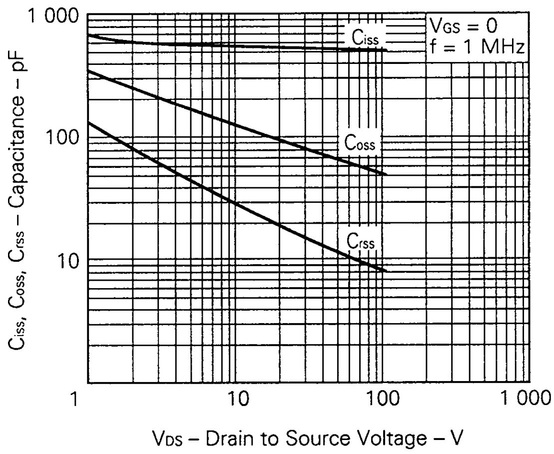




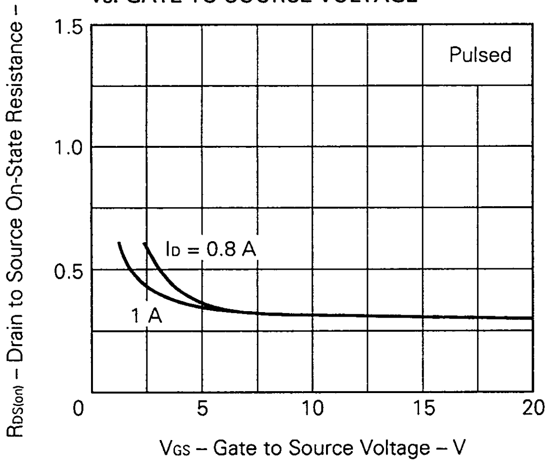
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



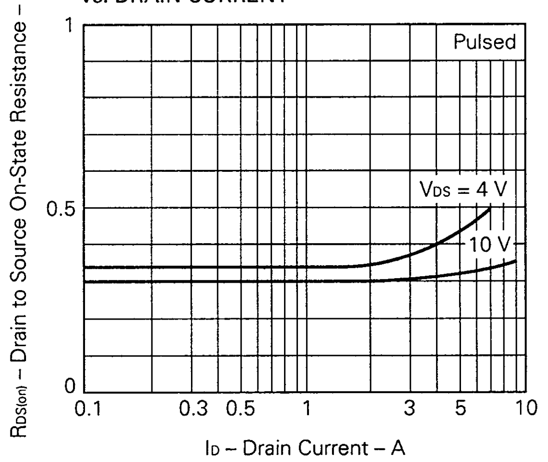
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



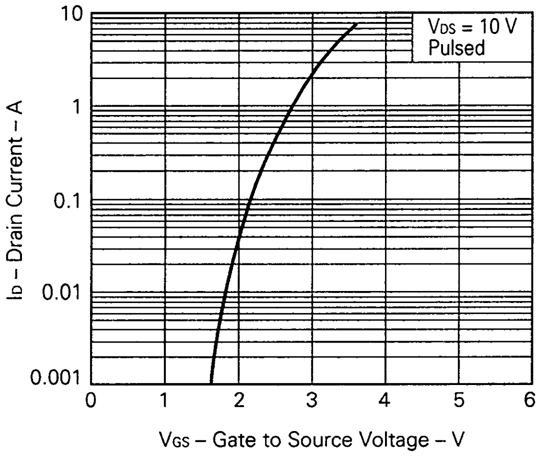
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



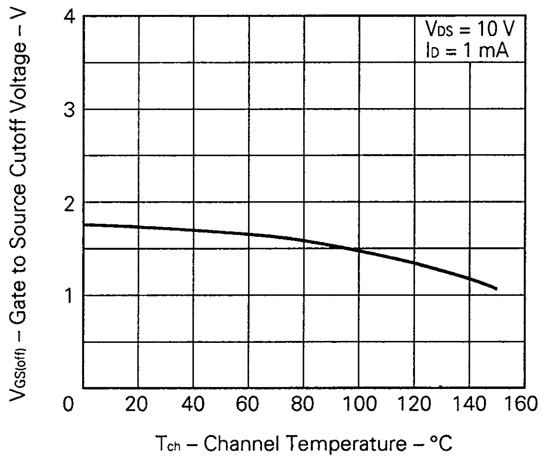
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

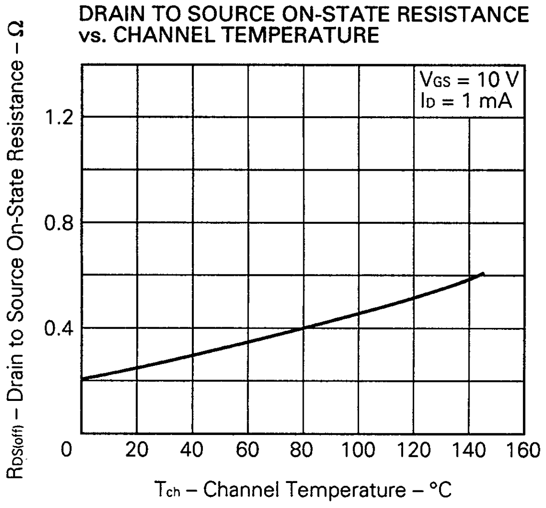


TRANSFER CHARACTERISTICS



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE




DRAIN TO SOURCE ON-STATE RESISTANCE
vs. CHANNEL TEMPERATURE
VGS = 10 V
ID = 1 mA
RDS(off) – Drain to Source On-State Resistance – Ω
1.2
0.8
0.4
0
20
40
60
80
100
120
140
160
Tch – Channel Temperature – °C

Reference

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Application circuit using Power MOS FET	TEB-1035

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