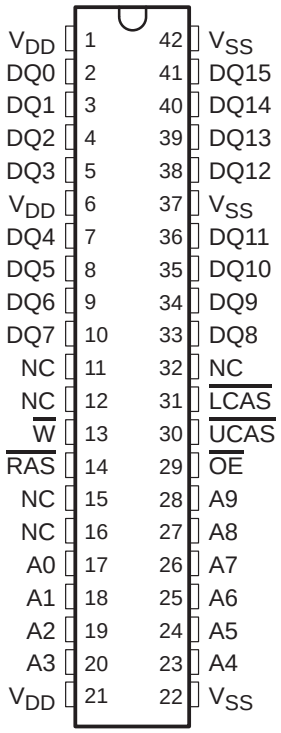
This data sheet is applicable to TMS418160As symbolized by Revision "E" and subsequent revisions as described in the device symbolization section.

- **Organization . . . 1048576 by 16 Bits**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **1024-Cycle Refresh in 16 ms**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ/ WRITE CYCLE MIN
'418160A-50	50 ns	13 ns	25 ns	90 ns
'418160A-60	60 ns	15 ns	30 ns	110 ns
'418160A-70	70 ns	18 ns	35 ns	130 ns

- **Enhanced Page-Mode Operation With $\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ (xCBR) Refresh**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DZ Suffix)**
- **Ambient Temperature Range 0°C to 70°C**

DZ PACKAGE
(TOP VIEW)



description

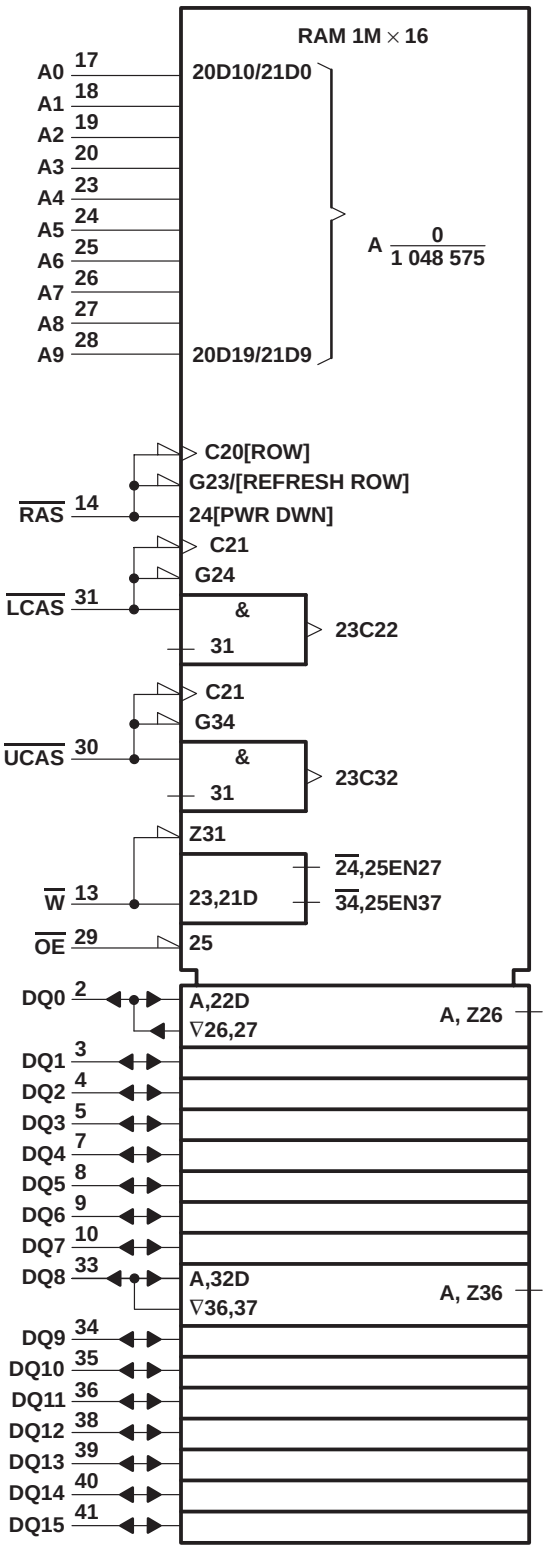
The TMS418160A is a 16777216-bit dynamic random-access memory (DRAM) device organized as 1048576 words of 16 bits. It employs state-of-the-art technology for high performance, reliability, and low power at low cost.

This device features maximum $\overline{\text{RAS}}$ access times of 50-, 60-, and 70 ns. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS418160A is offered in a 42-lead plastic surface-mount SOJ package (DZ suffix). This package is designed for operation from 0° to 70°C.

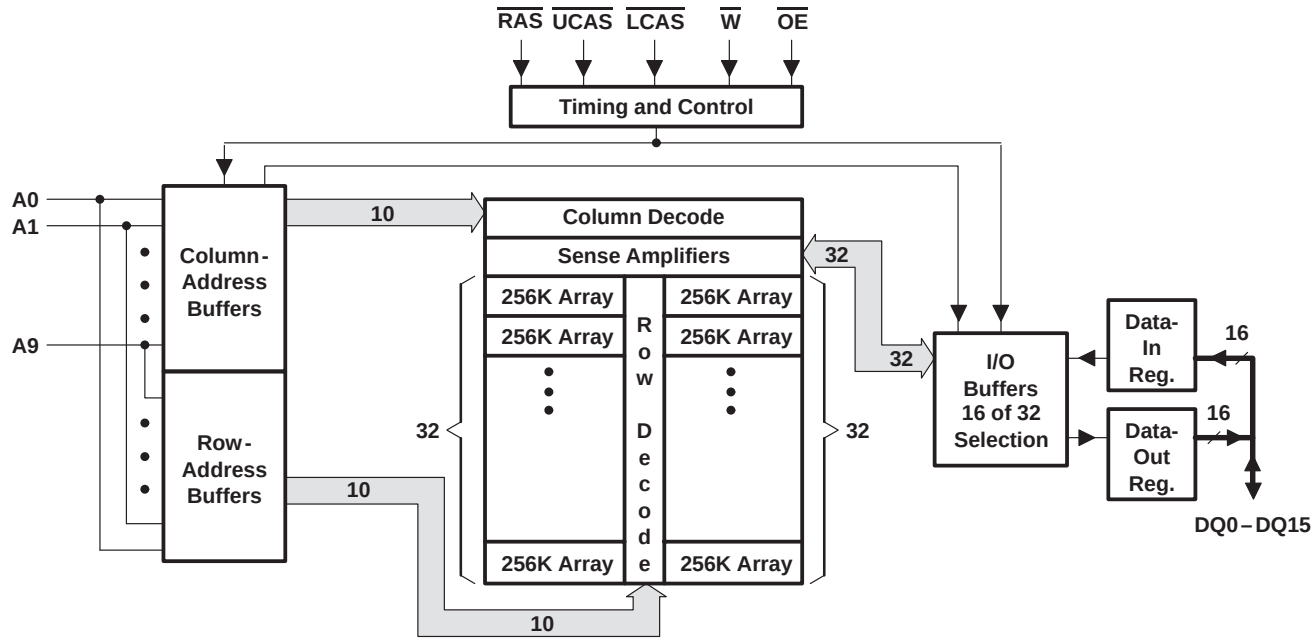
PIN NOMENCLATURE	
A[0:9]	Address Inputs
DQ[0:15]	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
$\overline{\text{NC}}$	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



operation

dual $\overline{\text{xCAS}}$

Two $\overline{\text{xCAS}}$ pins ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$) are provided to give independent control of the 16 data I/O pins (DQ0–DQ15), with $\overline{\text{LCAS}}$ corresponding to DQ0–DQ7 and $\overline{\text{UCAS}}$ corresponding to DQ8–DQ15. Each $\overline{\text{xCAS}}$ going low enables its corresponding DQx pin.

In write cycles, data-in setup and hold time (t_{DS} and t_{DH}) and write-command setup and hold time (t_{WCS}, t_{CWL} and t_{WCH}) must be satisfied for each individual $\overline{\text{xCAS}}$ to ensure writing into the storage cells of the corresponding DQ pins.

Different modes of operation for upper and lower bytes in one cycle are not allowed, such as the example shown in Figure 1.

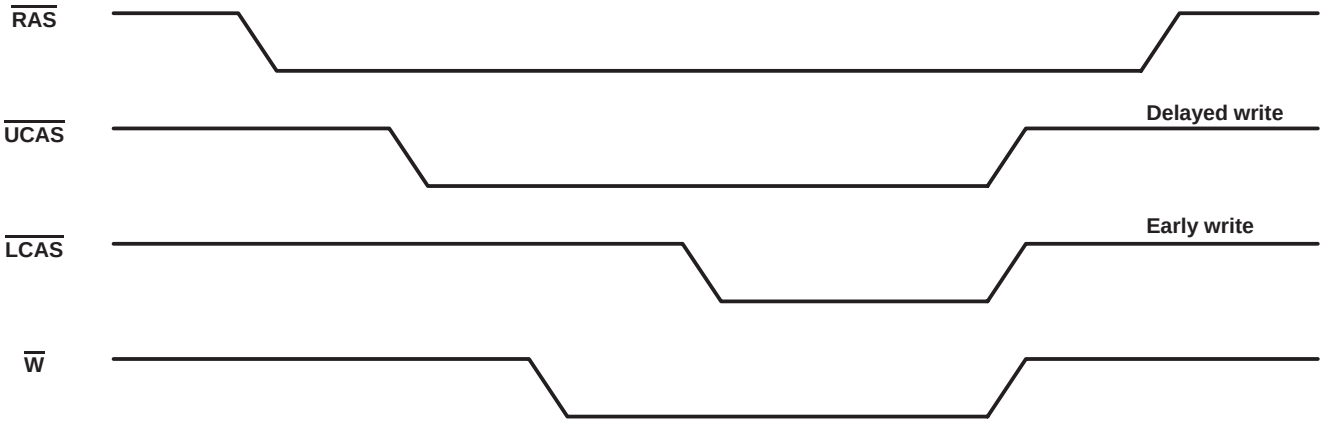


Figure 1. Illegal Dual-$\overline{\text{xCAS}}$ Operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplexing is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This performance improvement is referred to as enhanced-page mode. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ transitions low. A valid column address may be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{xCAS}$ low) if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA}.

address: A0 – A9

Twenty address bits are required to decode each of the 1048576 storage cell locations. Twelve row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

The column address is latched on the first $\overline{xCAS}$ falling edge with address setup and hold parameters referenced to that edge. In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum hold time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

write enable ($\overline{W}$)

Read- or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. Data in is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operations to be completed with $\overline{OE}$ grounded.

data in (DQ0 – DQ15)

Data is written during a write- or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to a $\overline{xCAS}$ falling edge and the data is strobed into the on-chip data latch for the corresponding DQs with setup-and-hold times referenced to this $\overline{xCAS}$ signal.

In a delayed-write- or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. Also, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines (see parameter t_{OED}).

data out (DQ0–DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{xCAS}}$ and $\overline{\text{OE}}$ are brought low. In a read cycle, the output becomes valid after the access-time-interval t_{CAC} (which begins with the negative transition of $\overline{\text{xCAS}}$) as long as t_{RAC} (access time from $\overline{\text{RAS}}$) and t_{AA} (access time from column address) are satisfied. The delay time from $\overline{\text{xCAS}}$ low to valid data out is measured from each individual $\overline{\text{xCAS}}$ to its corresponding DQx pin.

output enable ($\overline{\text{OE}}$)

$\overline{\text{OE}}$ controls the impedance of the output buffers. When $\overline{\text{OE}}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{\text{OE}}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ to be brought low (until either $\overline{\text{OE}}$ or $\overline{\text{xCAS}}$ is brought high) for the output buffers to go into the low-impedance state.

$\overline{\text{RAS}}$-only refresh

A refresh operation must be performed once every 16 ms to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding both $\overline{\text{xCAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{xCAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ (xCBR) refresh

xCBR refresh is utilized by bringing at least one $\overline{\text{xCAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{\text{xCAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 μs, followed by a minimum of eight initialization cycles, is required after power up to the full V_{DD} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or xCBR) cycle.

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Ambient temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'418160A-50		'418160A-60		'418160A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{DD} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{DD}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 5.5 V, V_O = 0 V to V_{DD}, $\overline{xCAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 5.5 V, Minimum cycle		180		160		150	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2		2	mA
		V_{IH} = V_{DD} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or xCBR)	V_{DD} = 5.5 V, $\overline{RAS}$ cycling, Minimum cycle, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (xCBR)		180		160		150	mA
I_{CC4}‡¶	Average page current	V_{DD} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		110		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page cycle, t_{PC}

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A9		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance#		7	pF

$\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable outputs
NOTE 3: V_{DD} = 5 V ± 10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 4)

PARAMETER		’418160A-50		’418160A-60		’418160A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		25		30		35	ns
t_{CAC}	Access time from $\overline{xCAS}$		13		15		18	ns
t_{CPA}	Access time from $\overline{xCAS}$ precharge		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$		13		15		18	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output data hold time from $\overline{xCAS}$	3		3		3		ns
t_{OHO}	Output data hold time from $\overline{OE}$	3		3		3		ns
t_{OFF}	Output buffer turn-off delay from $\overline{xCAS}$ (see Note 5)	0	13	0	15	0	18	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 5)	0	13	0	15	0	18	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven. Data-in should not be enabled until one of the applicable maximum specifications is satsified.

ac timing requirements (see Note 4)

		’418160A-50		’418160A-60		’418160A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	90		110		130		ns
t_{WC}	Cycle time, write	90		110		130		ns
t_{RWC}	Cycle time, read-write	131		155		181		ns
t_{PC}	Cycle time, page-mode read or write (see Note 6)	35		40		45		ns
t_{PRWC}	Cycle time, page-mode read-write	76		85		96		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 7)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 7)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ active (see Note 8)	13	10 000	15	10 000	18	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ (precharge)	30		40		50		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data-in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{xCAS}$ precharge	13		15		18		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	13		15		18		ns
t_{WCS}	Setup time, write command before $\overline{xCAS}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns

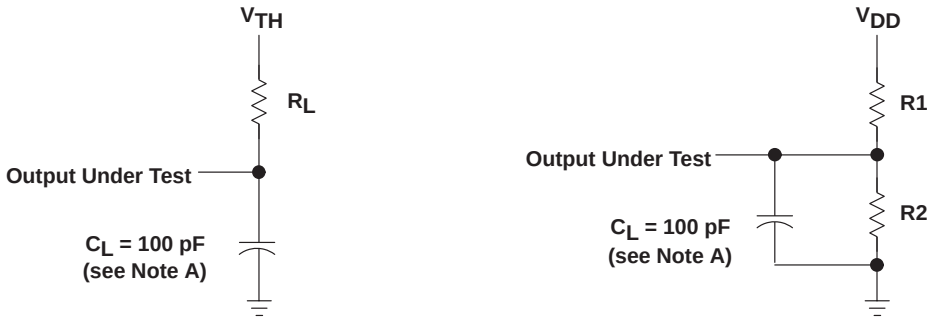
NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
6. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
9. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations

ac timing requirements (see Note 4) (continued)

		’418160A-50		’418160A-60		’418160A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address	10		10		15		ns
t_{DH}	Hold time, data-in (see Note 9)	10		10		15		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{\text{xCAS}}$ (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{\text{RAS}}$ (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{\text{xCAS}}$ active (early-write only)	10		10		15		ns
t_{CLCH}	Hold time, $\overline{\text{xCAS}}$ low to $\overline{\text{xCAS}}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{\text{RAS}}$ active from $\overline{\text{xCAS}}$ precharge	30		35		40		ns
t_{OEH}	Hold time, $\overline{\text{OE}}$ command	13		15		18		ns
t_{ROH}	Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$	10		10		10		ns
t_{WRH}	Hold time, write after $\overline{\text{RAS}}$ active (CBR refresh only)	10		10		10		ns
t_{CP}	Delay time, $\overline{\text{xCAS}}$ precharge	8		10		10		ns
t_{AWD}	Delay time, column address to write command (read-write operation only)	48		55		63		ns
t_{CHR}	Delay time, $\overline{\text{xCAS}}$ referenced to $\overline{\text{RAS}}$ (xCBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{\text{xCAS}}$ precharge to $\overline{\text{RAS}}$	5		5		5		ns
t_{CSH}	Delay time, $\overline{\text{RAS}}$ active to $\overline{\text{xCAS}}$ precharge	50		60		70		ns
t_{CSR}	Setup time, $\overline{\text{xCAS}}$ referenced to $\overline{\text{RAS}}$ (xCBR refresh only)	5		5		5		ns
t_{CWD}	Delay time, $\overline{\text{xCAS}}$ to write command (read-write operation only)	36		40		46		ns
t_{OED}	Delay time, $\overline{\text{OE}}$ to data in	13		15		18		ns
t_{RAD}	Delay time, $\overline{\text{RAS}}$ to column address (see Note 11)	13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{\text{RAS}}$ precharge	25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{\text{xCAS}}$ precharge	25		30		35		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ to $\overline{\text{xCAS}}$ (see Note 11)	18	37	20	45	20	52	ns
t_{RPC}	Delay time, $\overline{\text{RAS}}$ precharge to $\overline{\text{xCAS}}$ active	5		5		5		ns
t_{RSH}	Delay time, $\overline{\text{xCAS}}$ active to $\overline{\text{RAS}}$ precharge	13		15		18		ns
t_{RWD}	Delay time, $\overline{\text{RAS}}$ to write command (read-write operation only)	73		85		98		ns
t_{CPW}	Delay time, $\overline{\text{xCAS}}$ precharge to write command (read-write operation only)	53		60		68		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
9. Referenced to the later of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ in write operations
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



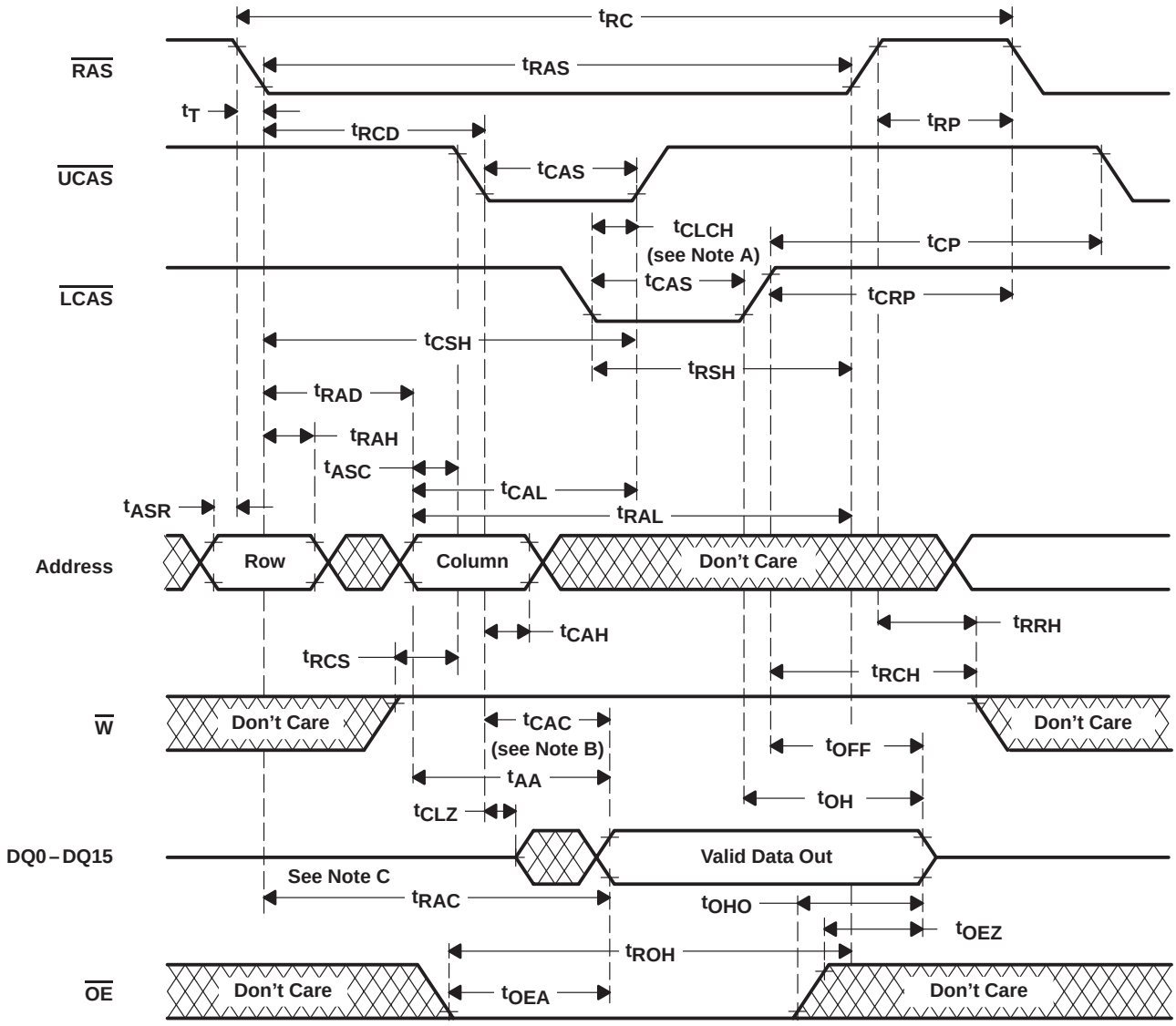
(a) LOAD CIRCUIT **(b) ALTERNATE LOAD CIRCUIT**

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{DD} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
’418160A	5	828	295	1.31	218

Figure 2. Load Circuits for Timing Parameters

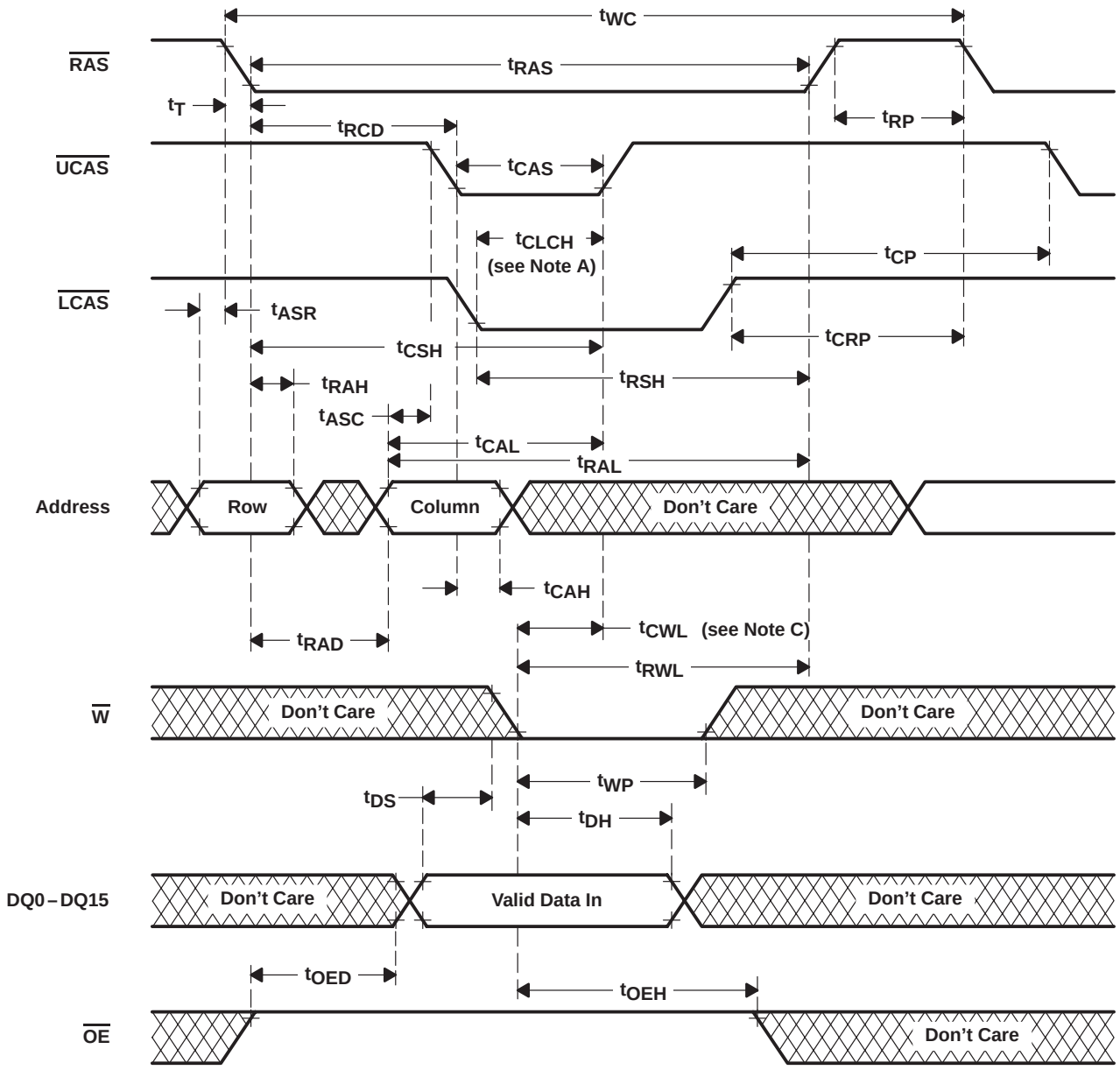
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Read-Cycle Timing

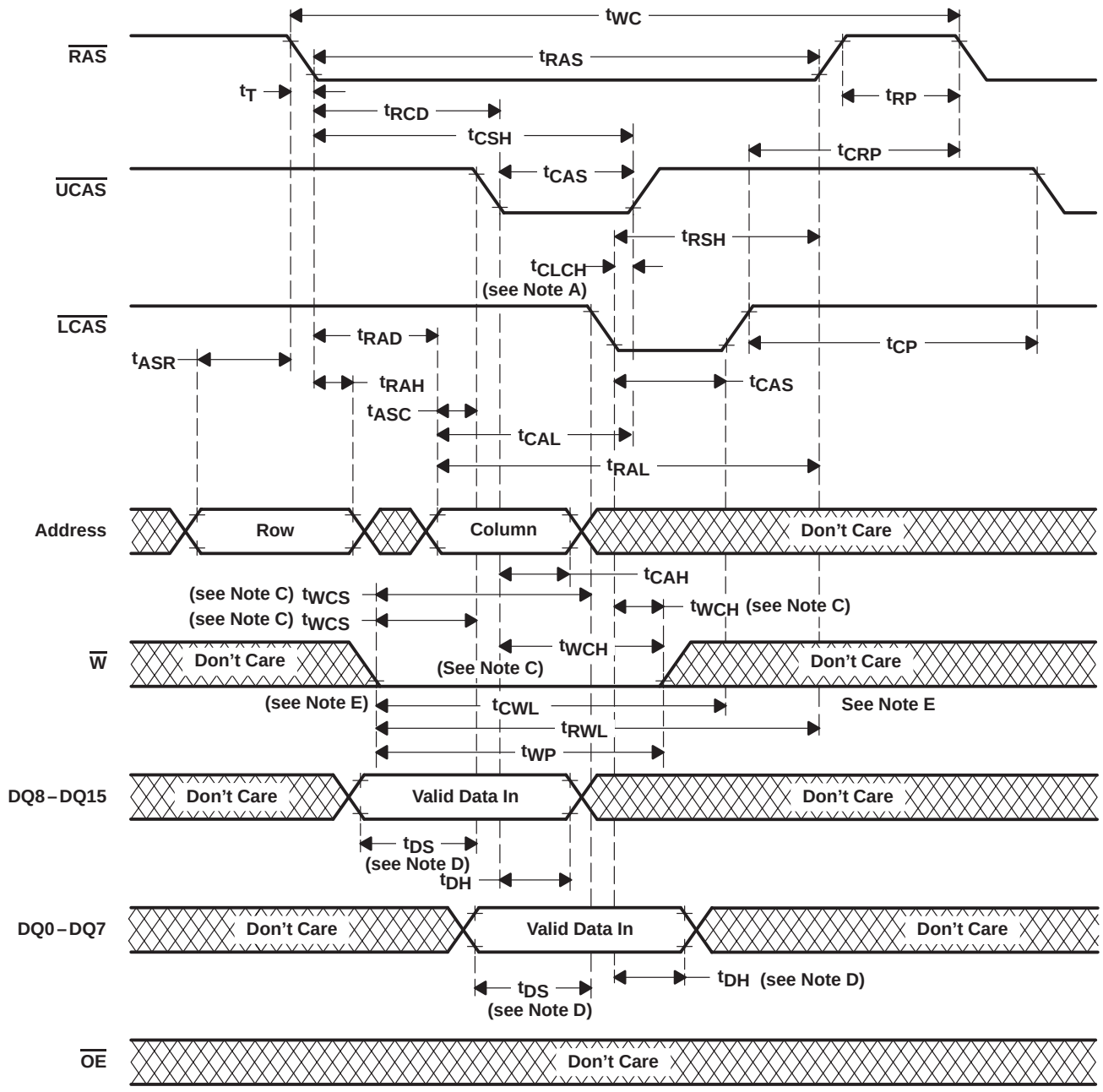
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.
C. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to write properly to each byte.

Figure 4. Write-Cycle Timing

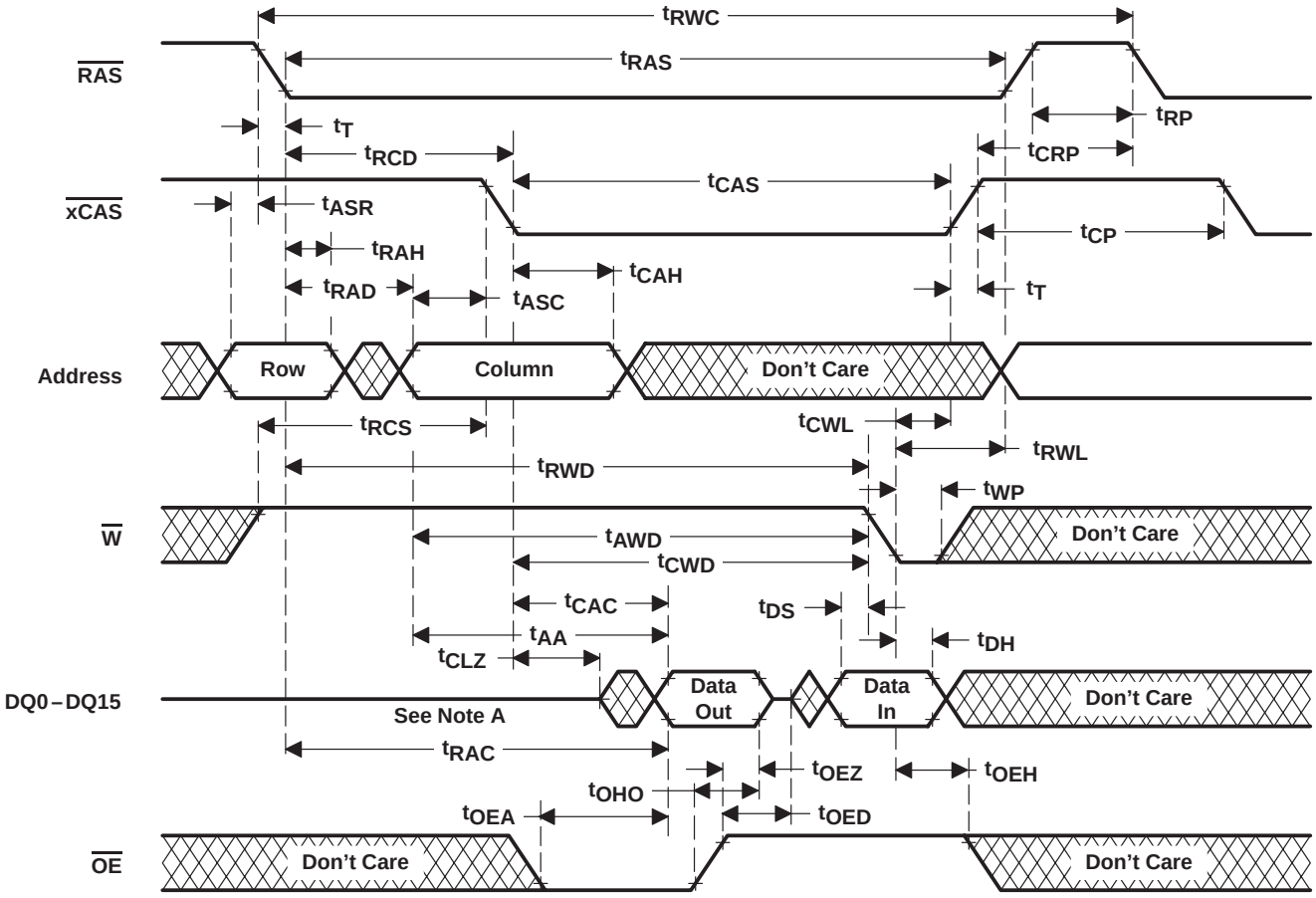
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.
C. t_{WCS} and t_{WCH} must be satisfied for each $\overline{\text{xCAS}}$.
D. t_{DS} and t_{DH} of a DQ input are referenced to the corresponding $\overline{\text{xCAS}}$.
E. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to write properly to each byte.

Figure 5. Early-Write-Cycle Timing

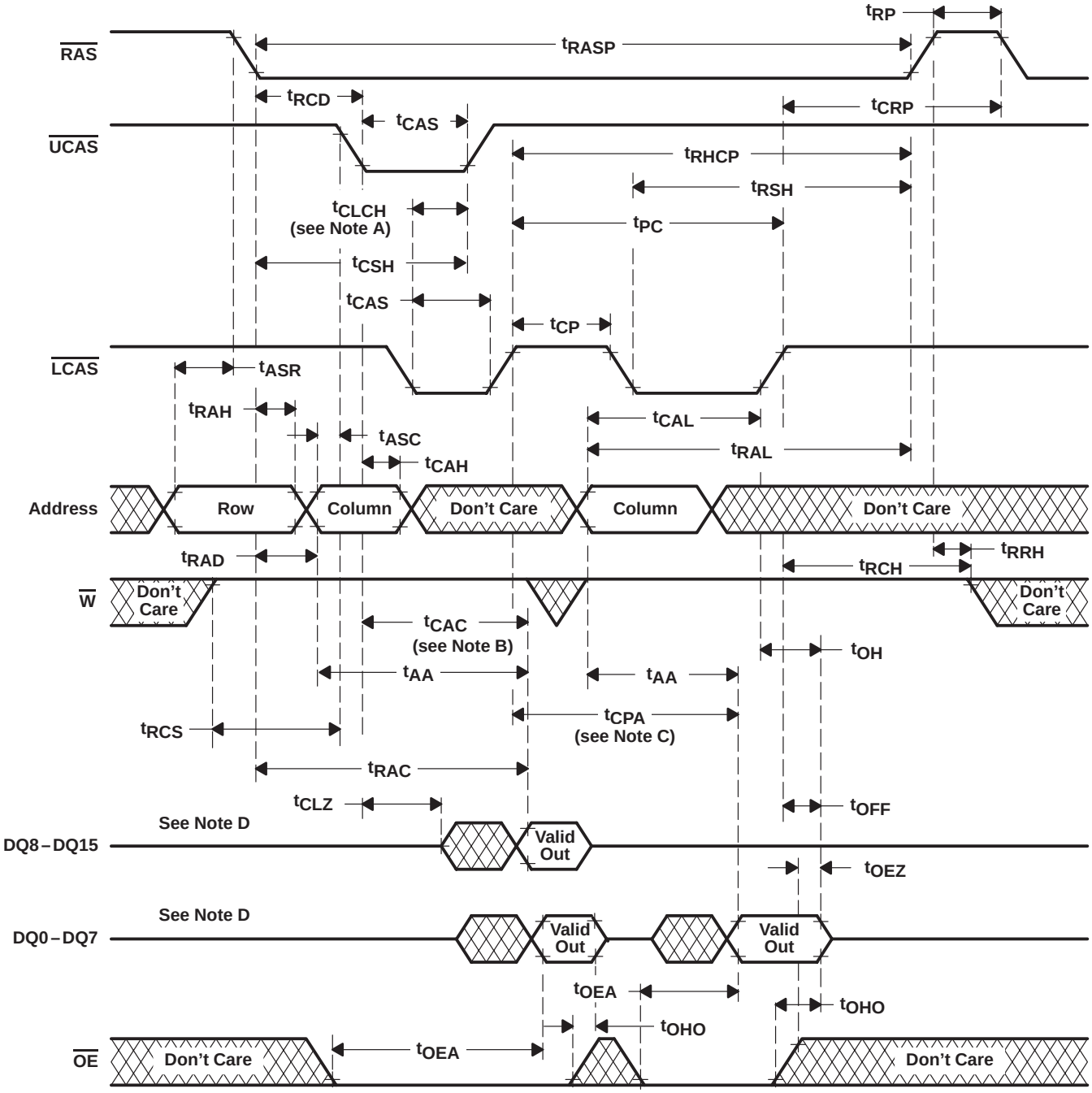
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

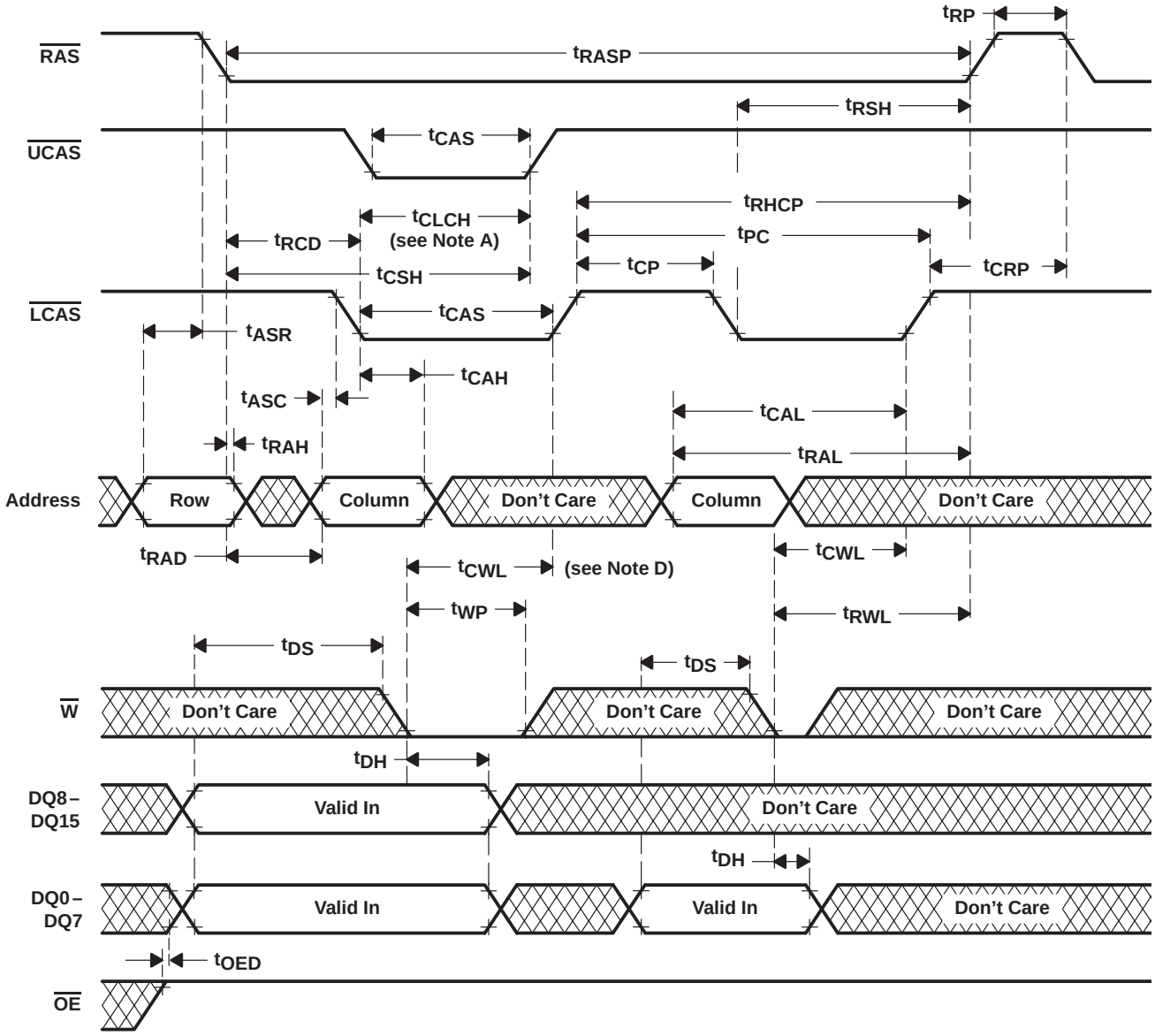
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write timing specifications are not violated.
F. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

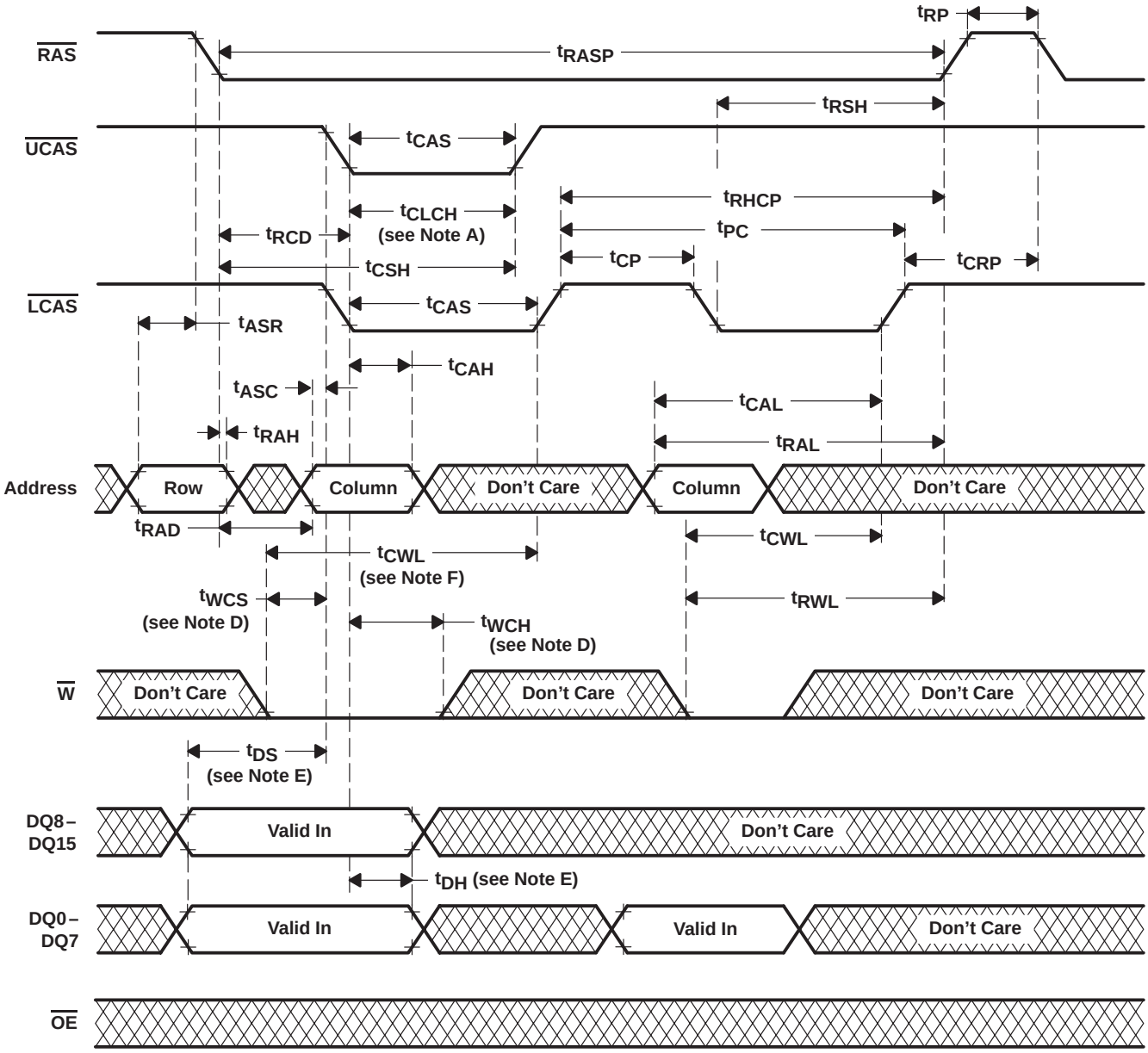
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to ensure proper writing to each byte.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

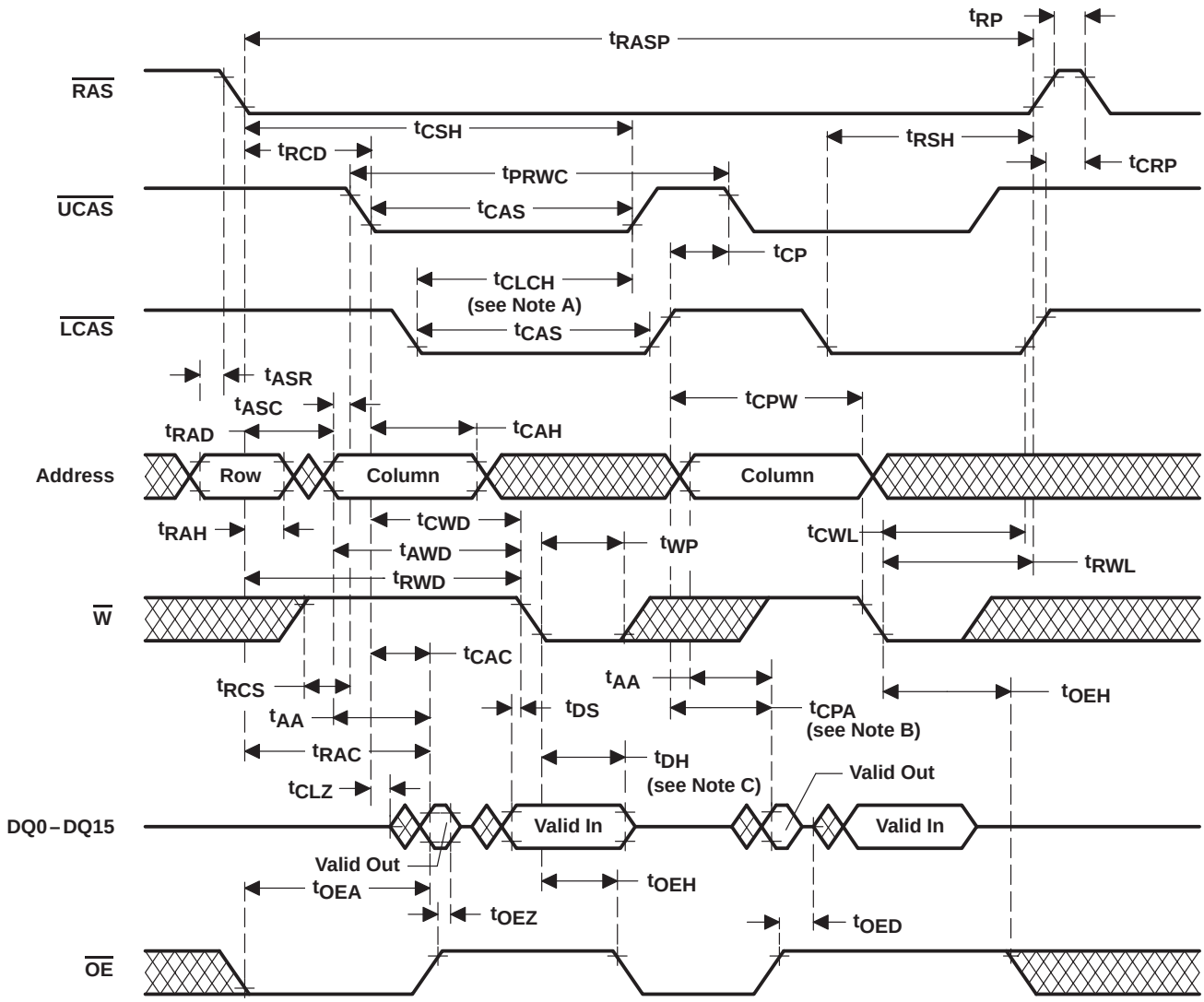
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. t_{WCS} and t_{WCH} must be satisfied for each $\overline{\text{xCAS}}$.
E. t_{DS} and t_{DH} for a DQ is referenced to the corresponding $\overline{\text{xCAS}}$.
F. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$.

Figure 9. Enhanced-Page-Mode Early Write-Cycle Timing

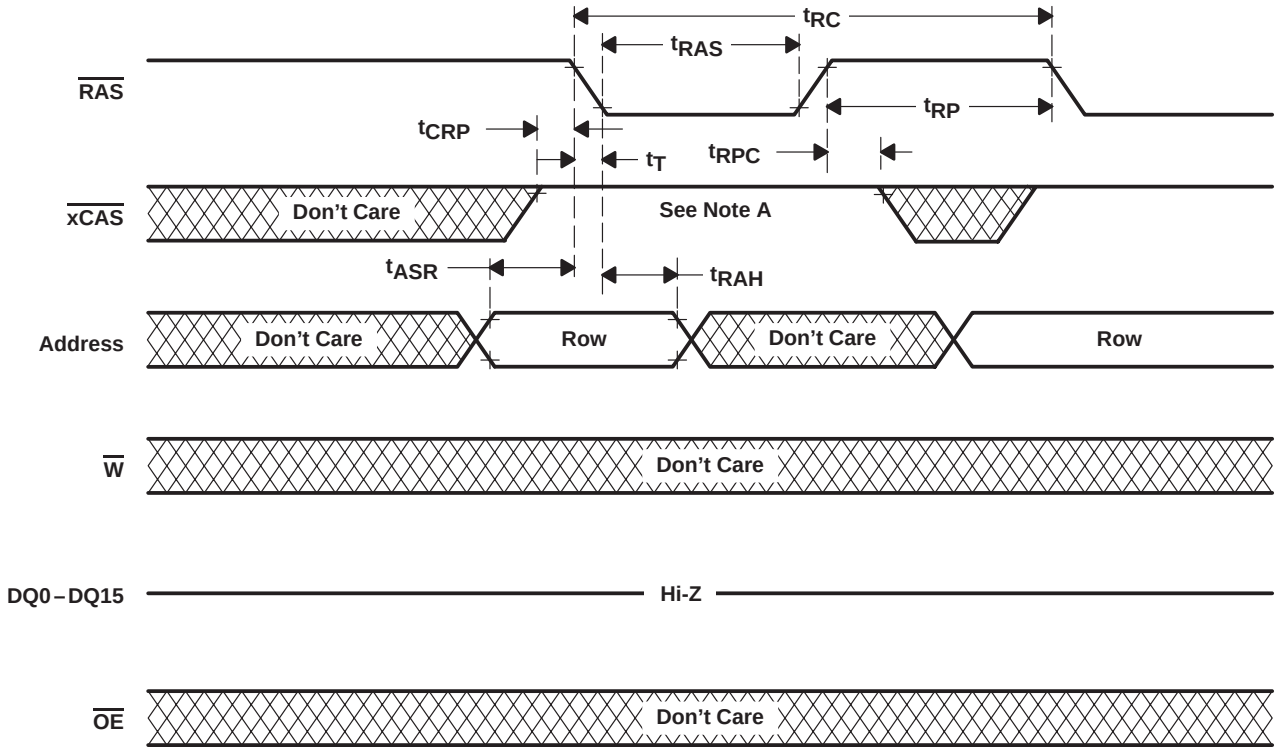
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. xCAS order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 10. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{\text{xCAS}}$ must be high.

Figure 11. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

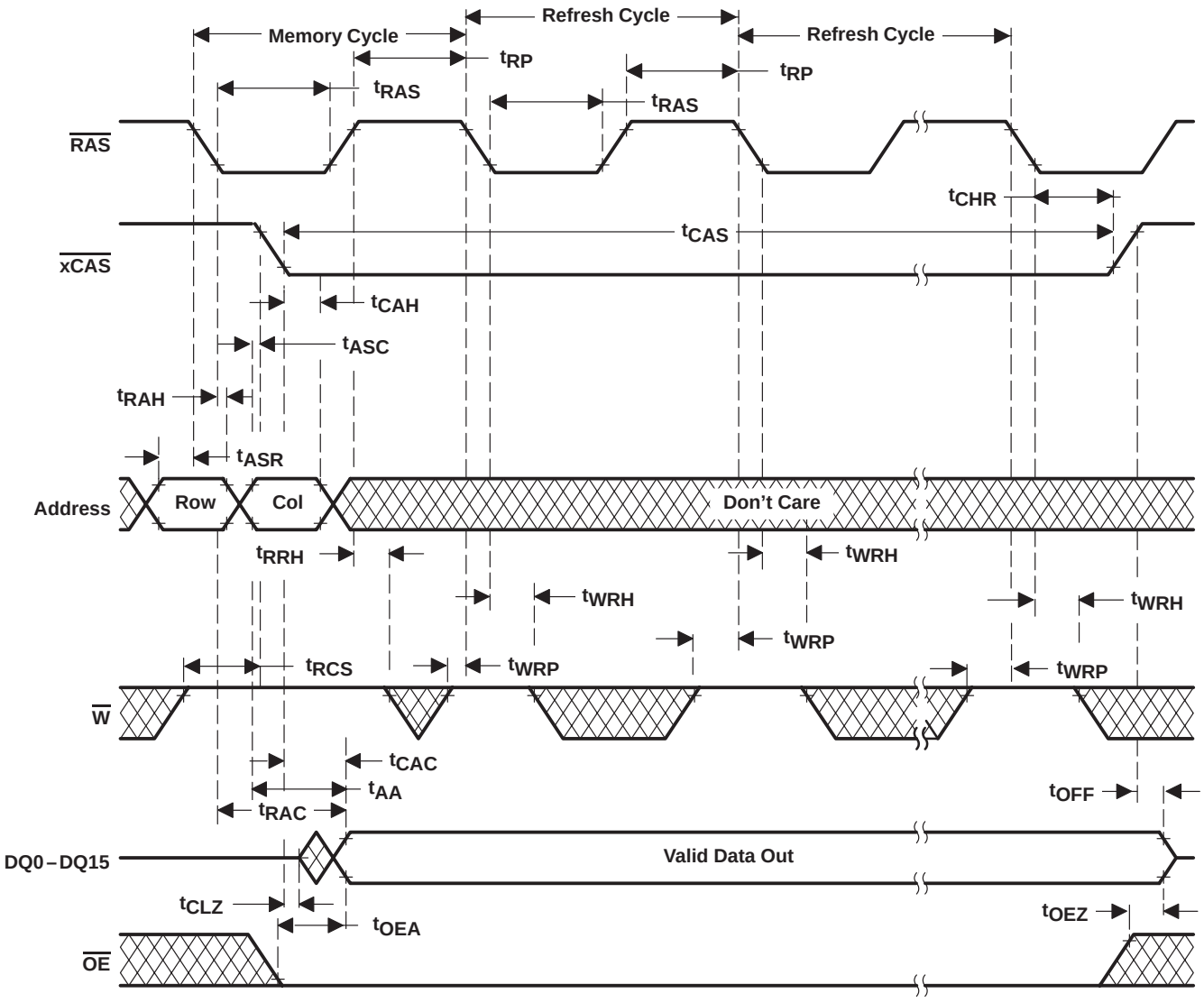


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

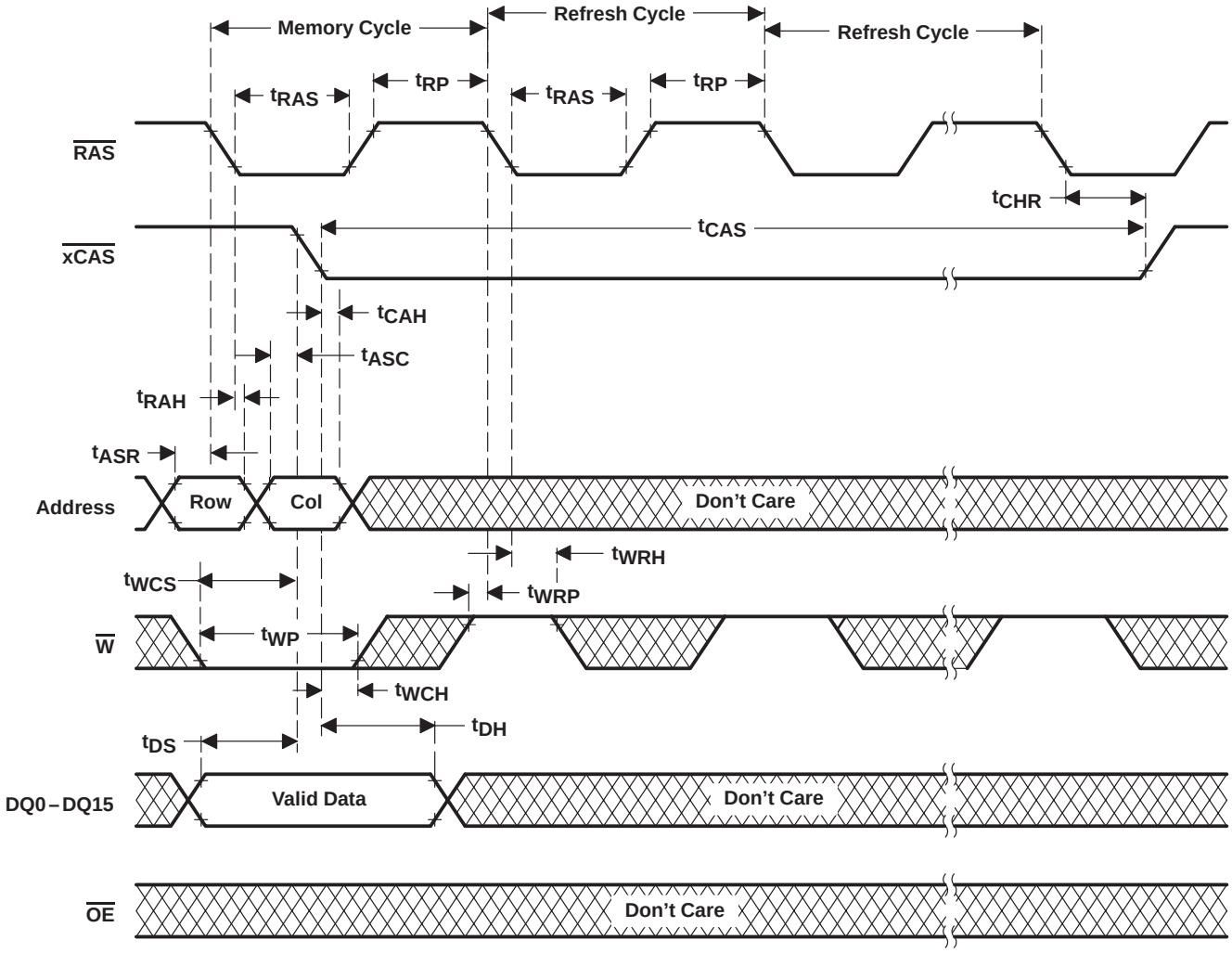
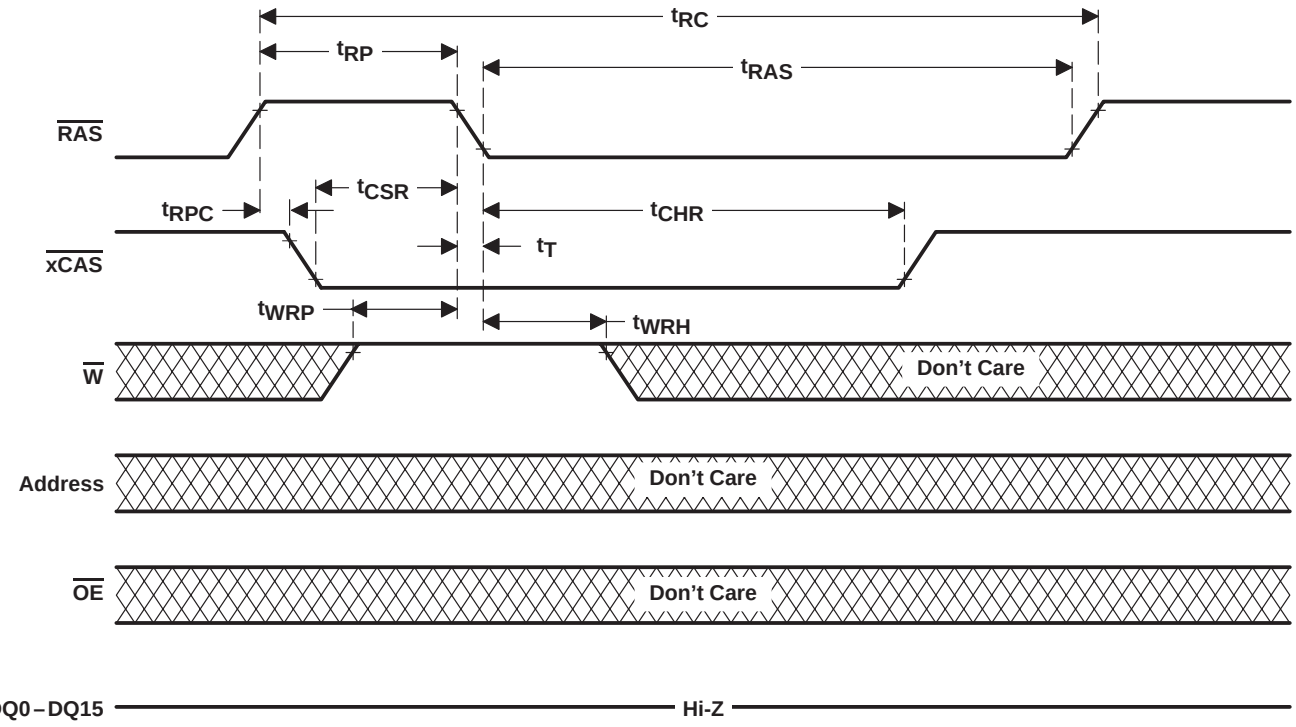


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

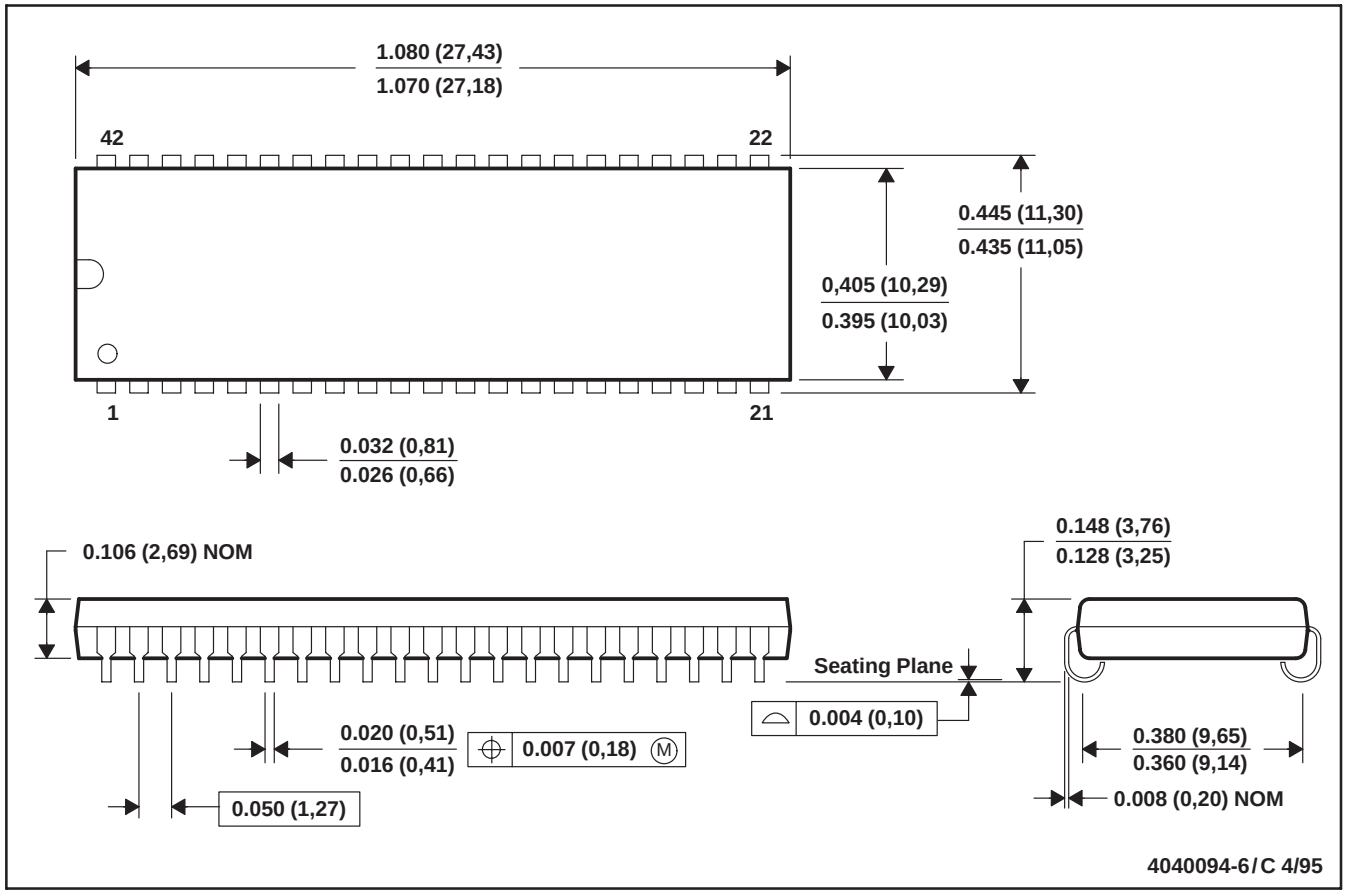


NOTE A: Any $\overline{\text{xCAS}}$ can be used. If both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are used, both must satisfy t_{CSR} and t_{CHR}.

Figure 14. Automatic-xCBR-Refresh-Cycle Timing

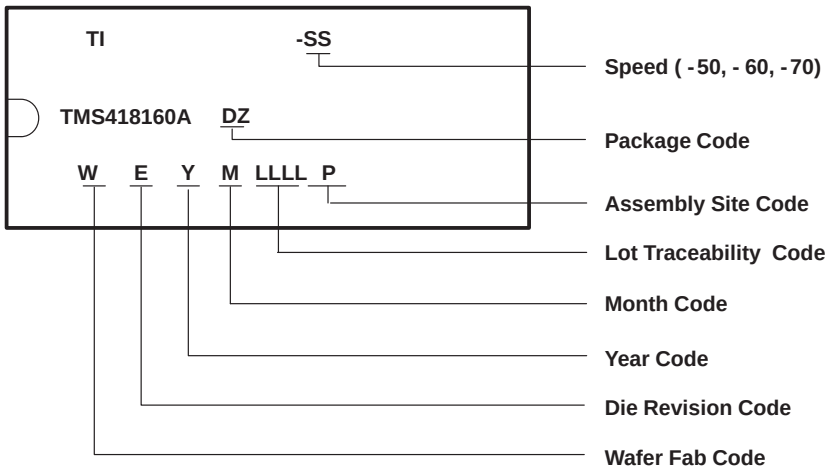
MECHANICAL DATA

DZ (R-PDSO-J42) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization



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